Single Event Upset Xilinx-Sandia Experiment (SEUXSE) on the International Space Station

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Robert Reed, Vanderbilt University
FPGA Mission Assurance Center, Univ. of New Mexico

Sponsored by National Nuclear Security Administration
Office of Nonproliferation Research and Development, NA-22

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy’s National Nuclear Security Administration under contract DE-AC04-94AL85000.
Background - Motivation

• Materials International Space Station Experiment (MISSE)
  - Experiments delivered/returned by Space Shuttle – astronaut EVA.
  - MISSE-7A&B will have power and telemetry, scheduled launch Oct. 2009.

• Internal Sandia funding was provided for MISSE-7A experiments
  - Passive exposure expt. on materials and devices.
  - Active SEU expt. on Xilinx Virtex 4 & 5 (V4 FX60, V5 LX330T).

• Goals focused on program needs with additional research benefit
  - Demonstrate capabilities of self-contained reconfigurable node: configuration, mitigation, soft-core processors, power conversion.
  - PCB fabrication with current device form factors.
  - Provide flight single and multiple bit upset Virtex 4 & 5 data to space community.
• MISSE-7 is planned for ELC2
  - S3 zenith, outboard of ISS

PEC-A, Zenith/Nadir
PEC-B, Ram/Wake
PCB Block Diagram

NOTES:
- Require +3.3V only
- Prototype Parts, also requires +3.3V
- Requires +5.0V
- Last Revised: 1001/07
Design Elements

• Xilinx OTP PROMs: configuration bit streams and processor software.
• These PROMs boot each device, then accessed by opposite Virtex for cross scrubbing.
• One PPC provides software control, self monitor for upsets, and data handling functions for V4. Second PPC runs self monitoring algorithms.
• TMRed MicroBlaze provides software control, self monitor for upsets, and data handling functions for V5 -- non-TMRed MicroBlaze runs self monitoring algorithms.
• All processors run from external SRAM including local data storage -- protected with Error-Detection-And-Correction (EDAC) circuitry.
• Each Virtex contains many different hardware logic element Device-Under-Test (DUT) units each with associated Functional Monitors (FuncMon) to detect and report SEU events.
• Each SEU event record includes time, bit location, expected and actual data values.
• FPGA environment is monitored with cross correlation to ISS radiation and environmental monitors.
• Actel provides hardware interface to ISS serial command and data channels.
• Actel contains external watchdog monitors of each Xilinx to recover from any SEFI modes.
• Custom radiation tolerant Point-Of-Load (POL) converters are used to generate all local voltages – 30 watt power allocation.
• POL converters simplify ISS power interface (single 5V source).
ISS Space Environment

- ISS Orbit: 336 km, 51.6° incl. – relatively benign radiation environment.
- Protons and heavy ions from trapped protons, galactic cosmic rays and solar flares are predicted to give 100’s of upsets/year.
- ISS Extra-Vehicular Charged Particle Spectrometer will provide real-time radiation environment data.
# On-Orbit Tests

<table>
<thead>
<tr>
<th>Test</th>
<th>V4FX60</th>
<th>V5LX330T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration/Scrubbing</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>Block RAM</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>PowerPC Cache</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>PowerPC Algorithm</td>
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<td>NO</td>
</tr>
<tr>
<td>Single MicroBlaze</td>
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<td>YES</td>
</tr>
<tr>
<td>TMR MicroBlaze</td>
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<td>YES</td>
</tr>
<tr>
<td>Gigabit Transceiver</td>
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<td>YES</td>
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<tr>
<td>Digital Clock Manager</td>
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<td>YES</td>
</tr>
<tr>
<td>DSP Blocks</td>
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<td>YES</td>
</tr>
<tr>
<td>IOB</td>
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<td>YES</td>
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</table>
Printed Circuit Board Information

- Printed Circuit Board is 6.76 inches by 13.76 inches
- 18 Circuit Layers
  - 10 signal layers
  - 8 power and ground planes
- Contains 1960 components
  - Mostly surface mounted components
  - Largest being the Xilinx 1738 and 1152 BGAs.
- Controlled impedance layers and signal traces
  - 50 ohms traces of 5.2 mils
- Differential signal pairs
  - 100 ohm traces of 4.7 mils
- Both blind and buried via interconnects between layers
  - Blind vias between layers 1-2 and 17-18
  - Buried vias between layers 2-17
Prototype Assembly

Top View

Bottom View
Devices Monitored for SEU/MBUs

- V4-FX60 on epi but in commercial packaging
- V5-LX330T commercial device
Flight Enclosure

- Volume is 7 Inches Wide By 14 Inches Long By 1.8 Inches High
  - Box mounted with screws through bottom of deck plate
- Aluminum Box with Carbon-Fiber Composite Lid (Top Face)
  - 5 sided aluminum box with alodine surface coating
  - Silver Teflon tape on alodine surfaces
  - 80-mil thick composite top lid mounted in an aluminum frame
    - Low outgassing epoxy with ~ 8 layers of pre-preg
    - Nickel plating for EMI
    - AZ-400 paint for thermal – Thanks to AZ Technology for testing.
- Mass of 5 Pounds
- Box has Rounded Edges and Corners for Astronaut Safety
- Kick Load Requirement Met
Thermal Analysis

Assumptions:
- Heat conducted from Xilinx chips to board to walls of housing, then to PEC
- Housing: Al6061-T6, 0.1 inch thick
- Board, nominal, 0.08 inch thick
- 30 W with PEC at 60C
- Orbit, 90 minute period
- No solar reflections from surrounding structure were used
- Nadir facing (earth).
- Orbital heating parameters:
  - Albedo = 0.4
  - Solar Constant = 1423 W/m²
  - Earthshine = 289 W/m²

<table>
<thead>
<tr>
<th>Model Prediction</th>
<th>Operational Limit (Components)</th>
<th>Margin</th>
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<th>Operational Limit (Components)</th>
<th>Margin</th>
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</thead>
<tbody>
<tr>
<td>Xilinx V4</td>
<td>1.1</td>
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<td>1.1</td>
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<td>95</td>
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<tr>
<td>Xilinx V5</td>
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<td>1.3</td>
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<tr>
<td>Composite Lid</td>
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</tr>
</tbody>
</table>

Temperature (C) after 8.6 hours, PEC=60C
Schedule and Future Plans

• Currently testing prototype
• 10/8/08 – Deliver prototype to NRL for system testing
• 12/5/08 – Deliver flight unit to NRL for Integration/Test
• 09/09 – Shuttle launch
• 09/09 to 10/10 – Run experiment and gather data
• 10/10? – Return on last Shuttle flight

• Flight results will be presented at future MAPLD, SEE, or NSREC conferences.
• Depending on funding, detailed modeling of the SEU/MBU effects will be performed by Robert Reed at Vanderbilt University.