



# Radiation Hardened FPGA Technology for Space Applications

## MAPLD 2008

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**October 17, 2008**



*RHAX250-S effort supported by the Defense Threat Reduction Agency*

# RHFPGA Programs at BAE SYSTEMS

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- RH FPGA Product Roadmap
  - RH FPGA Technologies
    - ONO (Oxide Nitride Oxide – Antifuse)
    - M2M (Metal to Metal Antifuse)
  - RH FPGA Program Status Review
    - Reinstall RH1020/RH1280 FPGA
    - RHAX FPGA Demonstration and Qualification Program
  - Summary and Outlook
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# Radiation Hardened FPGA Roadmap

## Rad Hard FPGA Product

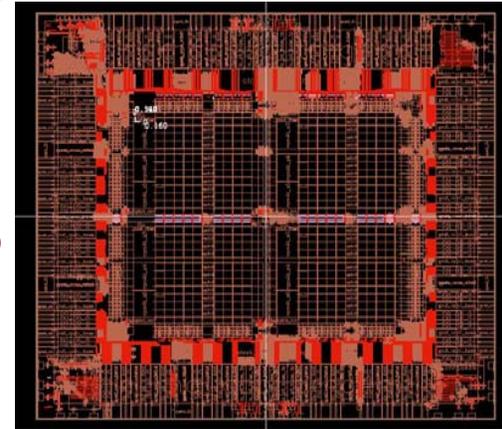
### Past

- Heritage: Actel ONO RH1280 and RH1020
- Anti-fuse technology, non-volatile
- 0.8µm RH CMOS, 5V Supply
- In production since 1996, over 25,000 shipped

Re-install  
in progress

### Present

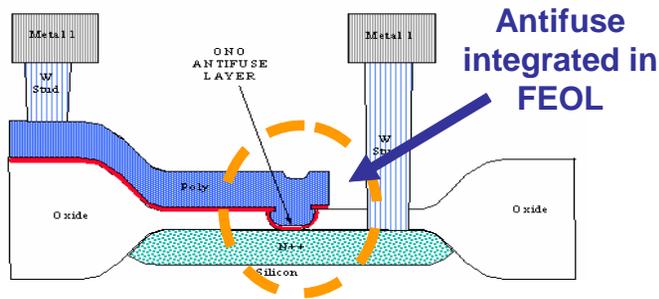
- M2M Anti-fuse Technology:
  - 250K-gate (RHAX250-S) Entry Vehicle
  - RH15 CMOS, 1.5V Core / 3.3V I/O
  - Flight Orders in 2009



### Future

- ≥3M-gate, re-programmable, non-volatile
- Radiation Hardened, high speed
- RH15 CMOS, 1.5V Core / 3.3V I/O
- Projected qualification starts in 2009

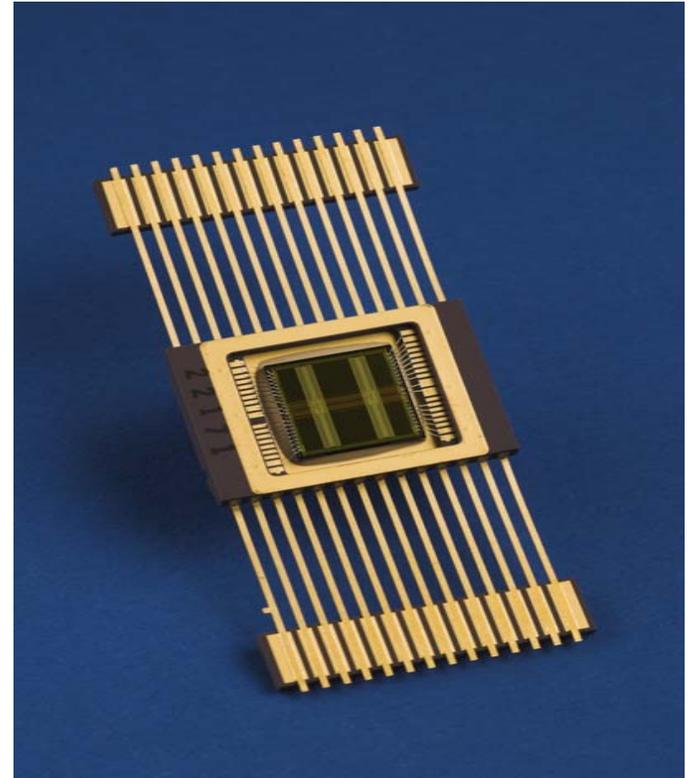
BAE Supporting RHFPGA Needs for RHOC requirements



- ONO technology : (0.8 micron features)
  - Flight qualified production (with build-out inventory) [1996-2002]
  - Process line re-tooled to support 250 and 150 nm technology nodes on 150mm wafers
- ONO technology now reinstalled in modernized foundry to restart FPGA & PROM product to supply continued demand [2007- ]
  - Used same design data  $\Rightarrow$  same form, fit, and function as product built previously
  - Keeping same 0.8 micron features

# PROM Features

- Features and Capabilities
  - Low voltage version: 32K x 8, 3.3V
    - SMD #5962G02502
  - High voltage version: 32K x 8, 5V
    - SMD #5962R96891
  - Latch-up immune
  - Total dose: 200 Krad(Si)
- Schedule and Status
  - In Production
  - Delivery in 8 weeks



# ONO Rad Hard FPGA Technology Features

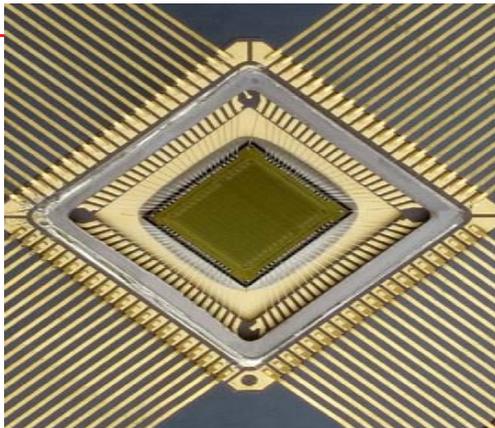
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## Features

- Guaranteed Total Dose Radiation Capability
- Low Single Event Upset Susceptibility
- High Dose Rate Survivability
- Latch-Up Immunity Guaranteed
- QML Qualified Devices
- Commercial Devices Available for Prototyping and Pre-Production Requirements
- Gate Capacities of 2,000 and 8,000 Gate Array Gates
- More Design Flexibility than Custom ASICs
- Significantly Greater Densities than Discrete Logic Devices
- Replaces up to 200 TTL Packages
- Design Library with over 500 Macro Functions
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to Two High-Speed, Low-Skew Clock Networks
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Non-Volatile, User Programmable Devices
- Fabricated in 0.8  $\mu$  Epitaxial Bulk CMOS Process
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer

## Product Family Profile

Device	RH1020	RH1280
<b>Capacity</b>		
System Gates	3,000	12,000
Gate Array Equivalent Gates	2,000	8,000
PLD Equivalent Gates	6,000	20,000
TTL Equivalent Packages	50	200
20-Pin PAL Equivalent Packages	20	80
<b>Logic Modules</b>	547	1,232
S-Modules	0	624
C-Modules	547	608
<b>Flip-Flops (Maximum)</b>	273	998
<b>Routing Resources</b>		
Horizontal Tracks/Channel	22	35
Vertical Tracks/Channel	13	15
PLICE Antifuse Elements	186,000	750,000
<b>User I/Os (Maximum)</b>	69	140
<b>Packages (by Pin Count)</b>		
Ceramic Quad Flat Pack (CQFP)	84	172



## Radiation Specifications

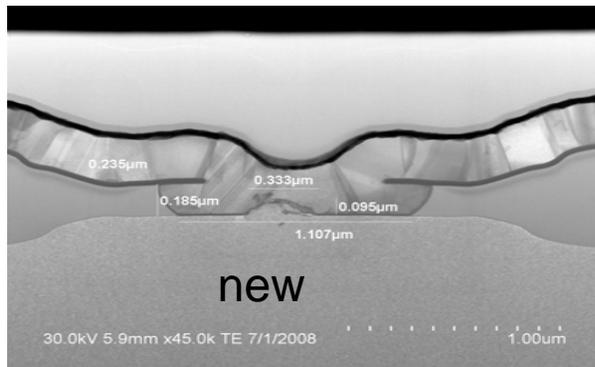
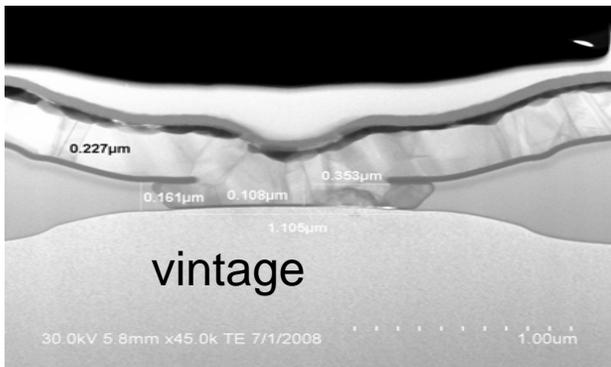
Table 1-2 • Radiation Specifications<sup>1,2</sup>

Symbol	Characteristics	Conditions	Min.	Max.	Units
RTD	Total Dose			300 k	Rad (Si)
SEL	Single Event Latch-Up	$-55^{\circ}\text{C} \leq T_{\text{case}} \leq 125^{\circ}\text{C}$		0	Fails/Device-Day
SEU1 <sup>3</sup>	Single Event Upset for S-modules	$-55^{\circ}\text{C} \leq T_{\text{case}} \leq 125^{\circ}\text{C}$		1E-6	Upsets/Bit-Day
SEU2 <sup>3</sup>	Single Event Upset for C-modules	$-55^{\circ}\text{C} \leq T_{\text{case}} \leq 125^{\circ}\text{C}$		1E-7	Upsets/Bit-Day
SEU3 <sup>3</sup>	Single Event Fuse Rupture	$-55^{\circ}\text{C} \leq T_{\text{case}} \leq 125^{\circ}\text{C}$		<1	FIT (Fails/Device/1E9 Hrs)
RNF	Neutron Fluence		>1 E+12		N/cm <sup>2</sup>

**Notes:**

1. Measured at room temperature unless otherwise stated.
2. Device electrical characteristics are guaranteed for post-irradiation levels at worst-case conditions.
3. 10% worst-case particle environment, geosynchronous orbit, 0.025" of aluminum shielding. Specification set using the CREME code upset rate calculation method with a 2 μ epi thickness.

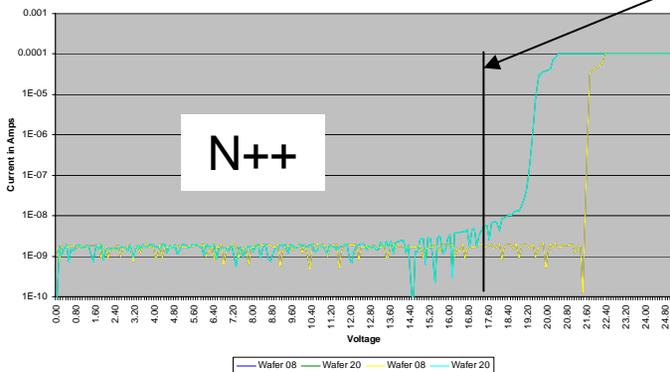
## ONO Anti-fuse Cross sections - Programmed



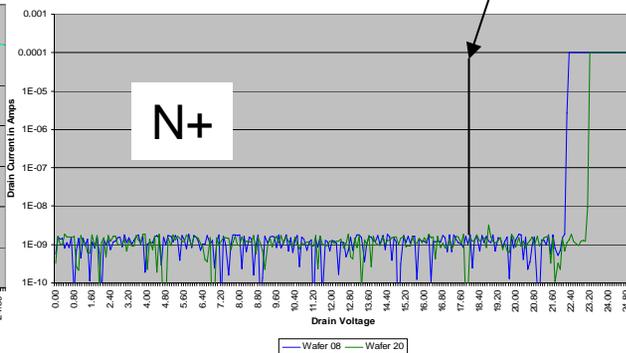
## Device Electrical Parameters

### Junction Breakdown Requirement

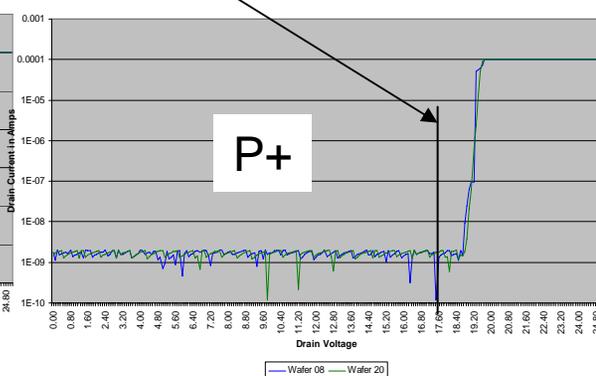
Lot: 2080477 Site: Center Macro: HVNCAF Structure: bottom N++ of ONO  
Test: Breakdown  
Diffusion Swept from 0 to 25 Volts - Substrate Ground



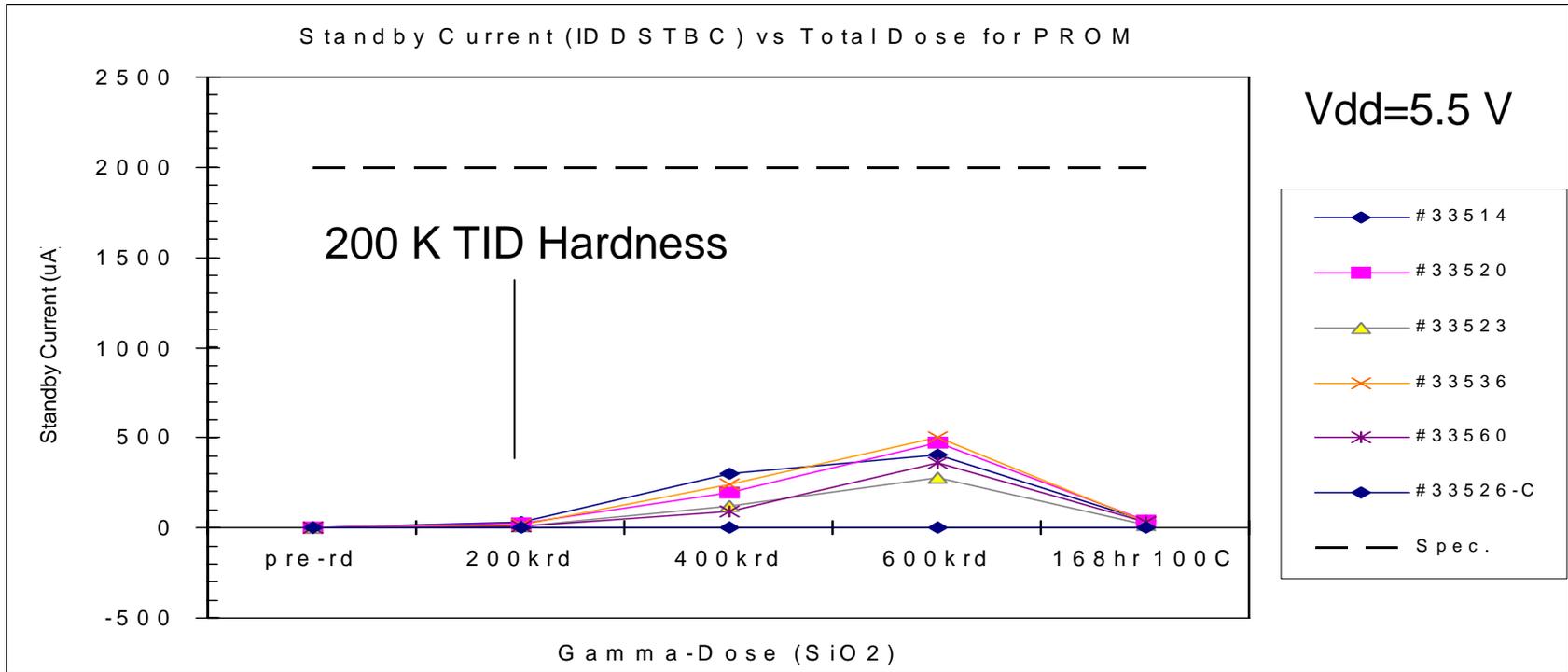
Lot: 2080477 Site: Center Macro: HVNFBET Structure: 50/1.3  
Test: Breakdown  
Drain Swept from 0 to 25 Volts - Source, Gate, Substrate Ground



Lot: 2080477 Site: Center Macro: HVPFBET Structure: 50/1.3  
Test: Breakdown (Absolute Values)  
Drain Swept from 0 to 25 Volts - Source, Gate, Well Ground



# RH ONO Technology TID Data - PROM



- Active current, VIL, VIH, Access time and chip enable time all remain stable through 600 Krd

**RH PROM Exceeds 200 Krad TID Requirements**

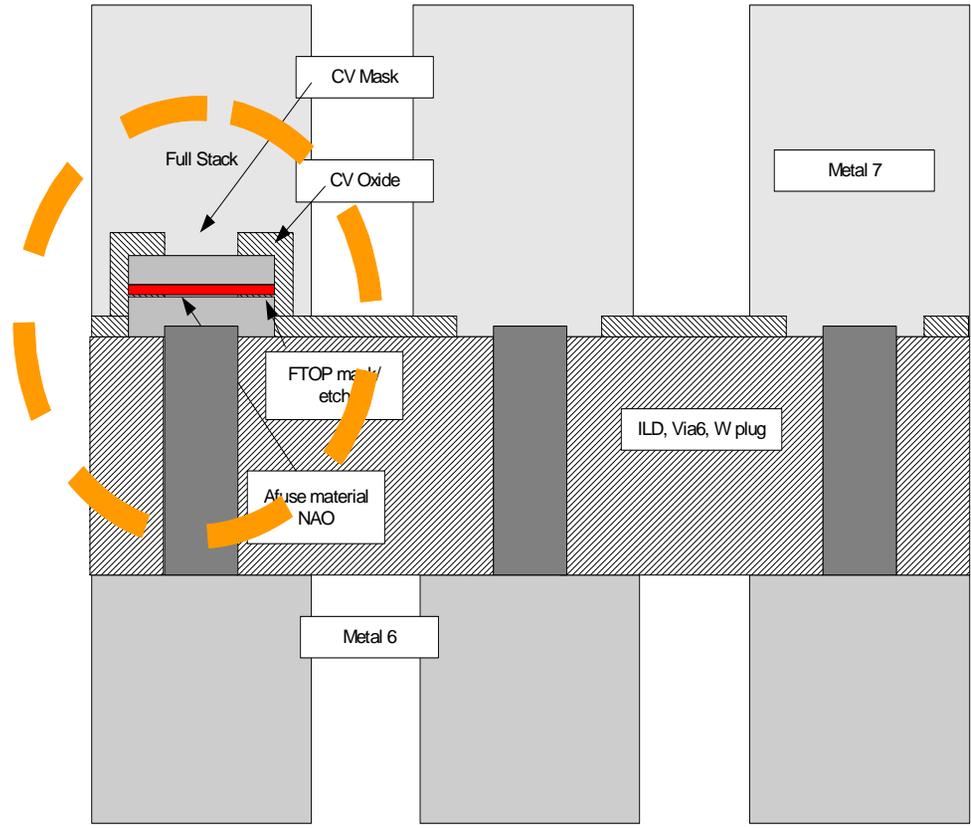
- Successfully reinstalled ONO process technology
- Flight-qualified PROM production restarted
- RH1280B prototype hardware successfully delivered, flight hardware in qualification.
  - BAE acquired license from Actel to produce, market and sell RH1280 FPGA's
  - SEGR completed successfully, TID testing in progress
- RH1020 FPGA build underway for prototype and flight Qualification

**ONO FPGA Flight Hardware in Production**

**Orders being taken for shipments in 2008**

# Metal to Metal Antifuse Based FPGA's

Antifuse  
integrated in  
BEOL





# Product Installation Approach



**Low Risk: Port a proven RT design to a validated RH process.**



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PROCESS

**FPGA**  
Unique features  
- High Voltage Tx  
- Anti-fuse

*RH FPGA process derived from the integration of unique features into rad hard 150nm base technology (RH15)*

**RH15**  
Radiation Hardened 150nm CMOS Process Technology on Epi Wafers

**Radiation Hardened 150nm CMOS Technology with features that support RH FPGA's**

**Actel**

DESIGN

*RH FPGA design results from the porting of proven rad tolerant design onto rad hard process technology*

**Proven RTAX250-S Design**

**RHAX250-S**

RTAX250-S is a 150nm product built at a commercial foundry on non-epi substrates.



# RHAX250-S Installation and Qualification Roadmap

## Approach

**RTAX250-S**

- RT AX250-S design transferred to BAE

**Process & Design Rule Development**

- assess RTAX design rules & process details
- define process flow
- create parametric targets
- build & evaluate short loops (Hi-V Tx; antifuse)

**Process Integration / Technology Validation**

- design technology characterization vehicle (TCV)
- build & evaluate full TCV lots

**Product Demonstration  
Prototypes Built & Tested**

**QML Qualification**

- perform qualification testing on FPGA samples taken from  $\geq 3$  lots

**RHAX250-S**

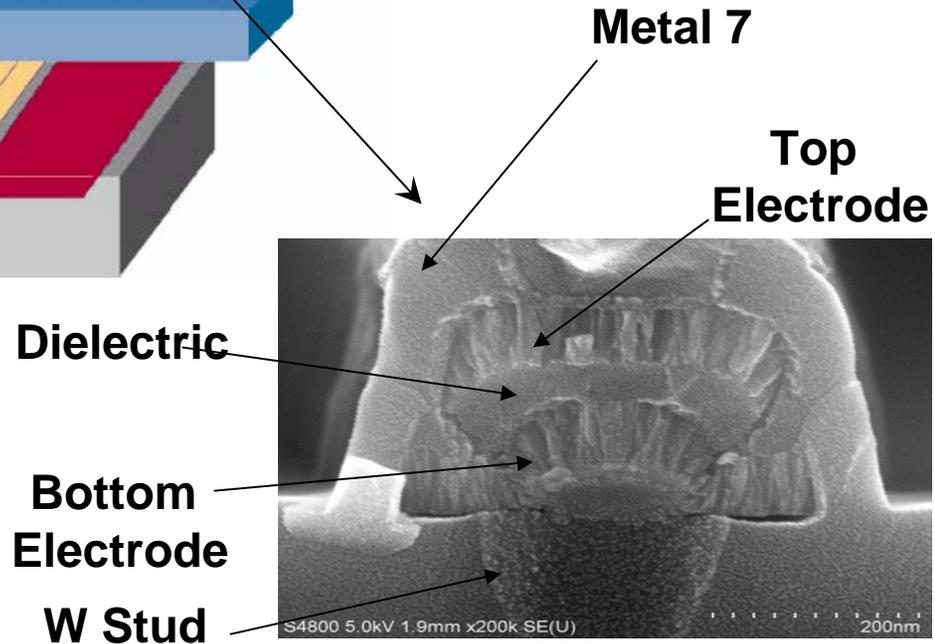
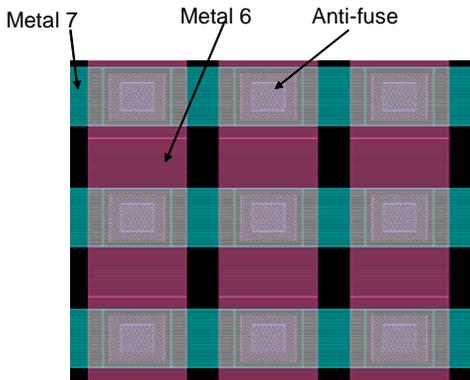
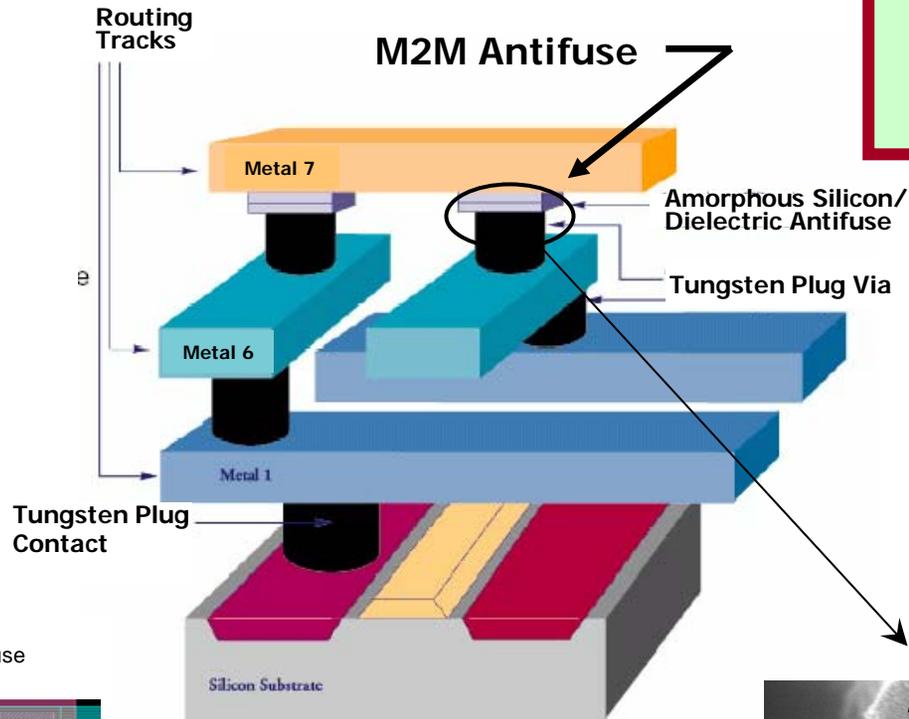
- flight qualified product, same form/fit/function

**Port Other RTAX Designs**



# Metal-to-Metal Antifuse

**Antifuse Placement:  
Between to last two metal  
layers, NOT inside the via  
but above the W-stud.**





# RHAX250-S Product Profile

<b>Device</b>	<b>RHAX250-S</b>
<b>Capacity</b>	
Equivalent System Gates	250,000
ASIC Gates	30,000
<b>Modules</b>	
Register (R-Cells)	1,408
Combinatorial (C-Cells)	2,816
Flip-Flops (Maximum)	2,816
<b>Embedded RAM/FIFO (without EDAC)</b>	
Core RAM Blocks	12
Core RAM Bits (K = 1,024)	54 K
<b>Clocks Segmentable</b>	
Hardwired	4
Routed	4
<b>I/O's</b>	
I/O Banks	8
User I/O's (Maximum)	248
I/O Registers	744
<b>Package</b>	
CCGA/LGA	-
CQFP	208, 352

### Performance

1.5V Core; 3.3V I/O
High-Performance Embedded FIFOs
350+ MHz System Performance
500+ MHz Internal Performance
700 Mb/s LVDS Capable I/Os

### Radiation Hardness Targets

TID	≥ 1Mrad(Si)
DR Upset	> 1E9 rad(Si)/sec
SEL	Immune
SEU <sub>REGS</sub>	< 1E-10 errors/bit-day (TMR-hardened)
SEU <sub>e-RAM</sub>	< 1E-10 errors/bit-day (EDAC)



**RHAX FPGA will have the identical form, fit, and function of its RTAX counterpart.**



# Predicted SEU Rates

vs. logic level & freq.

Test data taken on RTAX Product

Predicted SEU Rates (errors/bit/day) \*

Levels of Intervening Logic	Signal Frequency			
	15 MHz	37.5 MHz	75 MHz	150 MHz
8-Levels	5.31E-09	7.88E-09	3.75E-08	8.17E-08
4-Levels	2.01E-09	8.71E-09	1.89E-08	6.29E-08
0-Levels	6.08E-10	5.14E-09	2.84E-08	5.84E-08

Worsening SEU Rate

(Probability of Generating an SET)



Logic



Frequency

(Probability of Capturing an SET)

\* assumed radiation environment: GEO-min and 100-mil Al shielding

**Impact of SET on error rate depends on circuit design and signal frequency.**



**Further SEU Enhancements projected in Rad Hard Process using Epi layer**



# RHAX250-S Prototype Hardware

Prototype RHAX250-S FPGA's have yielded functional hardware,

Modules were programmed for total ionizing dose testing.

Circuit elements tested per module:

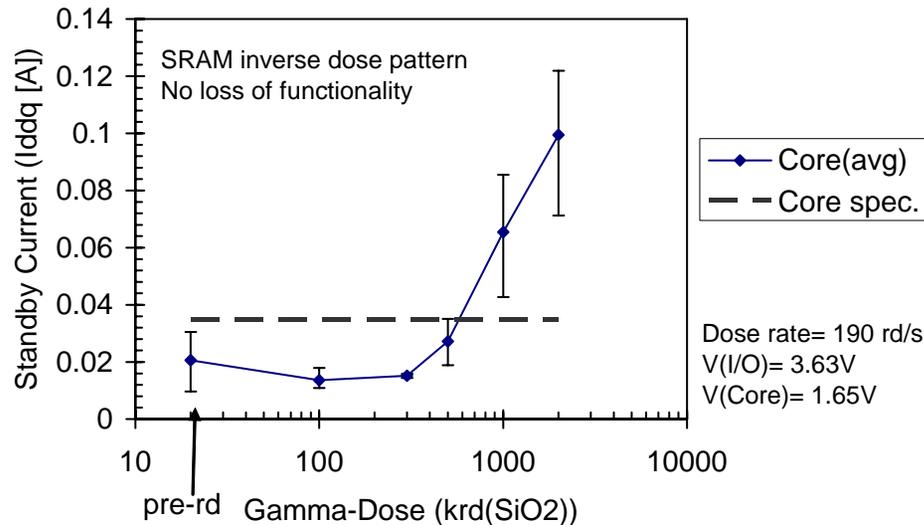
- 12 blocks of 4Kx1 SRAM (total: 48K)
- 1408-stage DFF register string
- Two 1408-stage logic chains



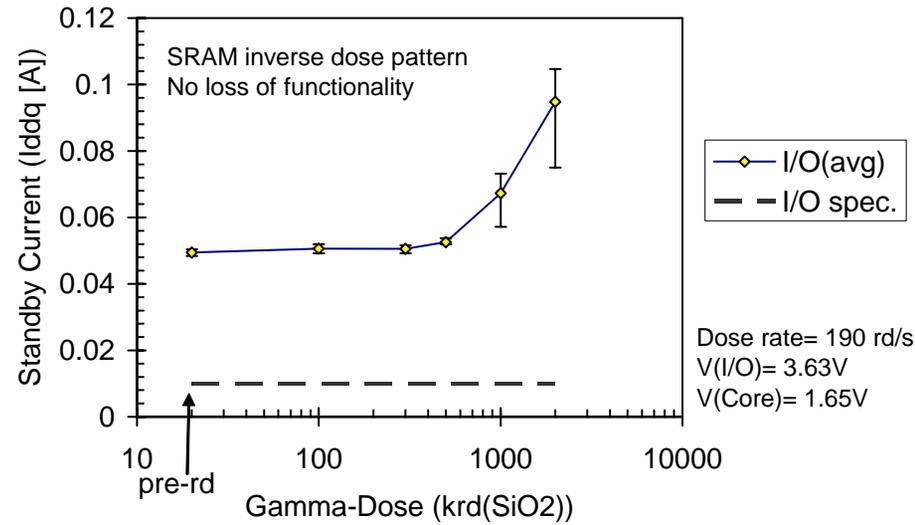
# RHAX250-S TID Test Results

RHAX250-S modules remained fully functional throughout testing to 2Mrd(SiO<sub>2</sub>)

TID Core Iddq Results for RHAX250-S



TID I/O Iddq Results for RHAX250-S



**TID test results on prototype FPGA's demonstrate improved hardness. Hardening process adjustments are being implemented to further enhance hardness.**



# Process Improvements

- Parts successfully programmed at Actel, with latest QCMON
  - Used NASA-Industry Tiger Team Algorithm
  - Parts pass all 346 tests at 125 Degrees C except Icca , standby current exceeded specification limit
  - Further leakage reduction required for flight parts

Lot 421 QCMON (346 Total Tests)									
PARTS	Contact Test	QCMON Funct	QCMON Hi Z	Input Current High	Input Current Low	Input Pull Ups	Input Pull Dns	Pwr Supply Stdbby Currents	Icca Stdbby Current
Mod # 1	P	P	P	P	P	P	P	P	20.3mA*
Mod # 2	P	P	P	P	P	P	P	P	31.5mA*
<b>P=PASS</b>		* Note: Spec limit is 20 mA.							



# Work in progress

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- Build more hardware incorporating identified process enhancements for further leakage reduction
- Subject functional hardware to full battery of reliability and radiation testing
- QML qualify the RHAX process technology
- Begin full RHAX250-S wafer production to supply Actel
- Port additional Actel RTAX FPGA designs onto rad hard process technology at BAE to extend rad hard offerings.



# Summary

- BAE and Actel are continuing their >12 year collaboration as rad hard FPGA suppliers.
- Next generation rad hard product is being built and tested.
- Total dose test results on RHAX250-S hardware demonstrates improved hardness over RTAX250-S.
- Single-event effects test results on AX250 demonstrates product design's high tolerance.
- Electrical, radiation, and reliability testing is on-going.
- Full flight-qualified production in progress for ONO technology and projected to start M2M technologies in early 2009



# Acknowledgements

BAE SYSTEMS

**The authors gratefully acknowledge the support for this effort provided by the Defense Threat Reduction Agency under contract DTRA01-03-D-0007 / 0004.**



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