MAPLD'09 Conference, Greenbelt, MD

CHREC
NSF Center for High-Performance Reconfigurable Computing

CHREC Novo-G

Alan D. George
Founder and Director of CHREC
Professor of ECE, Univ. of Florida

Herman Lam
Faculty Member of CHREC
Assoc. Professor of ECE, Univ. of Florida

This work was supported in part by the I/UCRC Program of the National Science Foundation under Grant No. EEC-0642422.
We also gratefully acknowledge Novo-G support provided by Altera, GiDEL, Impulse, Mitrionics, Aldec, & Synopsys.

Outline

- CHREC Overview
  - Mission
  - Structure
- CHREC Novo-G
  - Concept
  - Machine
  - Tools & participating CHREC projects
  - Applications in development
  - Future plans
- Conclusions

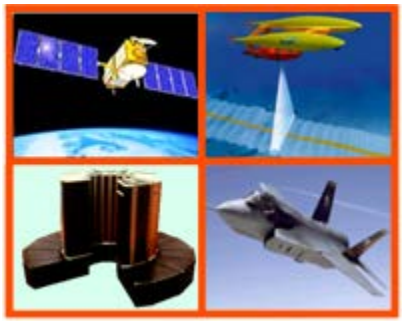
CHREC Overview

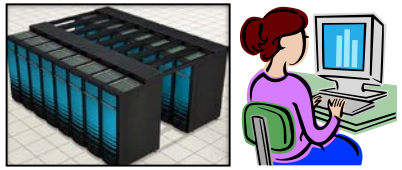
What is CHREC?

CHREC
NSF Center for High-Performance Reconfigurable Computing

- NSF Center for High-Performance Reconfigurable Computing
  - Unique US national research center in this field, established Jan'07
  - Leading ECE/CS research groups @ four major universities
    - **University of Florida** (lead)
    - **Brigham Young University**
    - **George Washington University**
    - **Virginia Tech**
- Under auspices of I/UCRC Program at NSF
  - **Industry/University Cooperative Research Center**
    - CHREC is supported by CISE & Engineering Directorates @ NSF
  - CHREC is both a National Center and a Research Consortium
    - University groups serve as research base (faculty, students, staff)
    - Industry & government organizations are research partners, sponsors, collaborators, advisory board, & technology-transfer recipients
  - **CHREC is recognized by NSF as one of its BEST national centers**

CHREC Mission



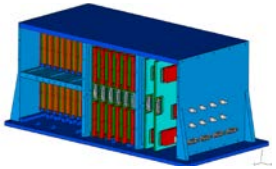


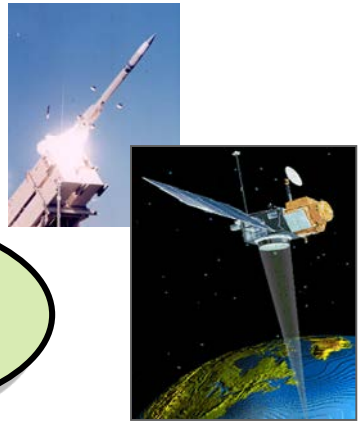
RC

CHREC

HPC

HPEC





Mission

Basic and applied R&D to advance S&T in advanced computing in these 3 increasingly overlapping domains.

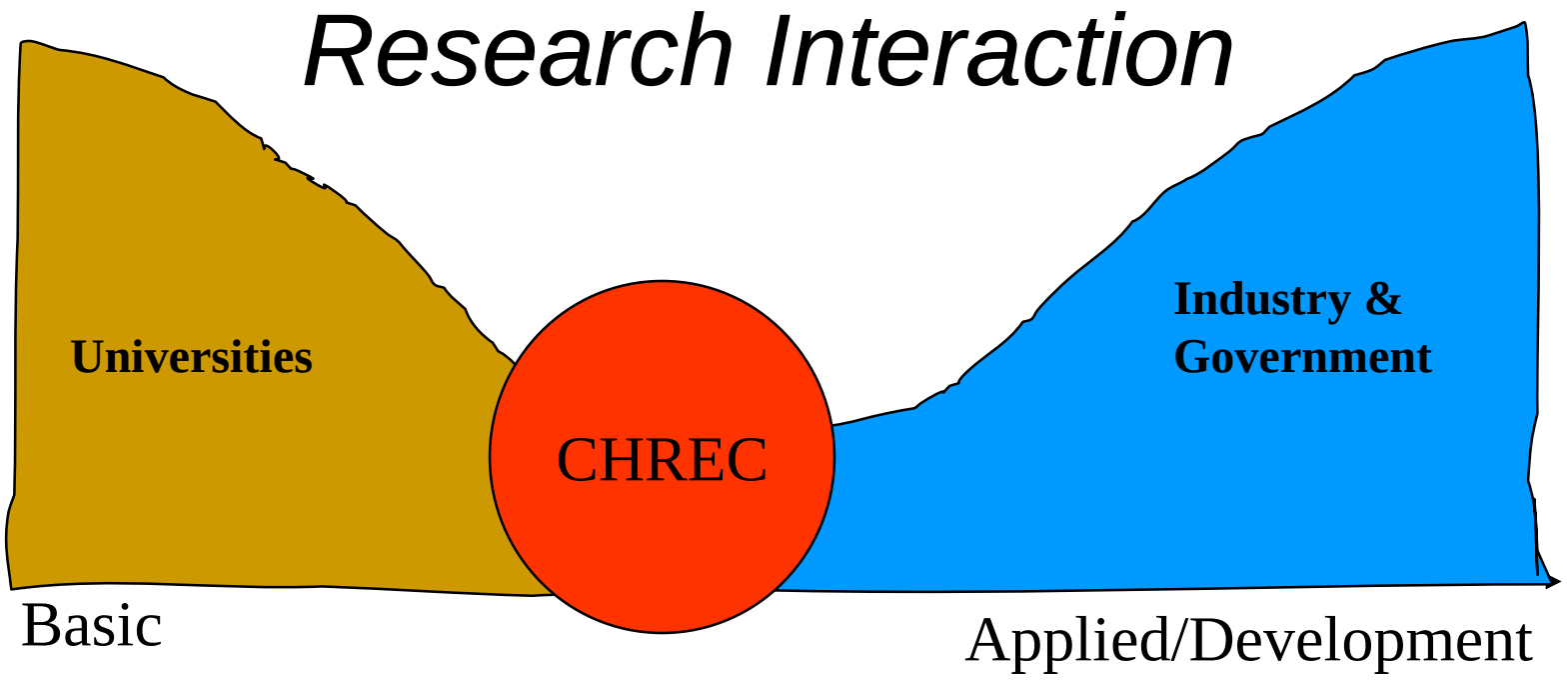
Many common challenges, technologies, & benefits, in terms of performance, power, adaptivity, productivity, cost, size, etc.

From device/system architectures to design concepts and tools.

From satellites to supercomputers!

Heavy emphasis upon MAPLD-related challenges

NSF Model for I/UCRC Centers



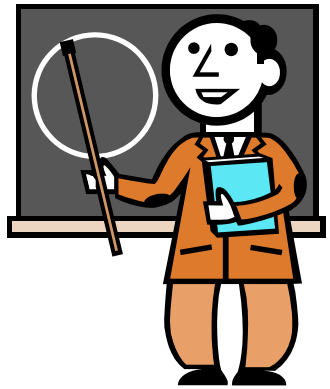
CHREC Members

1. AFRL Munitions Directorate (2)
2. AFRL Space Vehicles Directorate
3. Altera
4. AMD
5. Arctic Region Supercomputing Center (2)
6. Boeing Phantom Works (2)
7. Harris
8. Hewlett-Packard
9. Honeywell (2)
10. Intel
11. L-3 Communications
12. Lockheed Martin MFC
13. Lockheed Martin SSC
14. Los Alamos National Laboratory (2)
15. Luna Innovations
16. NASA Dryden Flight Research Center
17. NASA Goddard Space Flight Center
18. NASA Marshall Space Flight Center
19. National Instruments
20. National Reconnaissance Office (4)
21. National Security Agency *
22. Oak Ridge National Laboratory (2)
23. Office of Naval Research
24. Raytheon
25. Rincon Research Corp.
26. Sandia National Laboratory NM (2)
27. SEAKR Engineering
28. Xilinx

Many MAPLD-related organizations

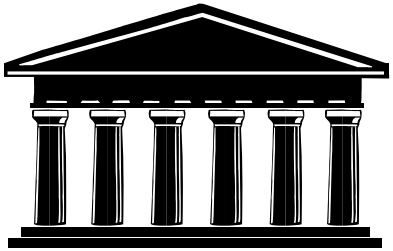
* '09 funds pending

CHREC Faculty



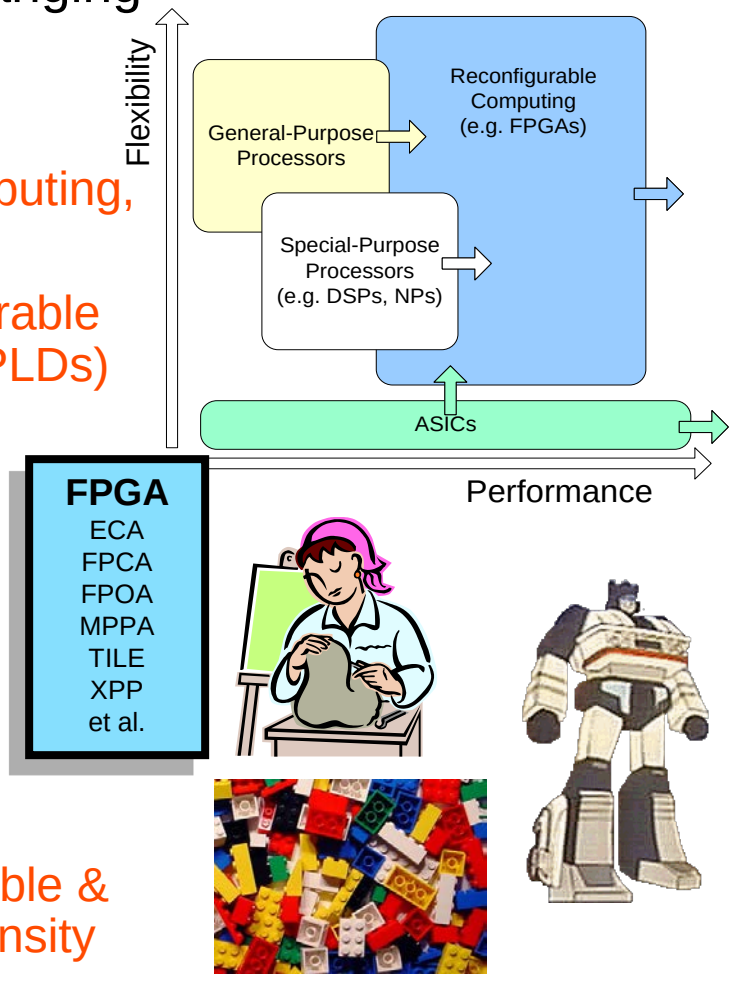
- **University of Florida (lead)**
  - **Dr. Alan D. George**, Professor of ECE – ***Center Director***
  - **Dr. Herman Lam**, Associate Professor of ECE
  - **Dr. Ann Gordon-Ross**, Assistant Professor of ECE
  - **Dr. Greg Stitt**, Assistant Professor of ECE
  - **Dr. K. Clint Slatton**, Associate Professor of ECE and CCE
- **Brigham Young University**
  - **Dr. Brent E. Nelson**, Professor of ECE – ***BYU Site Director***
  - **Dr. Michael J. Wirthlin**, Associate Professor of ECE
  - **Dr. Brad L. Hutchings**, Professor of ECE
  - **Dr. Michael Rice,** Professor of ECE
- **George Washington University**
  - **Dr. Tarek El-Ghazawi**, Professor of ECE – ***GWU Site Director***
  - **Dr. H. Howie Hwang**, Assistant Professor of ECE
  - **Dr. Vikram Narayana** & **Dr. Saumil Merchant**, Post-doc Research Scientists
- **Virginia Tech**
  - **Dr. Peter Athanas**, Professor of ECE – ***VT Site Director***
  - **Dr. Wu-Chun Feng**, Associate Professor of CS and ECE
  - **Dr. Francis K.H. Quek**, Professor of CS
  - **Dr. Shawn Bohner**, Courtesy Professor of CS

Most importantly, CHREC features a very strong team of students spanning our four university sites (majority US)



What is RC?

- Adaptive forms of computing capable of changing hardware structure to meet app demands
  - Static or dynamic reconfiguration
  - Reconfigurable computing, configurable computing, custom computing, adaptive computing, etc.
  - Often a mix of conventional fixed & reconfigurable devices (e.g. control-flow CPUs, data-flow FPLDs)
- Enabling technologies?
  - Field-programmable multicore devices
  - FPGA is "Patriarch" (but space is broadening)
  - Even Intel, AMD, IBM, & Microsoft engaged
- Applications?
  - Vast range – HPC, HPEC, GPC, et al.
  - Faster, smaller, less power, less heat, adaptable & versatile, selectable precision, high comp. density



Opportunities for RC?

10-100x speedups with
2-10x energy savings
in many cases

From Satellites to Supercomputers!

Performance ↑
Power ↓

RC: Application-oriented, software-controlled, hardware-adaptive computing

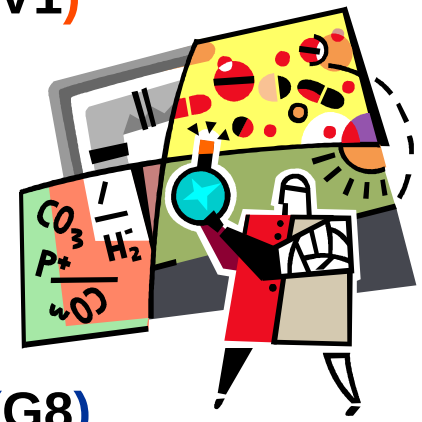
CHREC Research History

- 8 projects completed in 2007 (2 schools)
  - 8 scholarly conference & journal papers approved, published
  - Variety of other results (e.g. tools, codes, cores, graduates)
  - All motivated by interests & tech transfer of CHREC members
  - ~20 students supported
- 14 projects completed in 2008 (4 schools)
  - 17 scholarly conference & journal papers approved, published
  - Variety of other results (e.g. tools, codes, cores, graduates)
  - All motivated by interests & tech transfer of CHREC members
  - ~40 students supported
- 12 projects underway in 2009 (4 schools)
  - Already >22 scholarly conference & journal papers approved, published
  - ~40 students being supported

CHREC 2009 Research Projects

Device & System Architectures

- RC Device Architecture Exploration (F5)
- Characterizing and Optimizing Emerging Devices (V1)
- An API for Autonomous Adaptive Systems (V3)



Productivity Tools

- System-level Formulation and Design (F1)
- Translation and Execution Productivity (F2)
- Reuse Tools for RC Design (B1)
- Unified Parallel Programming of Tilera using UPC (G8)

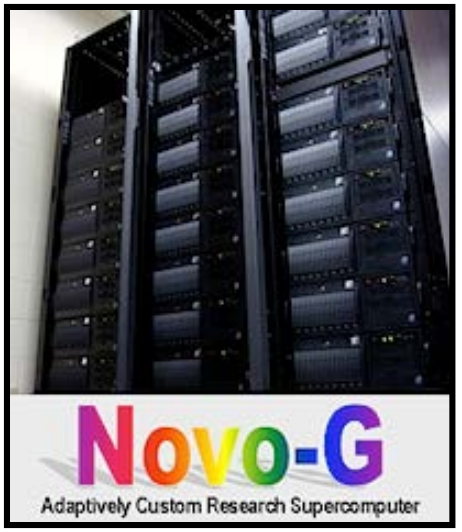
Fault Tolerance & Partial Reconfiguration

- Virtual Arch. & Design Automation for Partial Reconfiguration (F4)
- Reconfigurable & Hybrid Fault Tolerance (F6)
- Reliable RC Design (B5a&b)
- Virtualizing FPGA Resources for HPRCs (G7)

(where F=Florida, B=BYU, G=GWU, V=VaTech)

CHREC Novo-G

Novo-G Concept



- **Goals**
  - Investigate, develop, evaluate, & showcase:
    - Most powerful RC machine ever fielded for research
    - Innovative suite of productivity tools for app development
    - Impactful set of scalable kernels/apps in key science areas
  - Project & machine name: Novo-G
    - "**Novo**" is Latin: "to make anew, refresh, revive, change, alter," essence of RC
    - "**G**" for genesis (first of a series of Novo machines)
  - Focus on experimental research challenges of RC spanning **HPC** to **HPEC**
- **Motivations**
  - Design productivity is foremost need/challenge for widespread use of RC
  - Challenges accentuated as scale increases (devices, systems, apps)
  - Powerful experimental testbed to support R&D addressing these challenges
- **Emphases**
  - *Performance* (system), *Productivity* (concepts/tools), *Impact* (apps)

Novo-G Machine

- Cluster of 24+1 servers (compute + head node)
  - 96 Altera Stratix-III E260 FPGAs for app acceleration
    - Each w/ 768 18x18 multipliers, 254K logic elements, 204K registers, power <25W
      - e.g. On E260, 768 Integer, 192 SPFP, or 85 DPFP multipliers @ ~300MHz (Altera FPC)
    - System peak >22 Tops (Int), >5TFlops (SP), >2.5TFlops (DP) solely in FPGAs
  - FPGAs housed in four quad-FPGA PCIe x8 GiDEL boards
    - *Embedded-style* boards; supports both HPEC- & HPC-oriented research
    - 4.25GB memory attached to *each* app FPGA, 576GB total RAM in Novo-G
  - 24 boards housed in 24 Linux compute servers + head node
    - 20Gb/s non-blocking DDR InfiniBand; Gigabit Ethernet
    - 26 (24+2) quad-core 2.26GHz Intel Nehalem Xeon processors w/ QPI
- Funded by U. Florida plus special vendor discounts

Novo-G Machine

KVM/LCD unit for head node

1 head-node server with:

- 1U rackmount chassis
- Dual Xeon E5520 quad-core CPUs @ 2.26 GHz, 4MB Cache, 5.86 GT/s QPI
- 24GB ECC DDR3, 1333 MHz
- Integrated dual-GigE ports & video
- ICH10R controller for 6 SATA drives
- 3 x 1TB Enterprise SATA2 drives

24 compute servers, each with:

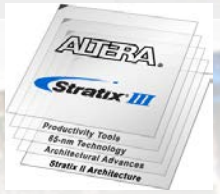
- 4U rackmount chassis with 645W P/S
- Intel Xeon E5520 quad-core CPU
- 6GB ECC DDR3, 1333 MHz
- Integrated dual-GigE ports & video
- GiDEL ProcStar-III PCIe x8 card
- Mellanox DDR InfiniBand PCIe card
- 250GB SATA2 drive

Not visible (IB & GigE switches, PDUs)

Novo-G ProcStar-III Board (one of 24)

GiDEL ProcStar-III Board	
Typical frequencies	100-325MHz
DMA channels	32
DDR2 module slots	8

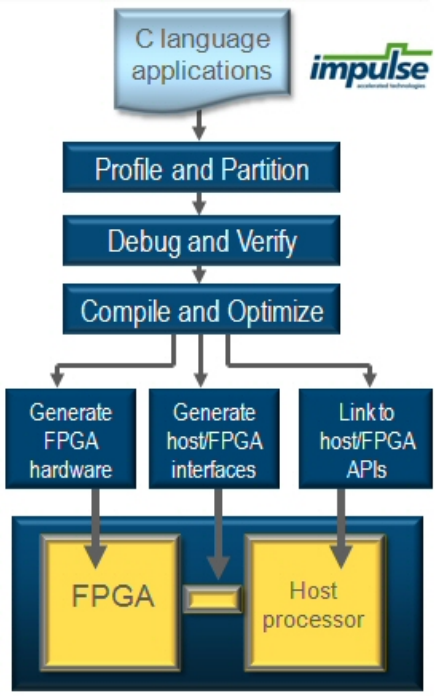
Altera Stratix-III E260 FPGA	
254,400	Logic Elements
768	multipliers (18×18)
14,688	Kbits of embedded memory
50%	less power than Stratix-II
65nm	technology



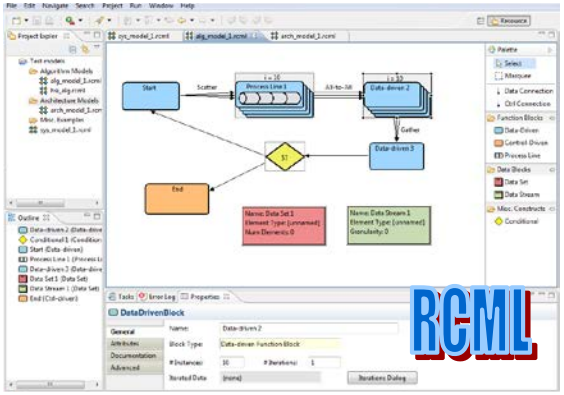
GiDEL

Novo-G Tools

- Commercial and open-source tools
  - Digital design tools: Altera, GiDEL, Aldec, Synopsys
  - Cores and libraries: Altera, GiDEL
  - High-level device design: Altera FPC, Impulse-C, Mitrion-C, SynplifyDSP, others TBD (e.g. OpenCL)
  - High-level system design: MPI, UPC, SHMEM
  - Other options now in discussion with several vendors



- Variety of CHREC tools being ported and used for Novo-G
  - Strategic design & prediction: RCML, RCSE, RAT
  - High-level system design: SHMEM+, SCF
  - Hardware virtualization for fast PAR: IFET
  - App verification & performance analysis: ReCAP
  - Assorted kernel & app cores



Example: Productivity Research

Reuse

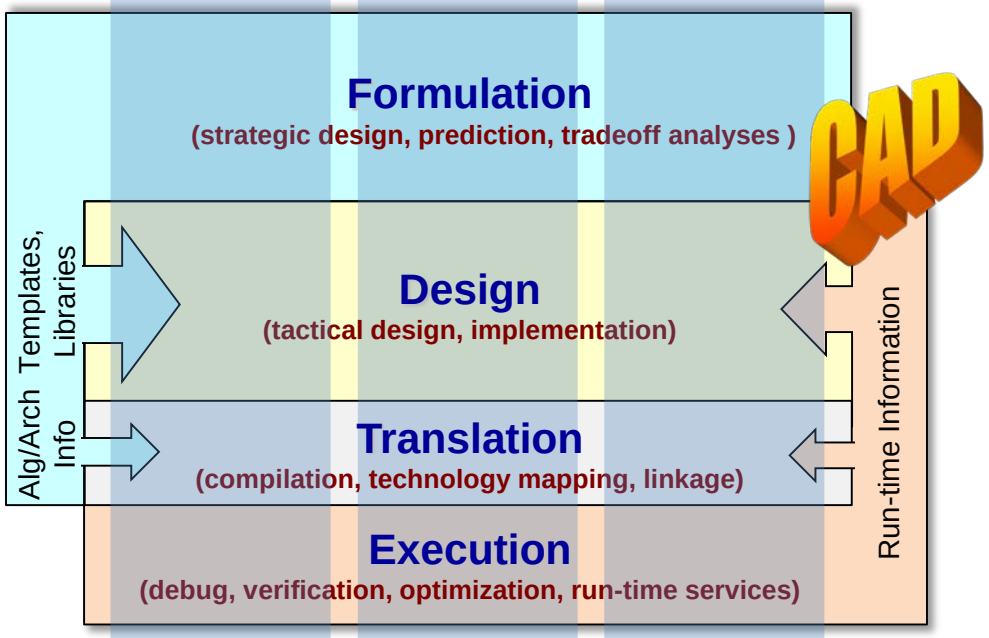
Exploit reuse in all phases to leverage pre-existing artifacts, requiring less original development

Abstraction

Exploit higher-level abstractions at each phase to reduce details and focus on separation of concerns

Turns per day

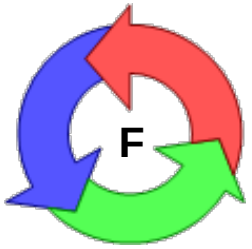
Significantly increase "turns per day" to reduce time and effort to iterate in development flow



Integration

Integrated end-to-end development environment improves flow, automation, reuse, and turns per day; maximizes productivity

$$\psi = \frac{U}{C}$$



Formulation-driven

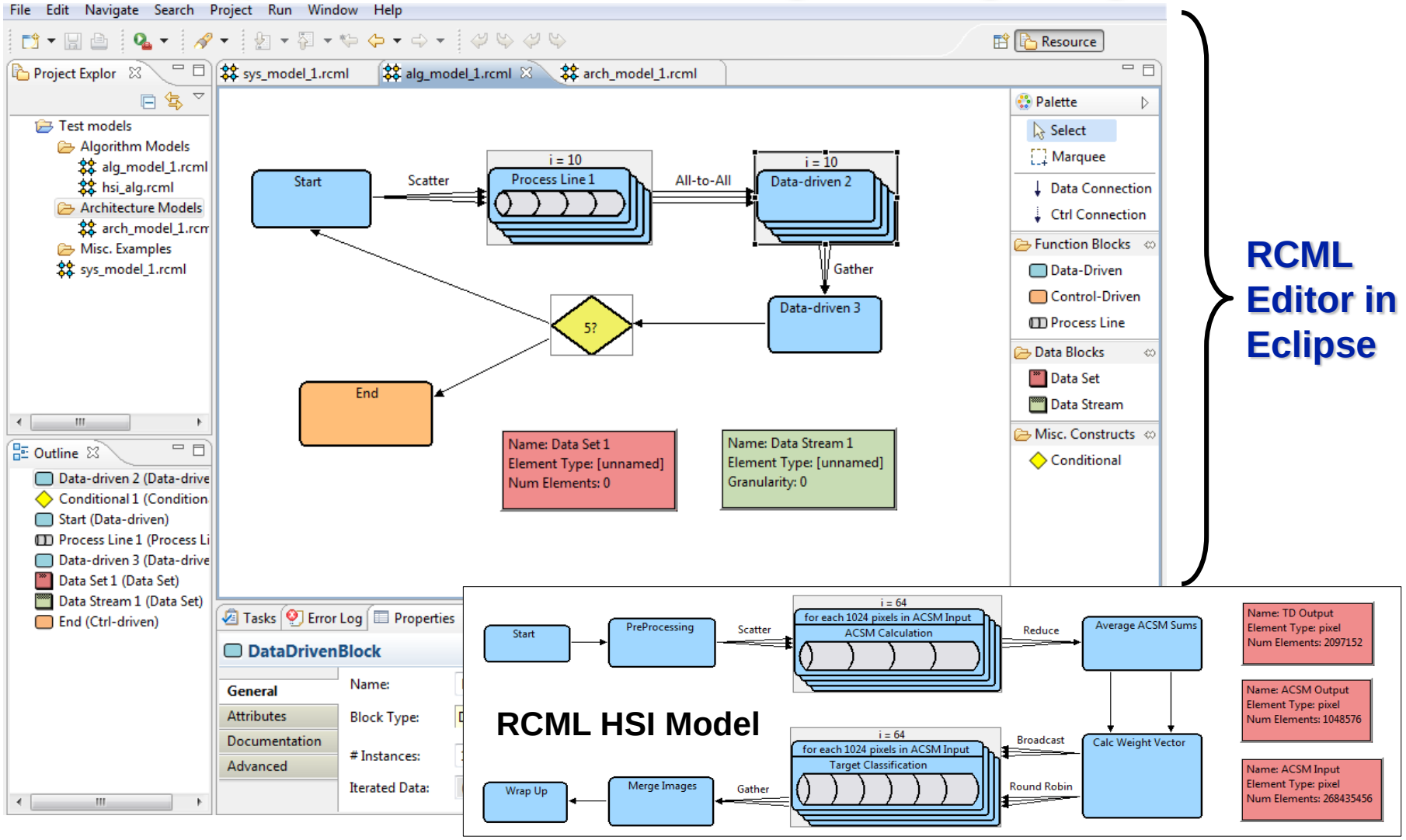
Time spent in Formulation phase saves far more in other (DTE) phases

Projected productivity impact on order of 20×
(vs. current design methods & tools)

CHREC
NSF Center for High-Performance Reconfigurable Computing

UF UNIVERSITY of FLORIDA
Virginia Tech
BYU BRIGHAM YOUNG UNIVERSITY
THE GEORGE WASHINGTON UNIVERSITY

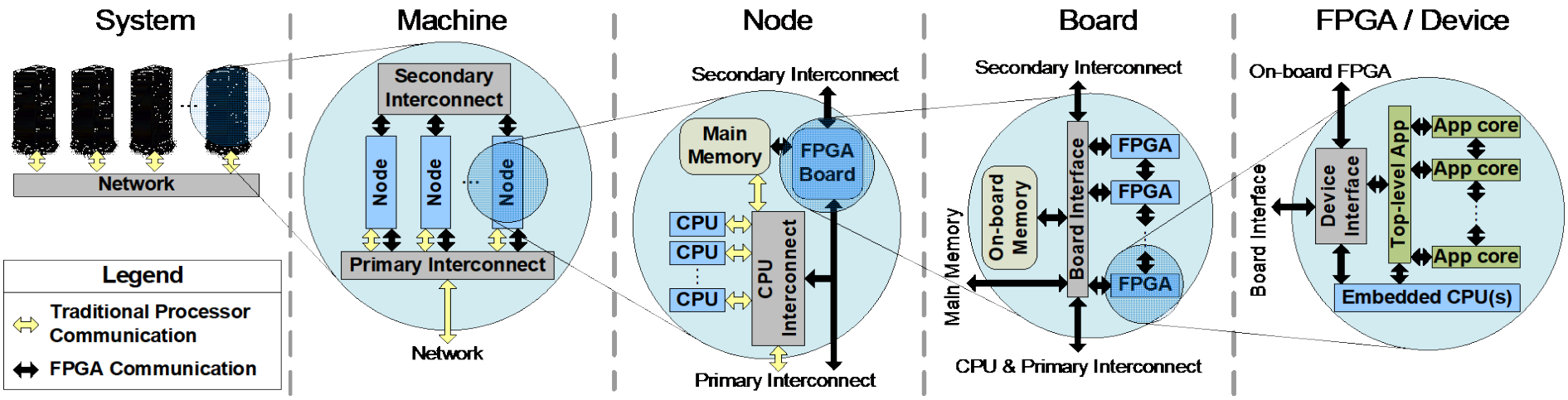
Example: RC Modeling Language

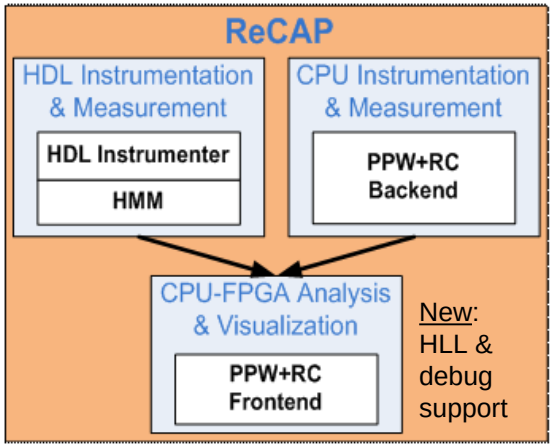


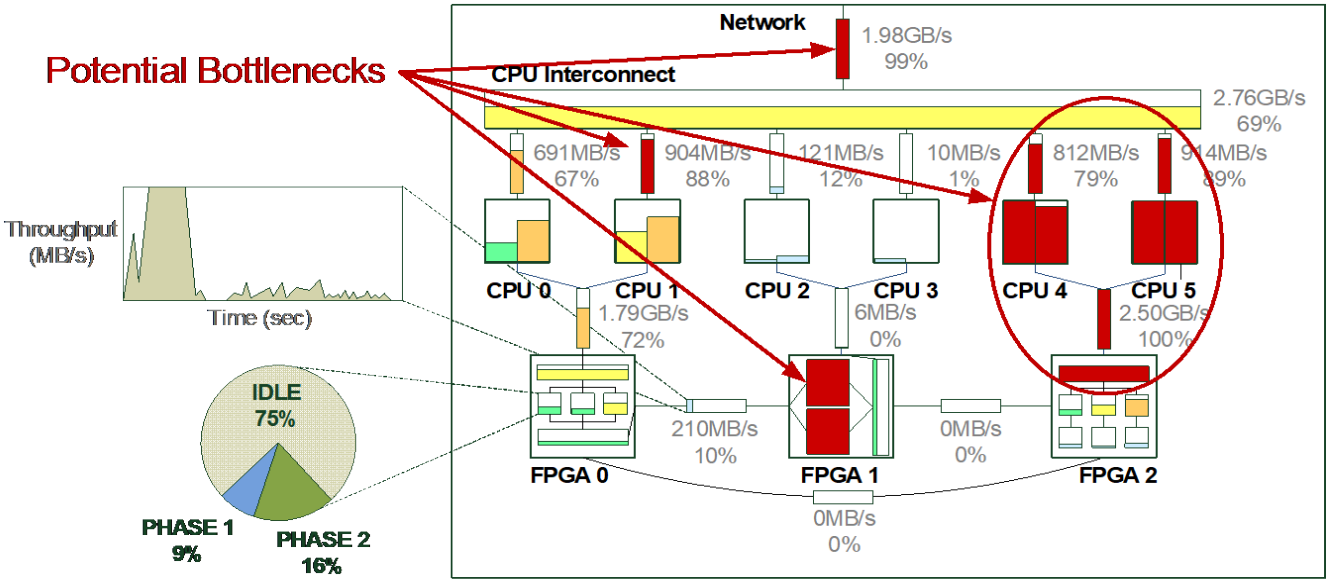
RCML Editor in Eclipse

Example: RC App Performance (ReCAP)

Productively identify & remedy bugs & bottlenecks in complex systems



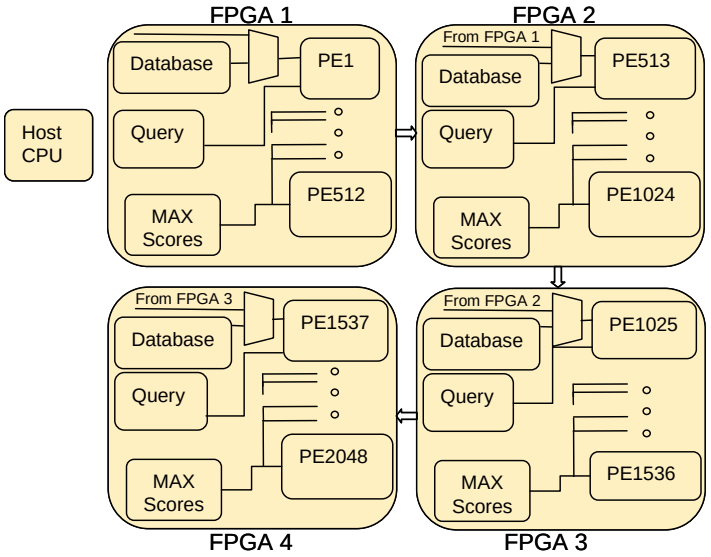




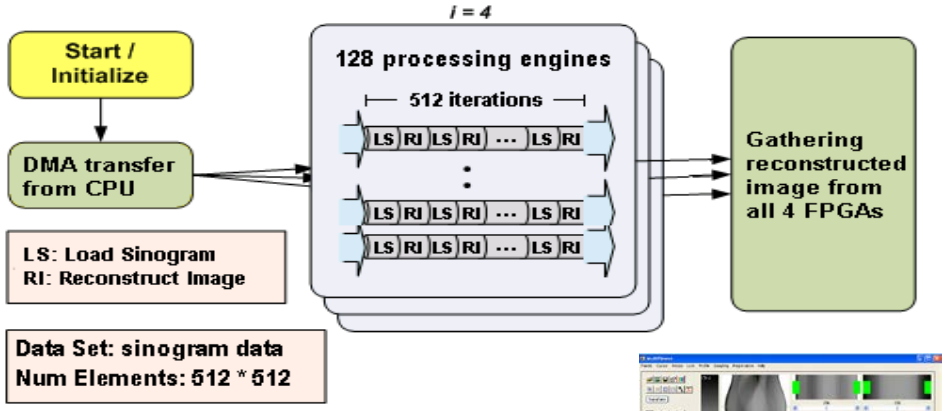
CHREC
NSF Center for High-Performance Reconfigurable Computing

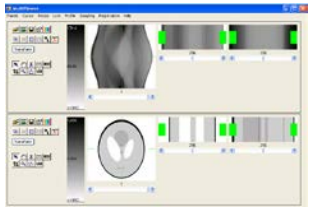
Novo-G Apps (in development)

- Bioinformatics (VHDL, Impulse-C)
  - Smith-Waterman (DNA sequence aligning)
  - VHDL: 512 PEs per FPGA, 125MHz
    - 2048 PEs streamed across board
    - Runs well on quad-FPGA board
      - FPGA vs. CPU-core speedup = ~700
      - Board vs. CPU-core speedup = ~2750
      - Novo-G vs. CPU-core speedup = ~65k est.
  - Impulse-C: working to fit similarly



- Image processing (VHDL)
  - Parallel-Beam Filtered Backprojection
    - Adapted VHDL code shared by U. Wash.
  - Implemented on quad-FPGA board
    - Early returns (tests still underway)
      - Board vs. CPU-core speedup = ~640
      - Novo-G vs. CPU-core speedup = ~15k est.





- Molecular dynamics (FPC)
  - Atomic particle trajectories
  - In design with Altera FP Compiler

Novo-G Future Plans

- Applications
  - Complete summer apps spanning all 96 FPGAs
  - Port selected apps from prior CHREC projects & systems
    - Hyperspectral imaging, 2D-PDF estimation, 3D-LIDAR processing, et al.
    - Previously running on our Nallatech cluster, Cray XD1 server, SRC-7 server, XD1000 server, DRC server, AlphaData cluster, etc.
- Tools
  - Complete port of CHREC tools suite to Novo-G
  - Engage with more tools vendors to support

- System
  - Expand machine size (we hope to double # of FPGAs by 1Q10)
    - Room to add second quad-FPGA board in each server
    - Explore options to directly connect two boards (bypass PCIe), and thereby stream apps across 8 powerful FPGAs

Conclusions

Conclusions

- Novo-G machine is now operational
  - Most powerful RC system ever fielded for R&D
    - Configured to support both **HPC** and **HPEC** experiments
      - Key issues, from satellites to supercomputers
    - Experiments spanning 1, 2, 3, 4, …, 96 powerful FPGAs
  - Target for many CHREC research projects
    - R&D on design, verification, optimization, scalability, productivity
- Resources available to all CHREC participants
  - Academia, industry, government
- Enabling technology for research breakthroughs
  - New theories, concepts, methods, tools, insight

Come Join Us in CHREC!

- For more info:

  www.chrec.org

  george@chrec.org

- Questions?