Using a FLASH Based FPGA in a Miniaturized Motion Control Chip

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Introduction

The Motion Control Chip (MCC) is a freestanding component that can control up to three brushed motors or one brush-less motor in torque, position or velocity mode.

Approximated dimensions (L,W,H) 75mm x 45mm x 10mm

Approximated weight 80g

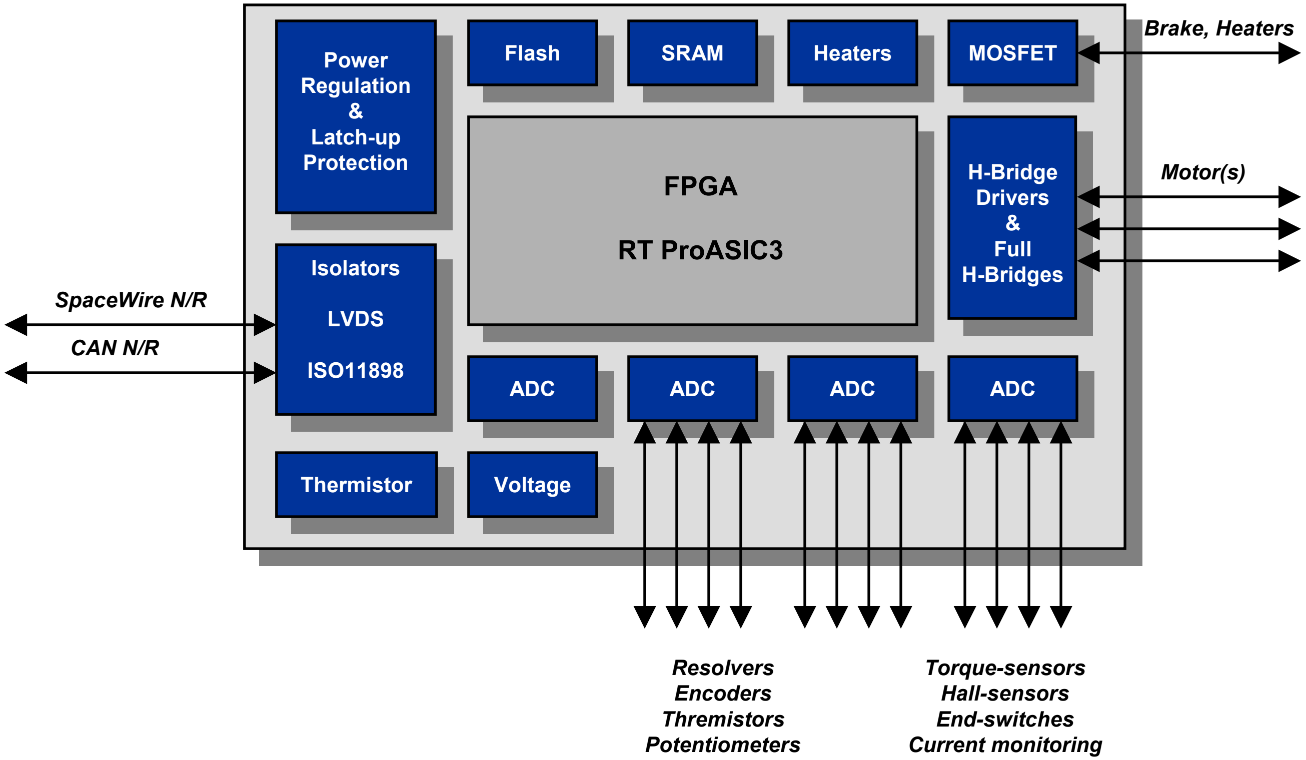
Potential applications are:

- Exoskeletons
- Robotic arms
- Drills
- Wheels and masts on rovers
- Solar panel positioning, etc.

All digital logic in an FPGA

Conceptual drawing of ESA's ExoMars rover

Motion Control Chip – block diagram

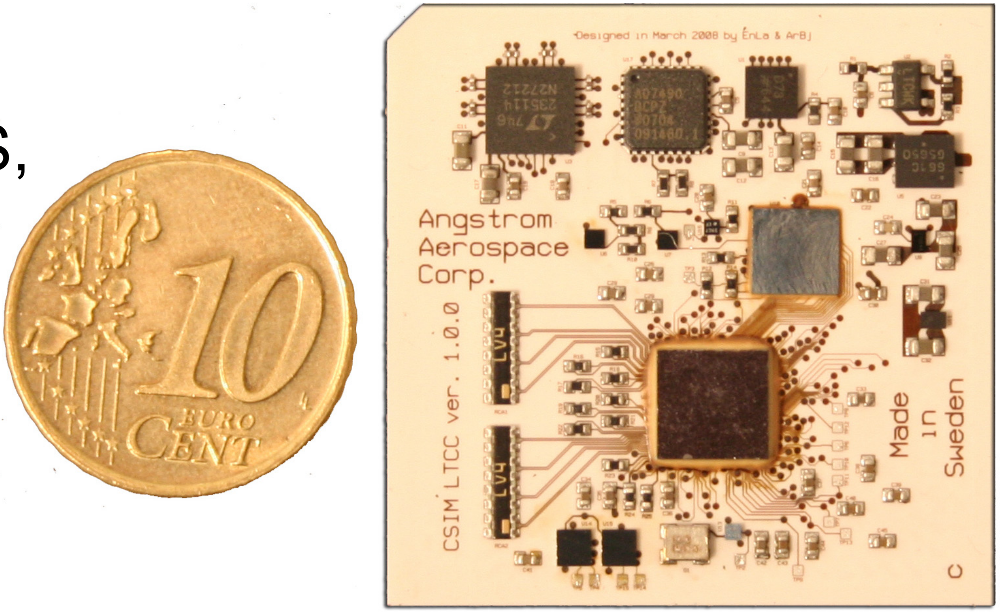


Miniaturization technology

The MCC design is based on ÅAC's proprietary packaging technology that offers high-resolution thin-film metallization on various substrates for advanced 3D-stacking.

The packaging technology allows advanced 3D-multi-chip-modules (3D-MCM) that can incorporate various kinds of naked die.

An example of previous designs is the RTU-100-CS, which is 34 mm x 34 mm and less than 2 mm in height, weighing 3 grams.

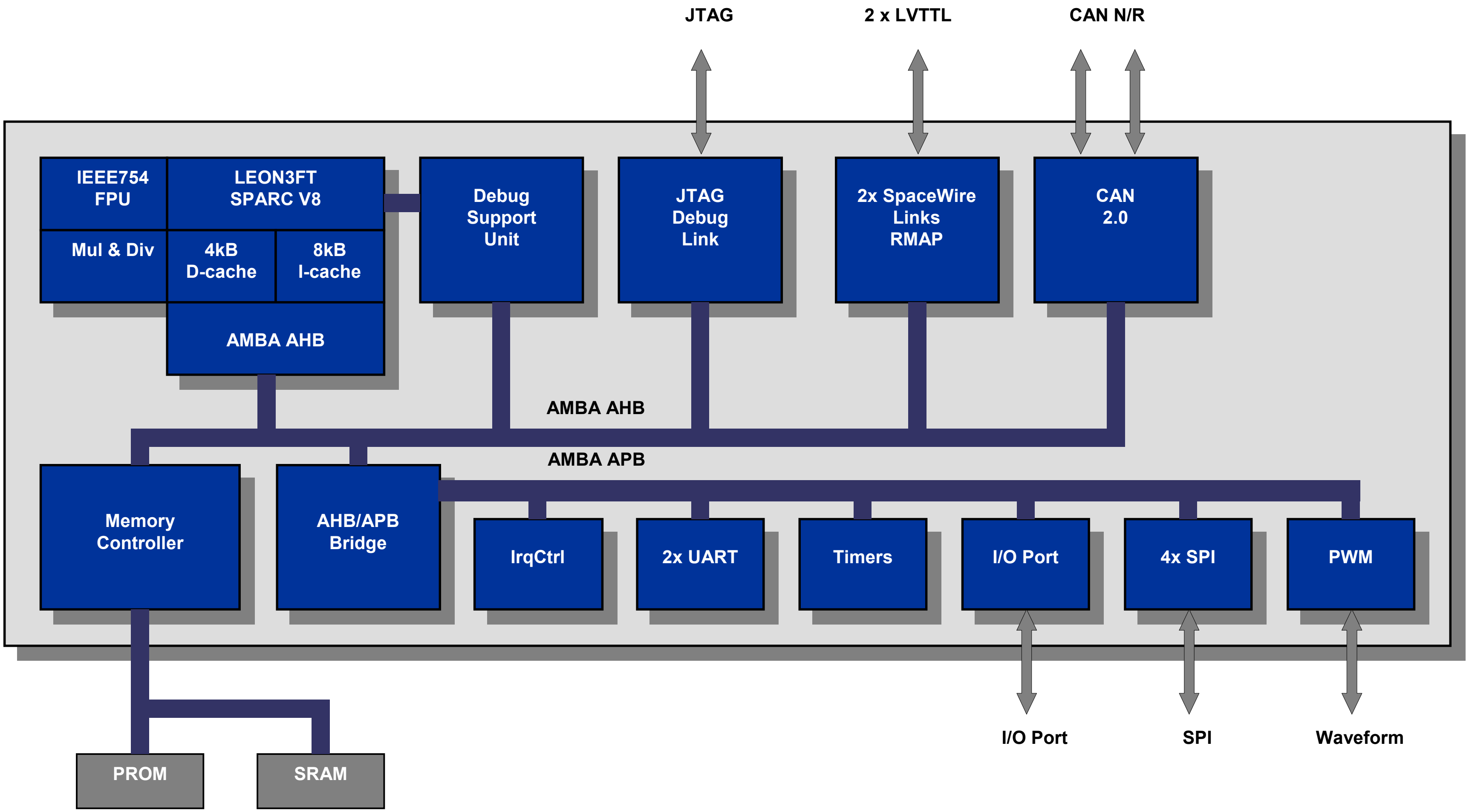


Remote Terminal Unit (RTU-100-CS)

Programmability

- The MCC concept is to provide a miniaturized system that is also programmable:
  - Main digital logic implemented in re-programmable Flash based FPGA (e.g. processor and interfaces)
  - Software stored in re-programmable Flash PROM
- Actel RT3PE3000L FPGA:
  - 3,000,000 System Gates
  - 75,264 Logic Tiles
  - 504 kbits RAM
  - 1 kbits FlashROM (user accessible)
- RT ProASIC3 devices use same silicon and process as commercial UMC 0.13 µm ProASIC3EL family
- RT3PE3000L uses the same silicon as the A3PE3000L

Motion Control Chip – FPGA



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LEON3 SPARC V8 Processor

- IEEE-1754 SPARC V8 compliant, 32-bit processor
- 7-stage pipeline, multi-processor support
- Separate multi-set caches with LRU/LRR/RND
- On-chip debug support unit with trace buffer
- Highly configurable:
  - Cache size 1-256 kByte, 1-4 sets, LRU/LRR/RND
  - Hardware Multiply/Divide/MAC options
  - MMU, FPU high-performance or small-size
  - Pipeline optimization for specific target technologies
  - Fault tolerance optimization for specific target technologies
- 400 MHz on ASIC (130 nm, 400 MIPS, 400 MFLOPS, 25 kgates)
- 20-30 MHz on Actel RTAX2000S FPGA
- 20-30 MHz on Actel RT ProASIC3 FPGA
- Certified SPARC V8 by SPARC International
- Suitable for space and military applications
- Baseline processor for space projects in US, Europe and Asia

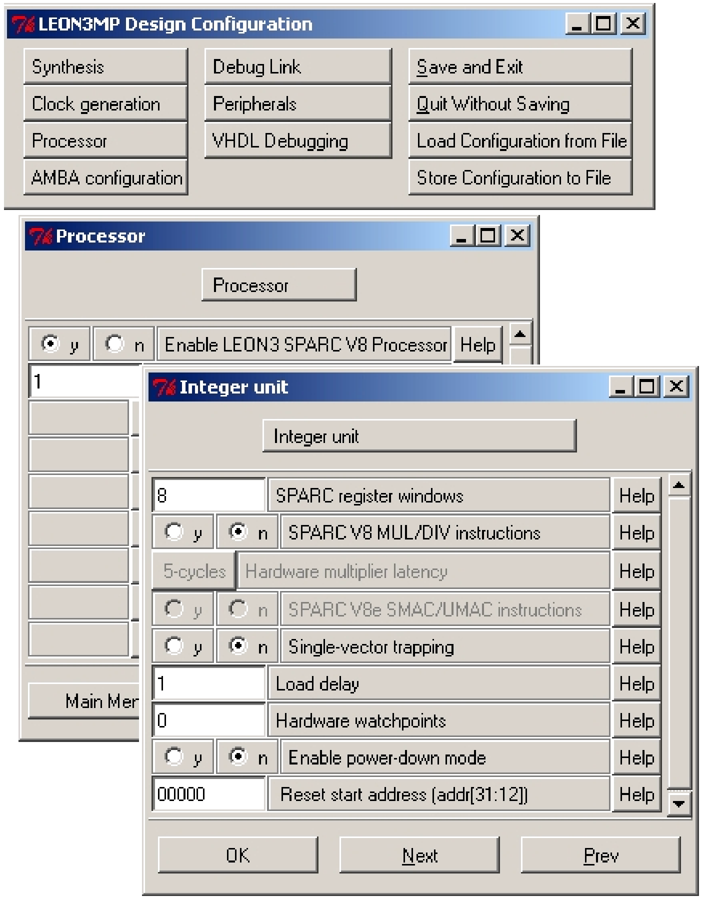
SPARC Compliant SCD V8

FPGA interfaces

- SpaceWire links with RMAP to support remote memory access for software download and debug, based on ECSS standards
- Selectively redundant CAN 2.0A/B bus interface, based on ISO and ECSS standards
- SPI interface for access to ADC devices, support for multiple accesses in parallel to allow correlations
- Pulse Width Modulation: symmetric and asymmetric
- General Purpose Input Output
- Memory Controller with EDAC to protect external Flash PROM and SRAM memory
- JTAG Debug Link, used for software download & debug

FPGA design using GRLIB IP library

- The FPGA design is based on GRLIB VHDL IP core library, which is a complete system-on-chip design environment available for end-user development:
  - Processors
  - Peripherals
  - Memory controllers
  - Serial and parallel high speed I/F
  - AMBA on-chip bus with Plug & Play
  - Fault tolerant and standard version
  - Support for tools & prototyping boards
  - Portability between technologies
- Can also integrate customer furnished IP cores
- Flexible licensing



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Radiation aspects

- Single event latch-up (SEL): > 96 MeV-cm^2/mg
- Single event upset (SEU):
  - Flash PROM memory: > 96 MeV-cm^2/mg
  - SRAM memory: 1 MeV-cm^2/mg
  - D-type flip-flop: 6 MeV-cm^2/mg
- Single-Event Transient (SET):
  - Clocks: 4 MeV-cm^2/mg
  - I/O banks: 7 MeV-cm^2/mg
- Mitigation:
  - Triple modular redundancy (TMR) on all flip-flops
  - Memory protection: EDAC, parity, etc.
  - I/O bank failure detection leading to reset
  - Watchdog leading to reset
- Total ionizing dose (TID): 20 krad
  - Radiation monitor based on ring oscillator (under consideration)

FPGA design results

- Synthesis and place&route results (RT3PE3000L -1):
  - Size: approximately 95% (with TMR and EDAC)
  - System frequency: 20 MHz
    (optimizations towards 25 MHz is ongoing)

- Performances:
  - CPU: 17 Dhrystone MIPS
  - FPU: 3 MFLOPS
  - SpaceWire: 20 Mbit/s (twice the requirement)
  - CAN: 1 Mbit/s
  - SPI: 10 Mbit/s
  - JTAG: 1 Mbit/s

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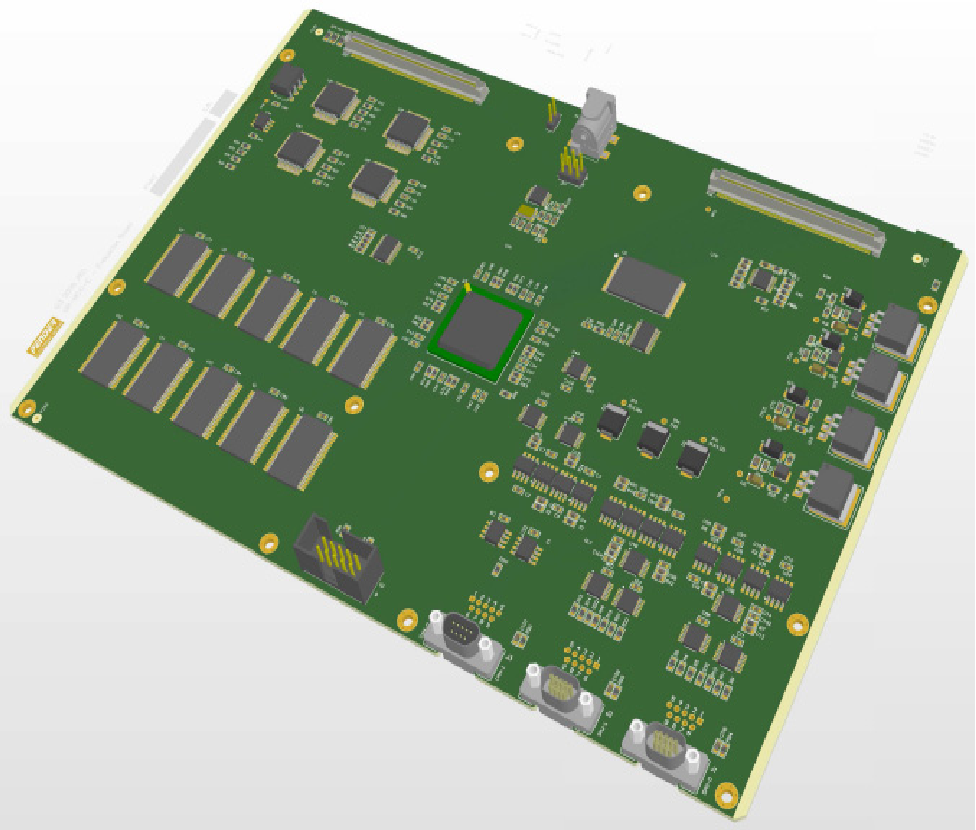
Prototype board – PCB version

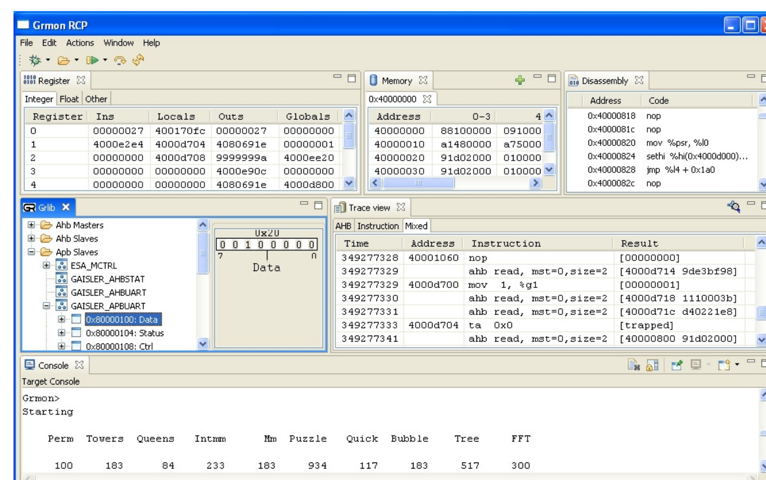
- Prototype MCC computer board (MCC-C), based on commercial grade components, contains:
  - A3PE3000L FPGA
  - SRAM memory
  - Flash PROM memory
  - Four ADC devices
  - LVDS I/F for SpaceWire
  - ISO11898 I/F for CAN
  - Power regulation
  - Connectors to interface analogue boards
  - MDM-9 connectors for SpaceWire & CAN (not on final MCC)



Software environment

- RTEMS real time operating system:
  - Version 4.10
  - Drivers for IP cores in FPGA:
    - SpaceWire or CAN controller
    - SPI (for ADC communication)
    - Memory controller
    - PWM, GPIO, etc.

- GRMON hardware debug monitor:
  - Supporting all kernels/compilers
  - Command line or GUI
  - GDB remote debug support
  - Connects to MCC via JTAG



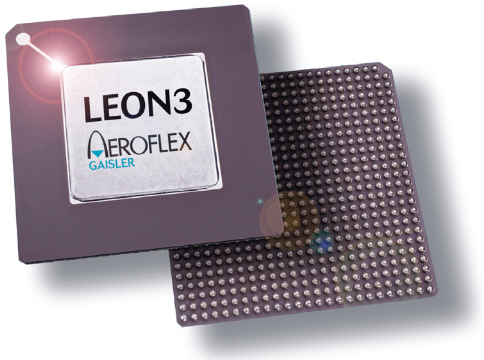
Status and follow-on

Status:

- MCC FPGA design ready for Critical Design Review (CDR)
- MCC PCB prototype computer board ready for production
- RTEMS drivers already being used with TSIM LEON3 simulator and in other projects

Follow-on activities:

- Based on the presented experience with the ProASIC3 technology, it seems feasible to move from anti-fuse technology to Flash based technology
- Investigating the possibility to offer existing LEON3FT-RTAX products also on RT ProASIC3 technology
- Preparing already now for the next generation Flash based FPGA technology



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Conclusions

- The re-programmable RT ProASIC3 FPGA technology fits well within applications with moderate radiation requirements.
- The in-situ programmability enables the development of highly miniaturized systems which can be adapted to customers needs late in the development cycle.
- Porting a LEON3-FT system from anti-fuse to Flash-based FPGA technology went smoothly, with much of the IP core library work already performed two years ago for the commercial version of the LEON3 processor.
- The authors acknowledge ESA for the commissioning and funding of the development of the MCC under ESA contract number 21737, lead by Dr Johan Köhler.

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General contact information

- LEON3 / GRLIB information:
  http://www.Aeroflex.com/Gaisler
- LEON3FT-RTAX-S data sheet and user manual:
  http://www.Aeroflex.com/Gaisler
- Motion Control Chip information:
  http://www.AACMicrotec.com/prod_3.htm
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