Over 3Gb/s Universal Lossless Compressor for Space Use

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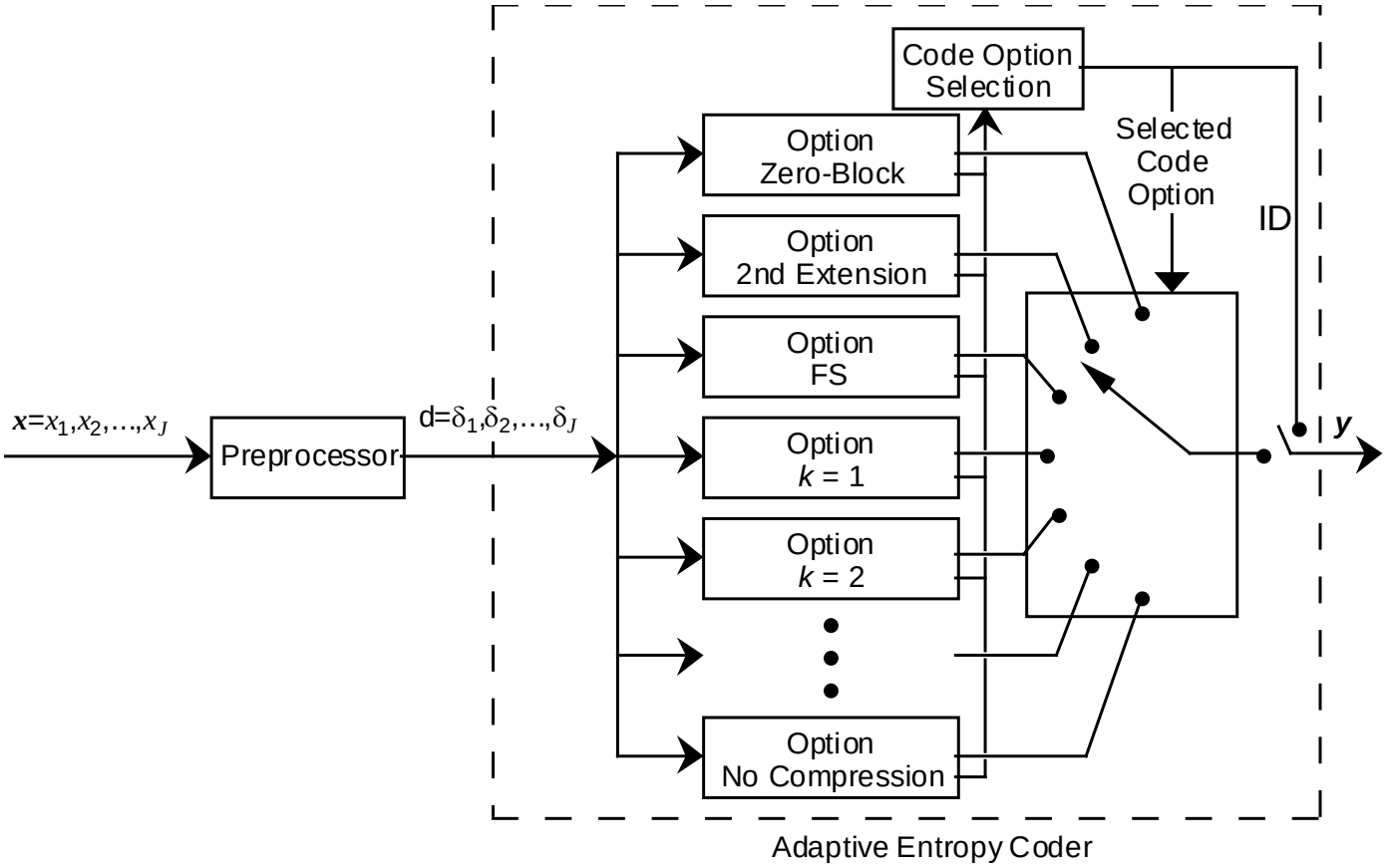
Outlines

- Universal Lossless Data Compression Algorithm for Space
  - What is it and its use in space
  - Algorithm and Available RH Chip
  - Previous RH Chip Limitations
- New Development
  - Features
  - Performance
- New Applications
- Conclusion

Universal Lossless Data Compression

- Algorithm: *CCSDS* 121B *Lossless Data Compression*, May 1997 Issue 1
  - A set of Huffman codes without code tables;
  - Best option selected based on actual coded length from each Huffman code;
  - Optimal for data with Geometric probability distribution (*e.g.* Laplacian), such as science instrument data after de-correlation
  - Applicable to 1D, 2D, 3D, …, data as it processes blocks of *J* samples for one optimal code option, thus *Universal*.

Algorithm Architecture



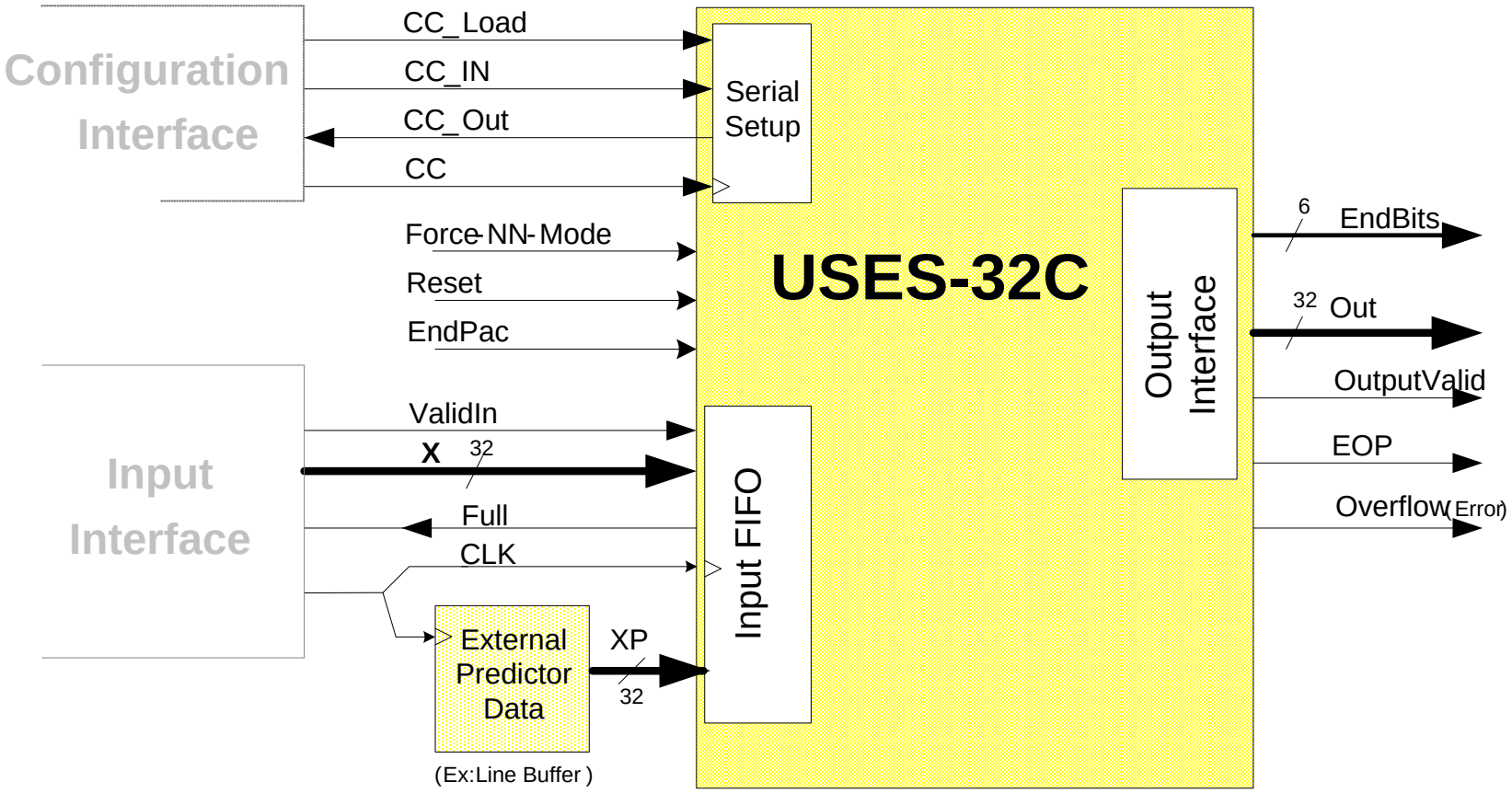
Space Applications

- *CCSDS* 121B applied over 25 missions on instruments from spectrometers, gamma-ray detectors, to various imagers, in both Hardware and Software forms.
- Rad-Hard chip, the *Universal Source Encoder for Space* (USES) developed in 90's in 1.2µ UTMC gate array:
  - 20 Msamples/sec, re-qualified to 33 Msamples/sec in 2010 for LDCM mission;
  - 0.1 watt/Msample/sec;
  - Flown on over 12 missions, LEO and planetary;
  - Limited to max 15-bit dynamic range input.

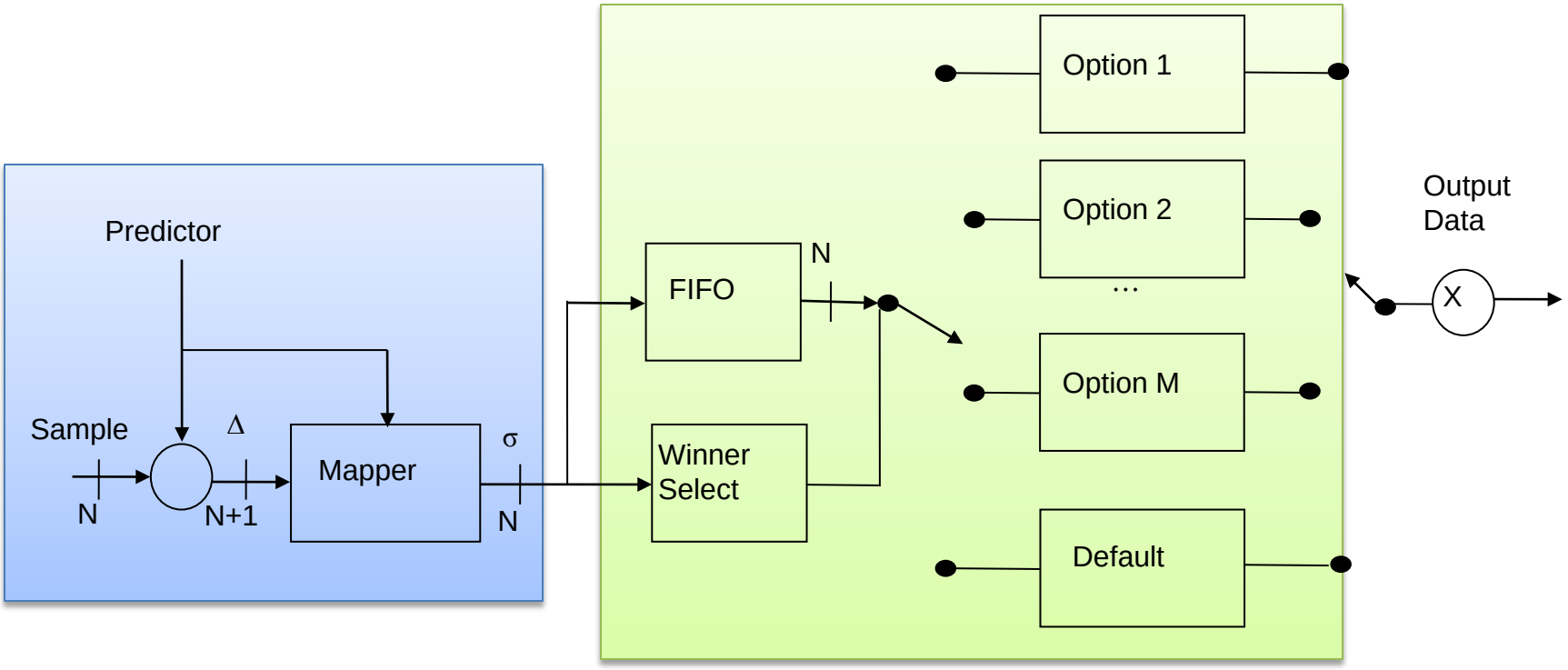
New Development: USES-32C

- Goals:
  - Achieve over 100 Msample/sec;
  - Allow up to 32-bit input data.
- Features:
  - Act as data packer when in bypass mode;
  - Allow input from 1-bit to 32-bit;
    - Improved performance for 1 ~ 4-bit data such as feature maps by allowing shorter code ID specified in upcoming Issue 2 of *CCSDS* 121B.
  - Supports 3 predictor modes: nearest, external, 2D.

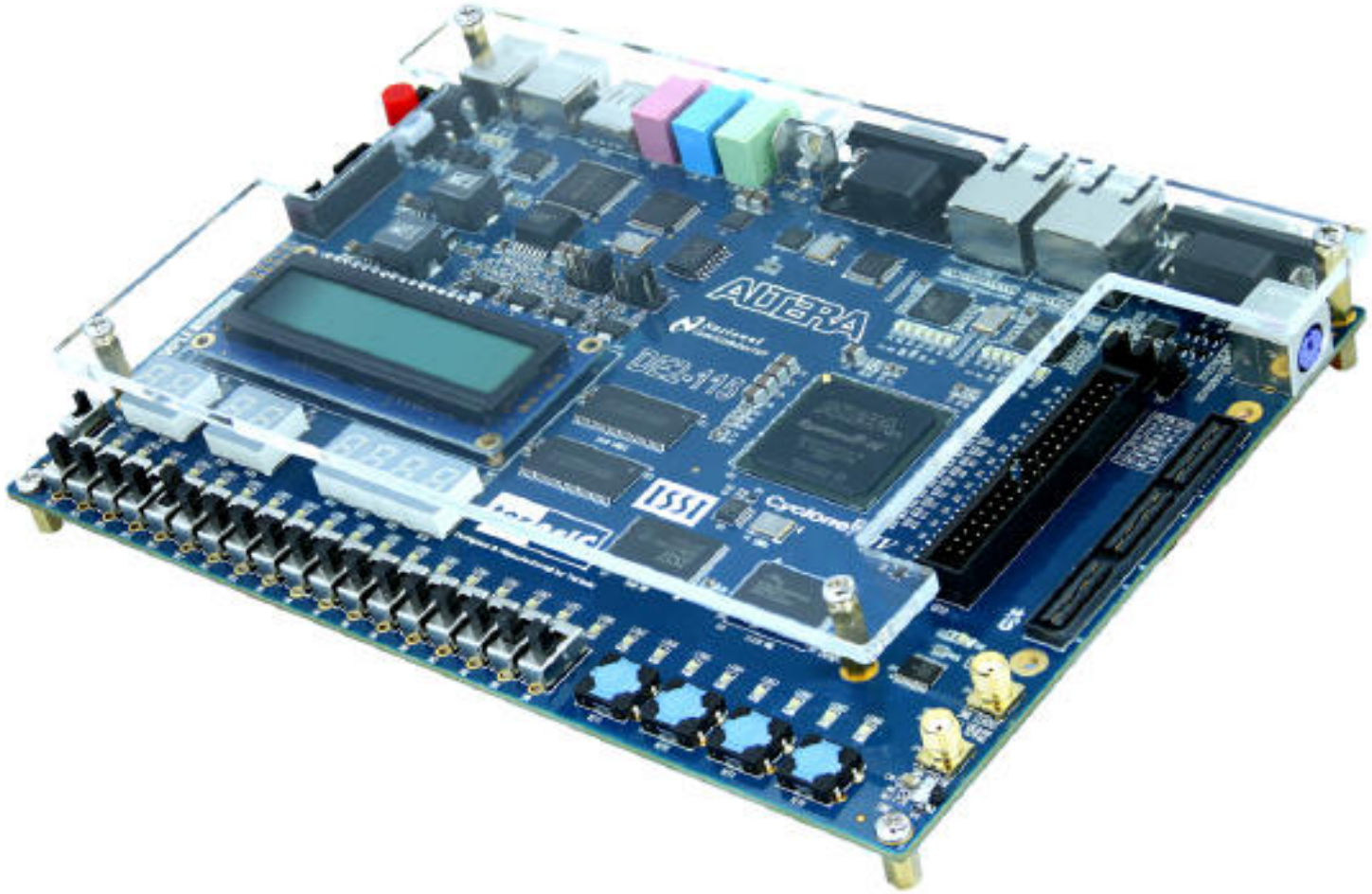
USES-32C I/O Signal



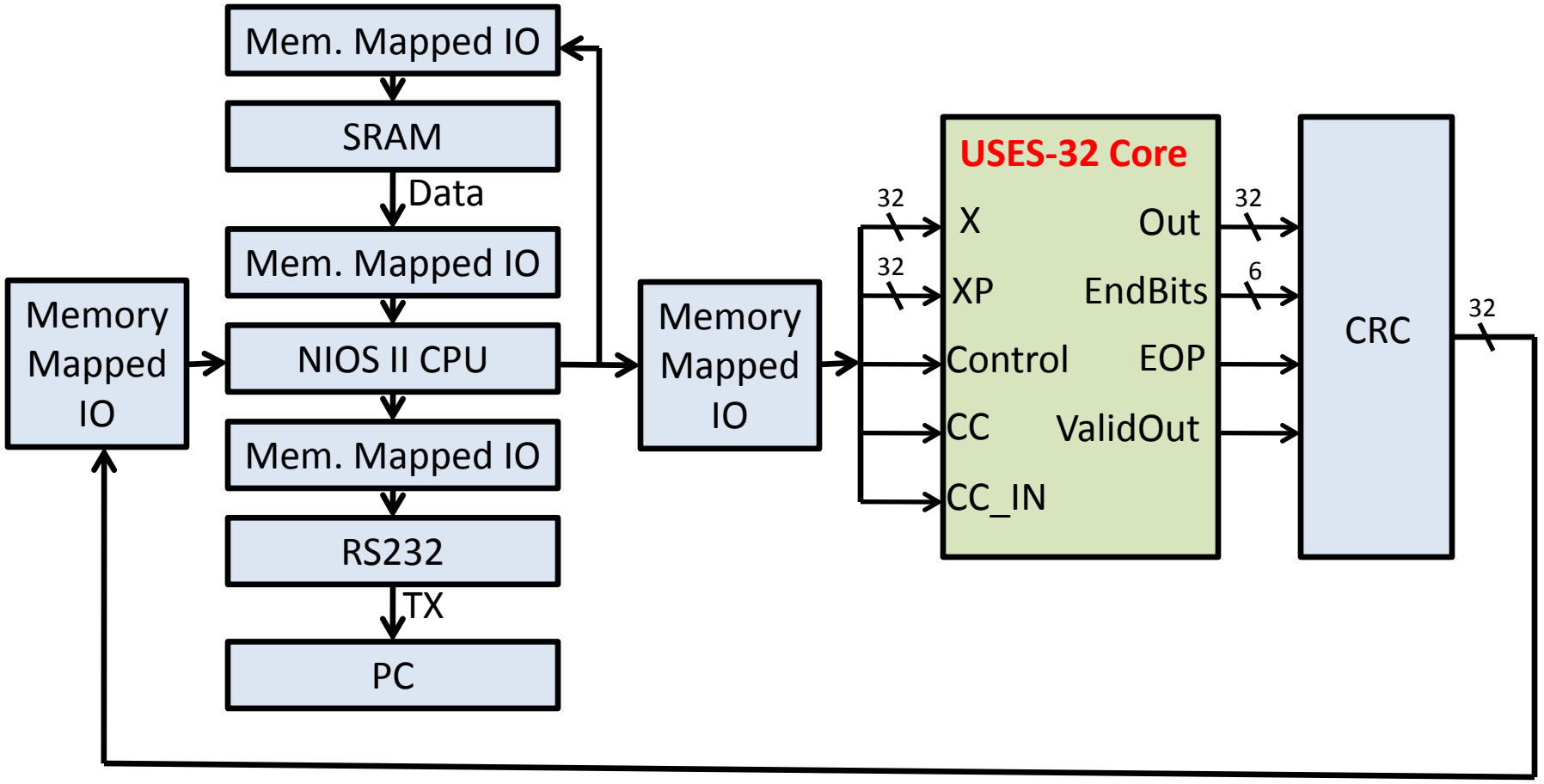
Major Processing Blocks



Terasic DE2-115 Altera Development Board



Testing Architecture



Test Procedures

- Images passed through USES-32 FPGA core
  - GSFC supplied images
  - Verified by comparison of CRC with software model
- Random testing on FPGA
  - Choose a random coding option for each block
  - Random number generated samples
  - Verified by comparison of CRC with software model
- Decoding of generated output to produce the original image

Performance

- Altera Cyclone IV E (EP4CE115F29C8)
  - Greater than 50Msamples/sec throughput
  - 13,603 logic elements (12%)
  - 6,393 registers (6%),
  - 213,632 memory bits (5%);
- Stratix III (EP3SE50F484C2):
  - 200 Msamples/sec throughput
  - 6,255 combinational ALUTs (16%)
  - 3,383 dedicated registers (9%)
  - 16,664 memory bits (<1%).

New Applications

- *CCSDS* 121B Entropy Coder specified in forthcoming *CCSDS* 123B *"Lossless Multipectral and Hyperspectral Image Compression"* recommendation, a state-of-the-art algorithm;
- The preprocessor in 123B uses a predictor based on adaptive filtering of up to 15 previous spectral band data;
- Including 123B preprocessor will enable USES-32C to be conformant to 2 *CCSDS* standards: 121B and 123B
  - Seeking funding opportunity

Conclusion

- A 32-bit *CCSDS* 121B standard Entropy Coder has been implemented and tested.
- Performance, pin count, and resource requirements have been improved over the original implementation architecture

Thank You

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