

Sentinel-2 MMFU

The first European Mass Memory System based on NAND-Flash Storage Technology

M. Staehle, M. Cassel, U. Lonsdorfer - Astrium GmbH - Processing and Platform Products
F. Gliem, D. Walter, T. Fichna - IDA TU Braunschweig

ReSpace/MAPLD 2011

August 22th - 25th
Albuquerque, USA

Presenter: Dr. M. Cassel - Astrium GmbH

All the space you need



Introduction

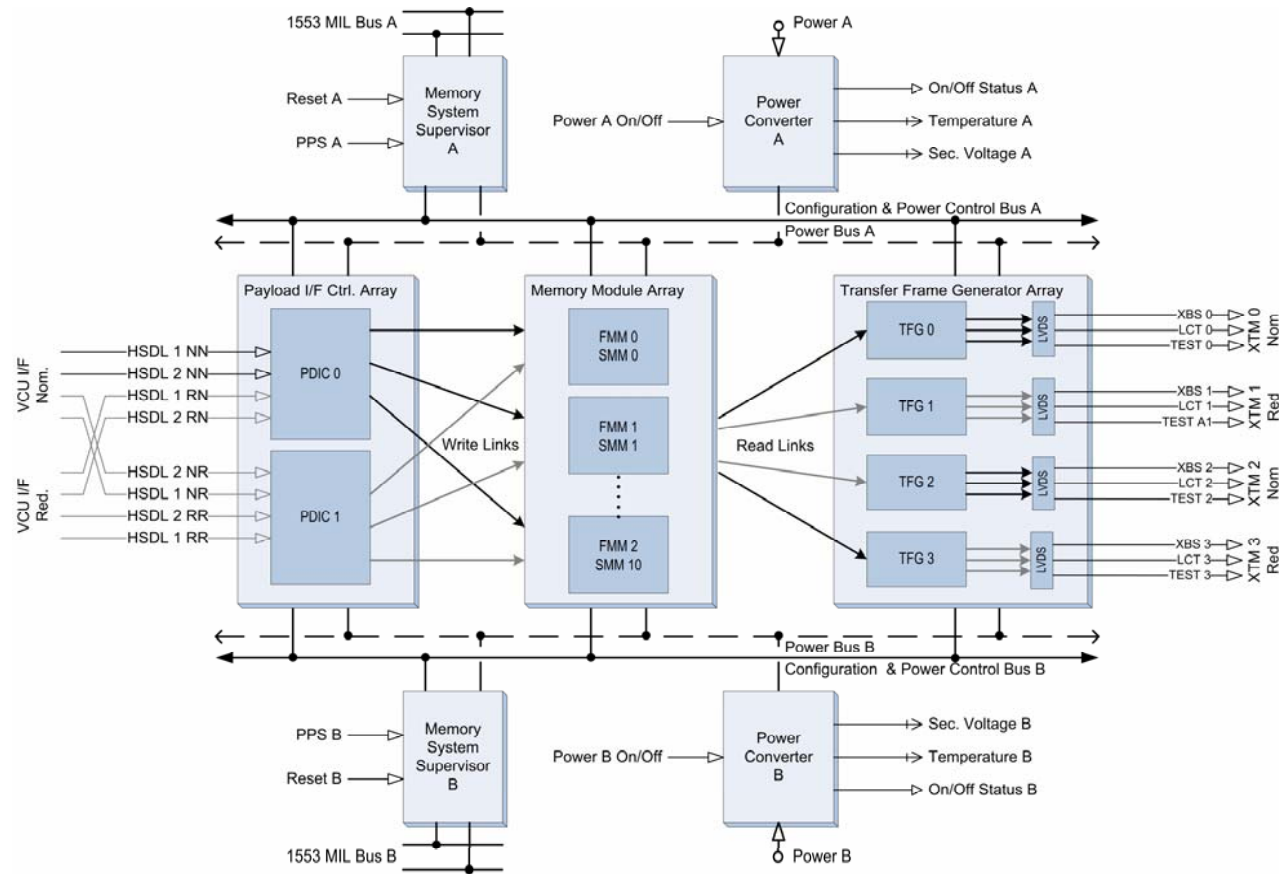
- For over 15 years the DRAM (Dynamic Random Access Memory) technology family represents the conventional semiconductor storage technology for mass memory systems in space applications.
- Now a strong competitor has arisen with the Single Level Cell (SLC) NAND-Flash memory technology, which have been introduced for space applications by Astrium. The first European application is the Sentinel-2 MMFU (Mass Memory and Formatting Unit). Sentinel-2 is the multispectral optical mission of the EU-ESA GMES programme, currently under development by Astrium in Friedrichshafen (Germany) scheduled for launch in 2013.
- The required storage capacity of 2.4 Tbit motivated the selection of the NAND-Flash technology which was already secured by a lengthy period (2004-2009) of detailed testing, analysis and qualification by Astrium, IDA and ESTEC.

This document is the property of Astrium. It shall not be communicated to third parties without prior written agreement. Its content shall not be disclosed.

NAND-Flash Characteristics and Fundamental Work

- The main advantages of the NAND-Flash technology are
 - i. the non-volatile data storage capability and
 - ii. the substantially higher storage density.
- Their main disadvantages, at a first glance, are
 - a) the lower write rate compared to SDR-SDRAM or DDR-SDRAM (Single or Double Data Rate Synchronous DRAM),
 - b) the access to larger data portions (pages) of 4 Kbyte per device,
 - c) the fact that data cannot be modified in place, and
 - d) the wear out limitations of 10^5 write operations per page.
- Astrium and IDA have continuously worked for over seven years on the subject “NAND-Flash Technology for Space”.
- As a result of this extensive radiation testing performed by Astrium and IDA, the radiation effects on these memory devices are well known now and appropriate error handling mechanisms have been developed.
- For the Sentinel-2 mission, a complete qualification program of the NAND-Flash has been performed.

S2 MMFU Requirements and Implementations (1)



Simplified S2 MMFU Architecture

This document is the property of Astrium. It shall not be communicated to third parties without prior written agreement. Its content shall not be disclosed.

S2 MMFU Requirements and Implementations (2)

Parameter	Requirement	Astrium MMFU	
		NAND-Flash	SDR-SDRAM
User Storage Capacity	2.4 Tbit (EoL)	6 Tbit (BoL)	2.8 Tbit (BoL)
Count of Memory Modules	-	3	11
Mass	≤ 29 kg	< 15 kg	< 27 kg
Max. Volume (L x H x W)	710 x 260 x 310 mm ³	345 x 240 x 302 mm ³	598 x 240 x 302 mm ³
Power (Record & Replay)	≤ 130 W	< 54 W	< 126 W
Power (Data Retention)	-	< 29 W (0 W)	< 108 W
Input Data Rate	2 x 540 Mbit/s + HK		
Output Data Rate	2 x 280 Mbit/s		
Life Time in Orbit	up to 12.5 years		
Reliability	≥ 0.98	0.988	> 0.98
Bit Error Rate (GCR) per Day	$\leq 9 \times 10^{-13}$ / day	5.9×10^{-14} / day	$< 9 \times 10^{-13}$ / day

S2 MMFU Requirements and resulting Implementations

S2 MMFU Requirements and Implementations (3)

Function	MMFU with NAND-Flash		MMFU with SDR-SDRAM	
	Modules (Functions)	Boards (Physical Assembly)	Modules (Functions)	Boards (Physical Assembly)
Memory System Supervisor	2	2	2	2
Payload Data Interface Controller	2	1	2	1
Memory Modules	3	3	11	11
Transfer Frame Generators	4	2	4	2
Power Converters	2	2	2	2
Total No. of Boards		10		18

Number of Functions and Boards

Discussion of Requirements (1)

■ Storage Capacity

- Astrium uses for all boards a standard format.
- Maximum number of memory and other EEE devices is limited by this form factor.
- Flash and SDRAM memory modules are identical in form, fit and function and can be mutually replaced.
- NAND-Flash device: TSOP1; 32 Gbit → **2 Tbit per module**
SDRAM device: Stack (3D Plus); 4 Gbit → **256 Gbit per module**
- The number of FMM modules (3) is determined by the total data rate and the operational concept. There are two memory modules operated in parallel. A third one is provided for redundancy.
- The number of SMM modules (11) is mainly determined by the required capacity. Also here two modules are operated in parallel and one SMM is included for reliability reasons.
- **Storage Capacity (BoL):**
 - **Flash based MMFU: 6 Tbit**
 - **SDRAM based MMFU: 2.8 Tbit**

Discussion of Requirements (2)

■ Mass and Volume

- Mass is always a critical issue for space missions which can be reduced by using NAND-Flash technology.
- The much higher storage density of the NAND-Flash devices (factor of 8) leads to a massive reduction in the number of required memory modules.
- **In case of the Sentinel-2 MMFU indeed 14 kg (about 50%) can be saved.**
- Further positive aspects evolve with reduction of the number of modules:
 - The system design from electrical and mechanical point of view is greatly relaxed.
 - Also the complete system design on satellite level, in terms of mass, power, thermal and other aspects, can be positively influenced by applying NAND-Flash based memory systems.

Discussion of Requirements (3)

■ Power

- The power consumption is reduced **by more than 50%**. This is mainly caused by the number of memory modules operated in parallel.
- Reasons are
 - Flash:
 - *There are only two active memory modules*
 - *No Scrubbing, no Refresh for data retention*
 - *Modules not in use can be switched off due to non-volatility*
 - SDRAM:
 - *Up to ten memory modules are operated in parallel.*
 - *Scrubbing and Refresh necessary for data retention*

Discussion of Requirements (4)

■ Data Rates

■ Device Characteristics

Performance Data	SLC NAND-Flash	SDR-SDRAM
Max. Write Performance @ IO clock	< 40 Mbit/s @ 40 MHz on page level (4K x 8)	< 800 Mbit/s @ 100 MHz burst operation
Max. Read Performance @ IO clock	< 250 Mbit/s @ 40 MHz on page level (4K x 8)	< 800 Mbit/s @ 100 MHz burst operation
Erase Time	2 ms on block level (256K x 8)	Not applicable

- Flash is slower due to erase time, programming time, lower working frequency.
- Lack in write performance can be mitigated by two measures.
 - parallel operation of Flash devices
 - interleaved access to several NAND-Flash devices (Interleaving uses the programming time of a NAND-Flash device to write in parallel to the next device)

Discussion of Requirements (5)

■ Lifetime and Reliability

- NAND-Flash devices provide a limited endurance.
This is caused by an inherent wear out mechanism of the Flash memory cells which limits the number of erase and write cycles to about 10^5 cycles.
- To mitigate the endurance limitation two measures can be applied:
 - Wear leveling (Address management system which distributes the write accesses rather uniformly over the address space)
 - Implementation of more storage capacity (easily possible due to the high storage density of Flash)
- A worst case analysis showed that for Sentinel-2 no measure is necessary. However wear leveling is implemented for several other reasons.
 - It avoids the development of "hot" regions during on-ground testing.
 - Maximum margin from endurance point of view can be achieved.
 - The mission times can be exceeded far beyond planned duration.
So the limited endurance is never a bottleneck for the lifetime of a mission.
 - It allows statistics in conjunction with the erase count.
NAND-Flash technology represents a rather new technology for space applications.

Discussion of Requirements (6)

■ Radiation and Error Rates

- With respect to TID sensitivity SDRAM and NAND-Flash devices behave quite similar (50 – 100 Krad).
- Single Event Effects (SEE):
 - MCE: Memory Cell Errors may occur all the time (SEU)
 - SEFI: Controller Errors may occur, if device is powered
 - SEL: Very unlikely, but has to be considered
- Probability of occurrence depends on operation.
Non-volatility of NAND-Flash devices offers specific advantages.
- **Flash can be switched off; hence SEFI rate can be reduced.**
- **SEFI and SEL errors can be removed with Flash without loss of data by reset and / or power cycling.**
- NAND-Flash devices provide an improved data immunity in case of SEFI and SEL occurrences. This is especially true for missions with short data transmission periods and comparatively long storage periods.

Conclusion

- The MMFU based on NAND-Flash shows clear advantages in comparison to SDRAM based systems and fits well to the high storage capacity and moderate data rates of the Sentinel-2 mission.
- The very high storage density of the NAND-Flash devices leads to a reduced number of memory modules with advantages in terms of power consumption, mass and volume.
- Non-volatility improves reliability and eases system design from mechanical and electrical points of view.
- The typical disadvantages of NAND-Flash are mitigated or even completely handled by an adequate system design and therefore are of no consequence for this mission profile.
- The radiation behavior of NAND-Flash devices provides advantages due to their inherent non-volatility which can be used to remove SEFI effects without data loss.
- A mass memory system using the NAND-Flash technology provides attractive features which have to be considered for current and next future satellite missions.