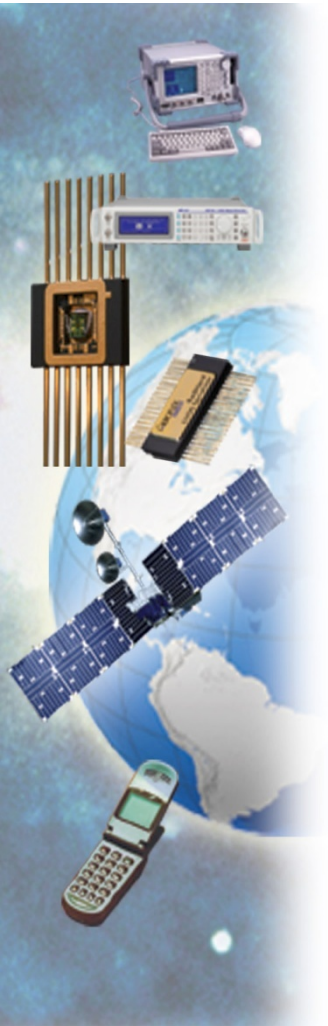

Aeroflex 16Mb / 64Mb MRAM Development Status

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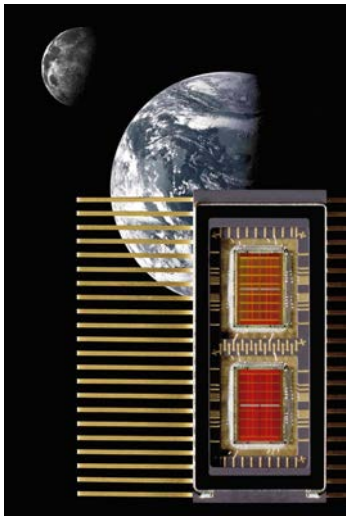

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Agenda

- Aeroflex Radiation Testing on 16Mb Commercial MRAM
- Aeroflex 16Mb MRAM Status
- Aeroflex 64Mb MRAM MCM Status
  - 64 lead, MCM package
  - MRAM evaluation board
  - Xilinx XQR4V / XQR5V Configuration Interface

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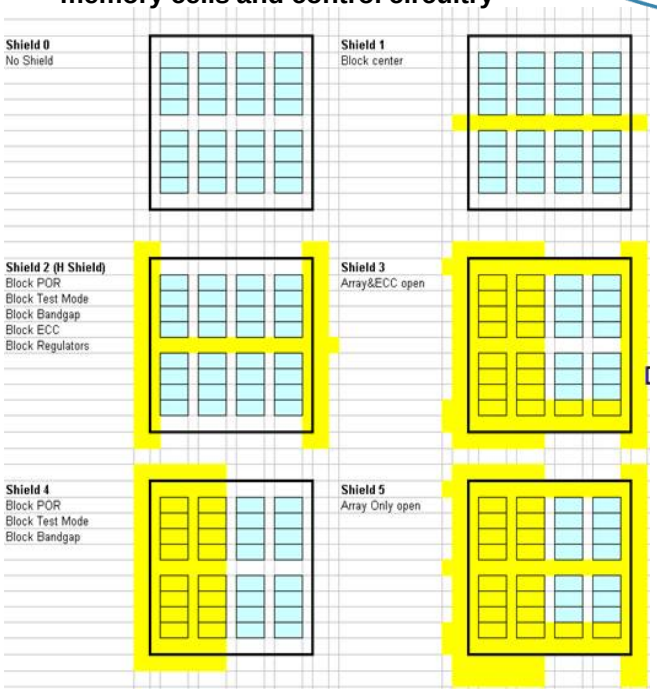
Hardening Approach for 16M MRAM

- Aeroflex performed testing of commercial 16M MRAM for Radiation Susceptibility
  - Heavy Ion testing at TAMU, TID testing at Aeroflex
- SEE sensitivity evaluated with shields (shown in yellow) to isolate critical circuits
- TID evaluated with test lot and Aeroflex "hardened by process" proprietary techniques
- Custom design rules generated to guide redesign and layout efforts

Shields used to evaluate SEE in memory cells and control circuitry



Operating Environment	Test Results
Single Event Latch-Up (SEL) Immunity	<17.4MeV-cm^2/mg
Single Event Upset LET (SEU)	≥ 100MeV-cm^2/mg
Total Ionizing Dose (TID)	≥ 70k Rad(Si)

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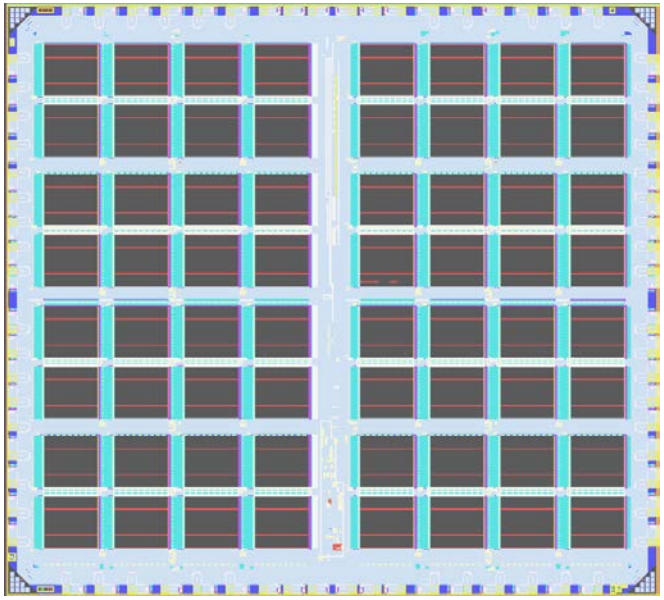
16Mb Design Mitigation – 100% Complete

- 2M x 8bit organization
- 45ns read/write cycle time
- Single 3.3V supply
- 40 lead DIP package, 25mil pitch
- Schedule Milestones:

Availability	Schedule
Prototype OOE (Commercial die)	June, 2011
Aeroflex rad-tolerant design tape-out	Aug, 2011
Prototype OOE (Rad-tolerant die)	Feb, 2012
Production OOE	Aug, 2012
QML Q	Oct, 2012
QML V	Dec, 2012



Operating Environment	Design Target
Single Event Latch-Up (SEL) Immunity	>80MeV-cm^2/mg
Single Event Upset LET (SEU)	≥ 100MeV-cm^2/mg
Total Ionizing Dose (TID)	≥ 100k Rad(Si)

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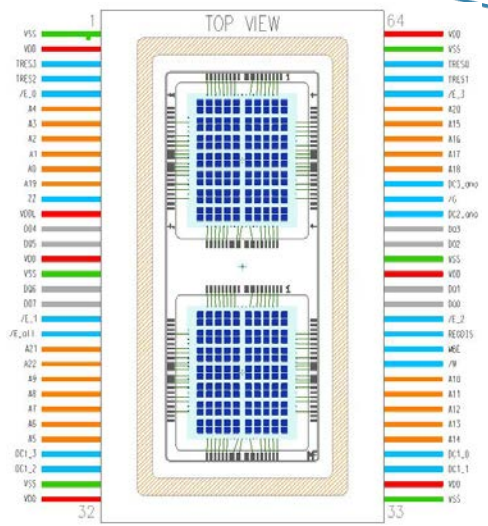
64Mb MCM Development

Task	Schedule
Package requirements definition for support of Xilinx V-4, V-5 FPGAs	Complete
Package pin assignments / outline definition	Complete
Package layout / routing / simulation (multiple passes)	Complete
Engineering Review / PDR (multiple passes)	Complete
Resolve PDR issues (multiple passes)	Complete
Final Package layout / routing / simulation	Complete
CDR layout / routing	Complete
Signal integrity analysis	Complete
Power analysis	Complete
Thermal analysis	Complete
Final Documentation / purchase req.	Complete (8/1/11)
Manufacturing: packages in-house	10/31/11
Package qualification	11/30/11



Availability	Schedule
Prototype OOE (Commercial die)	Dec, 2011
Prototype OOE (Rad-tolerant die)	March, 2012
Production OOE	Oct, 2012
QML Q	Nov, 2012
QML V	Feb, 2013

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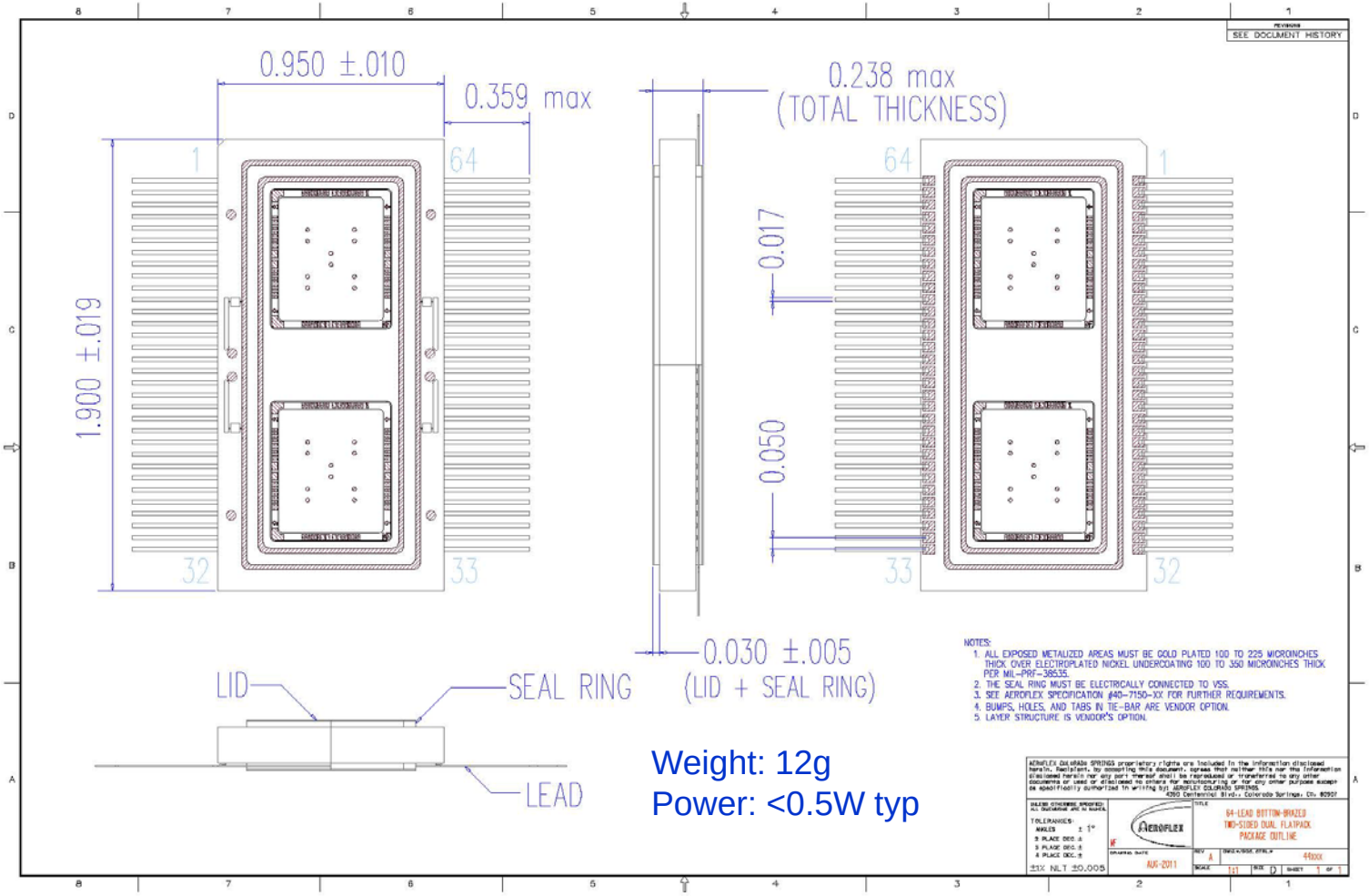
64 lead MCM Package Complete



Weight: 12g
Power: <0.5W typ

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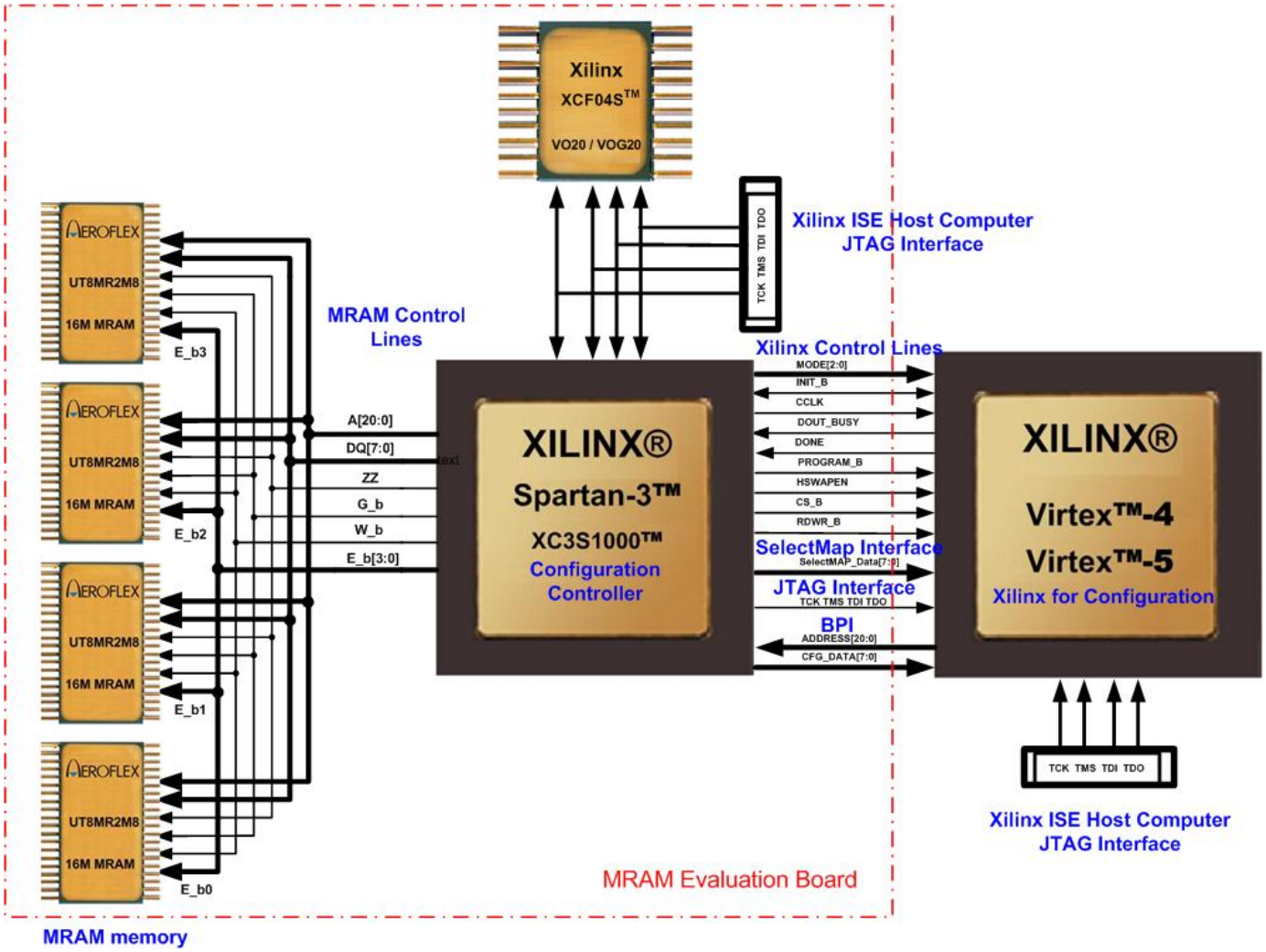
MRAM Evaluation Board Complete

- **Notional Diagram: Evaluation Board Interface to Xilinx XQR4V, XQR5V**



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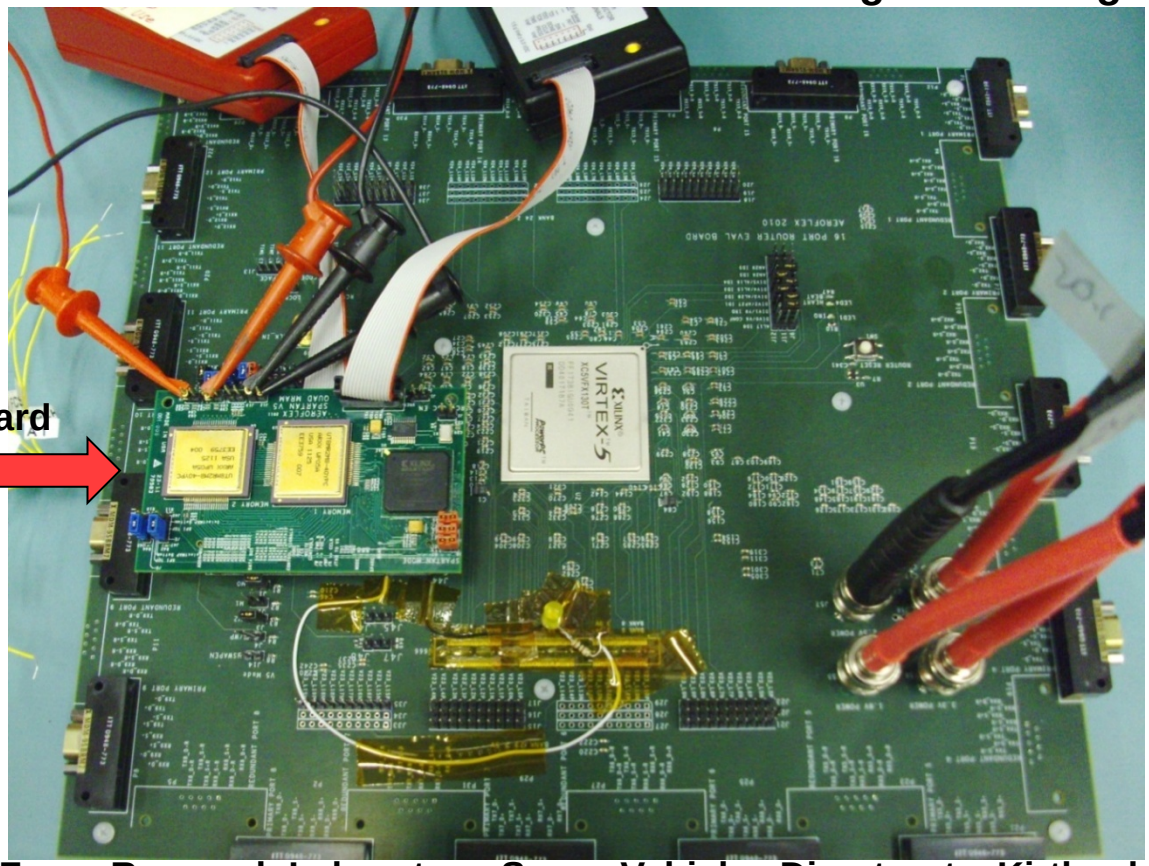
MRAM Evaluation Board

- MRAM evaluation board designed, manufactured and assembled
- MRAM board connects as mezzanine card through 75x2 pin connector to 16 port SpaceWire Router board
- SpaceWire Router board contains XC5V FX130T as configuration target

MRAM Evaluation Board



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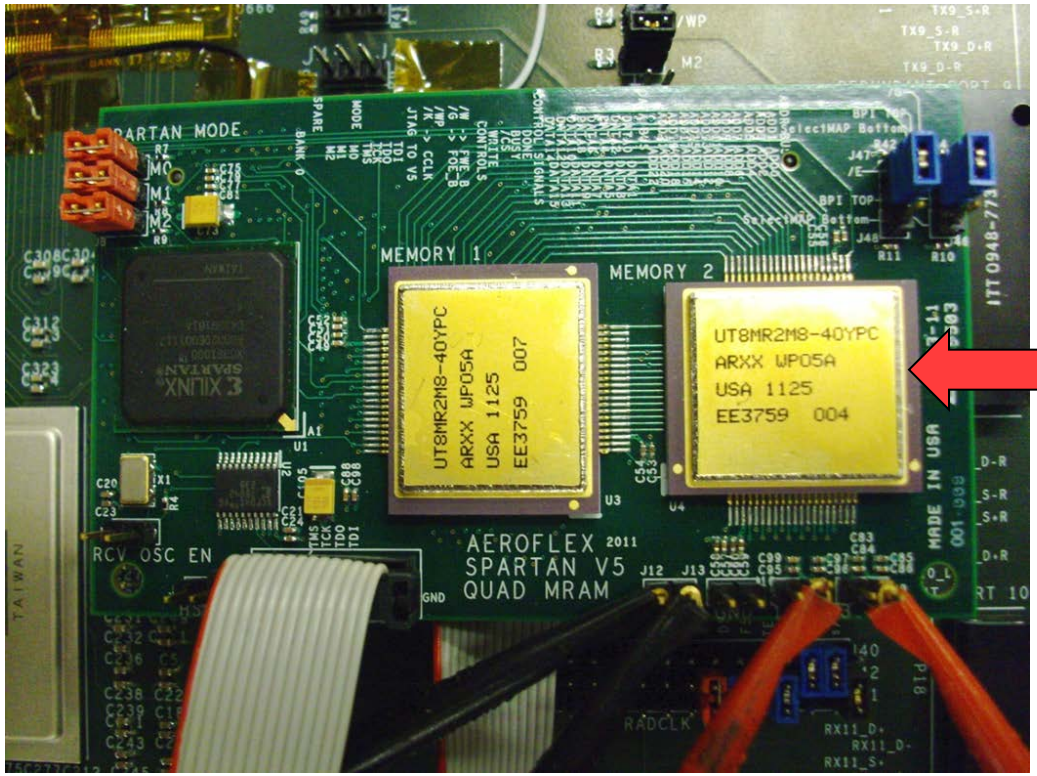
Proof of Concept: XQR4V / XQR5V Configuration

- Developed by Aeroflex Colorado Springs
- Initial Proof of Concept supports:
  - MRAM write / read: Evaluation board appears as XCF128X Flash PROM
  - Xilinx XQR5V: Configuration boot through 8 bit Master BPI-Up



MRAM die in 40 lead package

Dual sided: 2 die up, 2 die down

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Configuration Solution for Xilinx XQR4V / XQR5V

- Final configuration solution supports:
  - MRAM write / read
  - Xilinx XQR4V, XQR5V configuration boot
- Supported configuration modes
  - Master 8 bit BPI Up / Down
  - Single device Master / Slave SelectMAP (8 bit)
  - JTAG
- Configuration solution provided in single MCM package
  - 64Mb MRAM will appear as XCF128X Platform Flash PROM

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Summary

- Aeroflex performed extensive radiation testing to baseline the operating environment of the commercial 16Mb MRAM
- Aeroflex completed the redesign of the radiation tolerant 16Mb in August, 2011
  - Commercial prototypes available: June, 2011
  - Radiation tolerant prototypes available: Feb, 2012
- 64 lead MCM package design complete with initial package delivery in October, 2011
  - Prototypes available: Dec, 2011
  - Single component solution for configuration load
- Design, layout, manufacture and assembly of MRAM evaluation board complete using 4, 16Mb MRAMs and Xilinx Spartan-3
  - Proof of concept for configuration load
  - MRAM write / read as XCF128X Flash PROM verified
  - Configuration using 8 bit BPI Up mode and Xilinx XCFX130 FPGA verified