Radiation Testing of Aurora Protocol with FPGA MGTs

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Overview

- Introduction
- FPGA Multi-Gigabit Transceiver (MGT) Overview
- Radiation Test Motivation
- Aurora Protocol Overview
- Test Setup
- Test Results
- Conclusions
Introduction

- FPGA Multi-Gigabit Transceivers (MGTs) are used to transmit data serially to/from FPGAs
- MGTs are susceptible to SEUs resulting in
  - Data loss
  - Reduced bandwidth
- **GOAL**: Determine if the addition of a protocol can help mitigate known MGT SEU issues
SEUs in the Configuration Memory

- SRAM-based FPGAs are sensitive to radiation
  - Logic and routing sensitive to SEUs – not just memories
  - Soft fault that acts like a hard fault (until reconfigured) → firm fault

- In an SRAM-based FPGA, most SEUs happen in the Configuration memory

<table>
<thead>
<tr>
<th>Xilinx Virtex4 FX60 Device</th>
<th>Configuration Bits</th>
<th>17,004,288</th>
<th>79.8%</th>
</tr>
</thead>
<tbody>
<tr>
<td>User BlockRAM Bits</td>
<td>4,276,224</td>
<td>20.0%</td>
<td></td>
</tr>
<tr>
<td>User Flip-Flops</td>
<td>50,560</td>
<td>0.2%</td>
<td></td>
</tr>
</tbody>
</table>
SEU effects in MGTs

- Previous MGT SEU work has been done
  - Morgan – Aurora with commercial V5
    - Upset-Induced Failure Signatures, Recovery Methods, and Mitigation Techniques in a High-Speed Serial Data Link for Space Applications – NSREC 2008
  - Monreal – 5QV MGT characterization
    - Radiation Test Report, Single Event Effects, Virtex-5Qv Field Programmable Gate Array, Multi-Gigabit Transceivers - 2011
  - Characterized failure rates and failure mechanisms

![Table 1](image-url)
SEU effects in MGTs

- SEU in MGTs are expressed as either
  - Corruption of transmitted data (bit errors)
  - Failure of RX/TX mechanisms (component failure)
MGT Architecture on Xilinx FPGAs
Xilinx MGT Tile

Tile

Shared Resources

Xilinx Corporation Virtex-5 FPGA RocketIO GTX Transceiver User Guide (ug198), pg 28
MGT RX/TX Detail
Aurora Radiation Test Motivation

1. Understand Aurora’s ability to repair the communication link
2. Determine error signatures of different upsets
3. Correlate Aurora faults with known MGT fault mechanisms
4. Identify recovery techniques
Xilinx Aurora Protocol

- Protocol for serial data transmission
  - OSI link level protocol
  - Lightweight
    - ~500 slices, no BRAM
    - Minimal transmission overhead
  - Supports bonding of multiple lanes
- Easy to implement
  - IP core available via Xilinx Coregen
  - Simple framing interface
- Encompasses MGT tile
- Higher protocol levels easily built on top

Aurora Tile

MGT

CHREC
NSF Center for High-Performance Reconfigurable Computing

BYU
Brigham Young University
Xilinx Aurora Protocol - Features

- Simple Error Detection - No error correction
  - Reports tile level errors
  - Detects framing errors
- Design may contain PLL
- Instantiates an MGT tile
- Coregen sets MGT parameters
Test Setup – Error Output

- Three levels of error signals

V5FX130T – Service (SRV)
- CRC, Frame Generator
- Frame Checker
- CRC, Frame Generator
- Frame Checker

Aurora
Tile

V5 SIRF - DUT
- CRC, Frame Generator
- Frame Checker
- CRC, Frame Generator
- Frame Checker

Aurora
Tile

Data Aurora Tile

Tile Aurora Data
Test Setup – Recovery Steps

1. Self Recovered
   1. Bit-errors, etc.

2. Aurora Recovered
   1. RX/TX Reset

3. Manually Recovered
   1. Aurora Logic Reset
   2. Aurora PLL Reset
   3. CDR Reset
   4. Tile Reset
   5. Configuration Scrub
   6. Configuration Scrub with GLUT Mask Off

4. Reconfigure
March 21-25, 2011 – Texas A&M (College Station)

- 14 hours of beam time
  - Neon-1, Argon, Xenon, and Krypton
  - 3.1, 10.2, 22.9, and 46.1 MeV-cm²/mg

Special thanks to Sandia, Seakr Engineering and Xilinx for their help and support on this test.
Test Results – Recovery Types

- 97% of events required no intervention
- All but .12% of events recovered with manual intervention

Breakdown of Manually Recovered

<table>
<thead>
<tr>
<th>Manual Recovery Method</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aurora Reset</td>
<td>28.4%</td>
</tr>
<tr>
<td>Aurora Logic PLL Reset</td>
<td>28.4%</td>
</tr>
<tr>
<td>CDR Reset (Lane Level)</td>
<td>0%</td>
</tr>
<tr>
<td>GTX Reset (Tile Level)</td>
<td>12.3%</td>
</tr>
<tr>
<td>Scrub with GLUT Mask On</td>
<td>21.0%</td>
</tr>
<tr>
<td>Scrub with GLUT Mask Off</td>
<td>9.9%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100%</strong></td>
</tr>
</tbody>
</table>
**Data Analysis – Error Signatures**

- **Signature** – Set of first set of signals seen in an event before any other error signals
- These signatures give insight into possible source of event
- Several surprising discoveries from this analysis
- Example log file (signature bolded) -

```
... Event Start, 030f9ee4ae, RX Disparity
  Event End, 030f9ee5b4, Soft Error, CRC Failure
...
  Event Start, 03221dfdec, CRC Failure
  Event End, 03221dfe93,
...```
## Data Analysis – Error Signatures

<table>
<thead>
<tr>
<th>Level</th>
<th>Signature</th>
<th>DUT</th>
<th>SRV</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tile</td>
<td>RX Disparity, RX Not in Table</td>
<td>592</td>
<td>630</td>
<td>1222</td>
</tr>
<tr>
<td>Tile</td>
<td>RX Realign</td>
<td>12</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>Tile</td>
<td>RX Buffer Error</td>
<td>15</td>
<td>4</td>
<td>19</td>
</tr>
<tr>
<td>Tile</td>
<td>TX Buffer Error</td>
<td>103</td>
<td>0</td>
<td>103</td>
</tr>
<tr>
<td>Aurora</td>
<td>Hard Error, Soft Error</td>
<td>12</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>Aurora</td>
<td>Frame Error</td>
<td>9</td>
<td>5</td>
<td>14</td>
</tr>
<tr>
<td>Aurora</td>
<td>RX Reset, TX Reset</td>
<td>4</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>Data</td>
<td>CRC Failure, Missing Frame</td>
<td>929</td>
<td>409</td>
<td>1338</td>
</tr>
<tr>
<td>Data</td>
<td>Persistent CRC</td>
<td>14</td>
<td>0</td>
<td>71</td>
</tr>
<tr>
<td><strong>All</strong></td>
<td><strong>Total</strong></td>
<td>1719</td>
<td>1076</td>
<td>2795</td>
</tr>
</tbody>
</table>
Test Conclusions

- With Aurora protocol 97% of upsets are recovered
- For other 2.5% - Recovery mechanisms could be added to Aurora or other protocols with minimal effort
- MGT tile error signals do not report all tile level upsets - possibly ~50% of bit errors unreported
- CRC check necessary to catch all bit errors
Future Work

- Additional radiation testing performed July 2011
  - Data analysis ongoing
  - Analysis on availability, event durations, recovery times, multi-lane events
  - DRP Scrubbing

- Development and testing of mitigation techniques
  - Lossless protocols
    - Dual Channel, RAISERIO
  - Low-cost protocol
    - LRP