MAPLD 2011
RTProASIC3 Qualification Updates

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Presentation Outline

- RTProASIC3 Highlights
- Flash Switch Architecture and Operation
- Production Test Methodology
- Qualification Results Summary
- Conclusion
RTProASIC3 Highlights
RTProASIC3 Highlights

- 130nm Flash based LVCMOS process
- Firm Error (FER) Immune

- Secure Programming / Arm Cortex-M1 soft processor support
- Versa Tiles (Core operates at either 1.2V or 1.5V)
- Clock Conditioning Circuit / PLL
- Embedded SRAM Blocks
- Charge Pumps
- Flash*Freeze Technology
- FlashROM
- USER

- Charge Pumps
- Allows instantaneous shut off of dynamic power consumption while retaining all SRAM and register information

- ISP AES Decryption
- (i.e. LVTTL, LVCMOS, PCI, PCI-X, LVPECL, LVDS, BLVDS, M-LVDS, GTL, GTL+, HSTL)
# RTProASIC3 Highlights

## Features Summary

<table>
<thead>
<tr>
<th>RT ProASIC3 Devices</th>
<th>RT3PE600L</th>
<th>RT3PE3000L</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM Cortex-M1 Devices</td>
<td>N/A</td>
<td>M1RT3PE3000L</td>
</tr>
<tr>
<td>System Gates</td>
<td>600 k</td>
<td>3 M</td>
</tr>
<tr>
<td>VersaTiles (D-flip-flops)</td>
<td>13,824</td>
<td>75,264</td>
</tr>
<tr>
<td>RAM kbits (1,024 bits)</td>
<td>108</td>
<td>504</td>
</tr>
<tr>
<td>4,608-Bit Blocks</td>
<td>24</td>
<td>112</td>
</tr>
<tr>
<td>FlashROM Bits</td>
<td>1 k</td>
<td>1 k</td>
</tr>
<tr>
<td>Secure (AES) ISP</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Integrated PLL in CCCs</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>VersaNet Globals</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>I/O Banks</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Maximum User I/Os</td>
<td>270</td>
<td>620</td>
</tr>
<tr>
<td>Package Pins</td>
<td>CG/LG484, CQ256</td>
<td>CG/LG484, CG/LG896, CQ256</td>
</tr>
</tbody>
</table>
Flash Switch Architecture and Operation
Flash Switch Architecture

- The Flash switch (Non-Volatile Memory cell) is a floating gate transistor

- The RTProASIC3 Flash cell is composed of 2 transistors sharing a common floating and control gate

- Used for logic head configuration and routing tracks connection/isolation
Internal charge pumps provide the high positive/negative voltages required.
Production Test Methodology
Production Test Methodology

Per MIL-STD-883E
Production Flow

Bake / Wafer Sort
Assembly
Constant Acceleration / Fine and Gross Leak
Serialization
NVM / Functional Test
Pre Burnin Electrical Test (25C)

Dynamic Burnin 160hrs (125C)
Post Burnin Electrical Test (25C)
Mil Cold Electrical Test (-55C)
Mil Hot Electrical Test (125C)
QA Electrical Test (25C)
EOL
Burn-In Electrical Test

- High utilization Burn-In test design used in both production flow and qualification (Group C test)

Coverage of test
- Electronic serialization based on Lot/Wafer/Die X,Y information
- Standby $I_{dd}$ on individual power domain
- Full DC parametric testing for all configurations on all bonded I/Os
- Functional test for Burn-in design
- PLL functional test
- Delay Line Test (speed performance)
Burn-In Design Overview (1 of 3)

- **Clock Source**
  - External clock is fed into the PLLs of the device
  - PLLs deliver the clock signals through global (low skew) networks

- **Combo Block**
  - Utilizes every combinatorial macro in the A3P library

- **Register & Latch Block**
  - Utilizes every sequential macro in the A3P library.

- **USER FlashROM (UFROM)**
  - Pre-determined Combo Block output pattern is stored into the UFROM
  - Content is compared during burn-in
Burn-In Design Overview (2 of 3)

- **Embedded SRAM Blocks**
  - Full test coverage on all SRAM cells
  - Dual Port / Two Port / FIFO configurations
  - Varying depth and width configurations

![Diagram of embedded SRAM blocks](image)
Burn-In Design Overview (3 of 3)

- **Shift Register Block**
  - Scalable block for maximizing core utilization
  - Controlled simultaneous switch rate (SSR)

- **IO Block**
  - Scalable block for maximizing I/O utilization
  - Utilizes all possible I/O configurations
  - Controlled simultaneous switching outputs (SSO)

- **Oscillator Block**
  - Free running oscillator to monitor silicon performance
Qualification Results Summary
# Qualification Results Summary

**Qualification Vehicle: RT3PE3000L–CG896**

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Reference</th>
<th>Test Condition</th>
<th># of Qual Lots</th>
<th># Failures / Sample Size</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group A</td>
<td>MIL-STD-883</td>
<td>$T_A = -55^\circ C / 25^\circ C / 125^\circ C$</td>
<td>1</td>
<td>0/116</td>
<td>PASSED</td>
</tr>
</tbody>
</table>
| Group C (HTOL)    | MIL-STD-883 (TM1005) | $T_A = 125^\circ C$  
$V_{CC} / V_{CC_PLL} = 1.6V$ 
$V_{CCI} / V_{PP} / V_{JTAG} = 3.6V$ | 1              | 0/79 (+2 spares)        | PASSED 2500 hrs$^1$ |
| Group D3/D4       | MIL-STD-883 (TM1005) | $T_A = -65^\circ C$ to $150^\circ C$ | 1              | 0/15                     | PASSED 100 cycles    |
| ESD               | MIL-STD-883 (TM3015) | HBM                             | 1              | 0/3                      | PASSED$^2$           |
| Latchup           | JEDEC 78          | $T_A = 125^\circ C$             | 1              | 0/6                      | PASSED               |
| Capacitance Test  | MIL-STD-883 (TM3012) | $T_A = 25^\circ C$             | 1              | 0/3                      | PASSED               |
| Characterization  |                   | $T_A = -55^\circ C$ to $125^\circ C$  
Bias = min to max operating condition | 1              | 5                        | COMPLETED            |

1) Note: Mil-STD-883 requires 1000hrs HTOL. As part of the on-going reliability process, HTOL will continue up to 6000hrs
2) Note: HBM passed for 500V (class 1B) on Vcc_PLL and 2000V (class 2) on all other power supplies and IOs
Group C – Endurance Result

- **Group C Flow**
  - Endurance test – 550 program / erase cycles
  - Margining – complete characterization of all flash cells
  - Pre – electrical / functional test
  - 1000hrs HTOL
  - Post – electrical / functional test
  - Margining – monitor any $V_t$ shift (charge leakage) in flash cell

![Margin Plots of Qual Lot (Pre vs. Post 1000hrs HTOL)](image)
Conclusion

- CMOS FIT Rate based on all 0.13um UMC Flash FPGA HTOL data is $16.6^*$
  (*Note: The calculated FIT is based on 60% confidence level @ 55°C using $E_a = 0.7$eV)

<table>
<thead>
<tr>
<th>Product</th>
<th>Package</th>
<th>Wafer Lot</th>
<th>Date Code</th>
<th>Number of Units</th>
<th>Test Time</th>
<th>$T_J$ (°C)</th>
<th>Test Time @ $T_J$ 125°C</th>
<th>168</th>
<th>500</th>
<th>1000</th>
<th>2000</th>
<th>3000</th>
<th>Unit Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>A3P600</td>
<td>FPGAG256</td>
<td>QH4H0</td>
<td>0728</td>
<td>81</td>
<td>1000</td>
<td>130</td>
<td>1288</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>104343</td>
</tr>
<tr>
<td>A3PE3000</td>
<td>FPGAG484</td>
<td>QHC9T</td>
<td>0806</td>
<td>1</td>
<td>2000</td>
<td>135</td>
<td>3298</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3298</td>
</tr>
<tr>
<td>RT3PE3000L</td>
<td>CGA896</td>
<td>QHR8G</td>
<td>0925</td>
<td>82</td>
<td>1000</td>
<td>142</td>
<td>2307</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>189203</td>
</tr>
</tbody>
</table>

**TOTAL Units for 0.13 μm FPGA = 292**
**Total Test Time Hours = 1563396**

- The following die/package combinations are qualified per the MIL-STD-883B in the RTProASIC3 family and are available for customer use as of today:

<table>
<thead>
<tr>
<th>Package Type</th>
<th>RT3PE600L</th>
<th>RT3PE3000L</th>
</tr>
</thead>
<tbody>
<tr>
<td>CG/LG484</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CG/LG896</td>
<td>N/A</td>
<td>✓</td>
</tr>
<tr>
<td>CQ256</td>
<td>TBD</td>
<td>TBD</td>
</tr>
</tbody>
</table>
Acknowledgement

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Tejpal Sahota
Solomon Wolday
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