



MAPLD 2011 RTProASIC3 Qualification Updates

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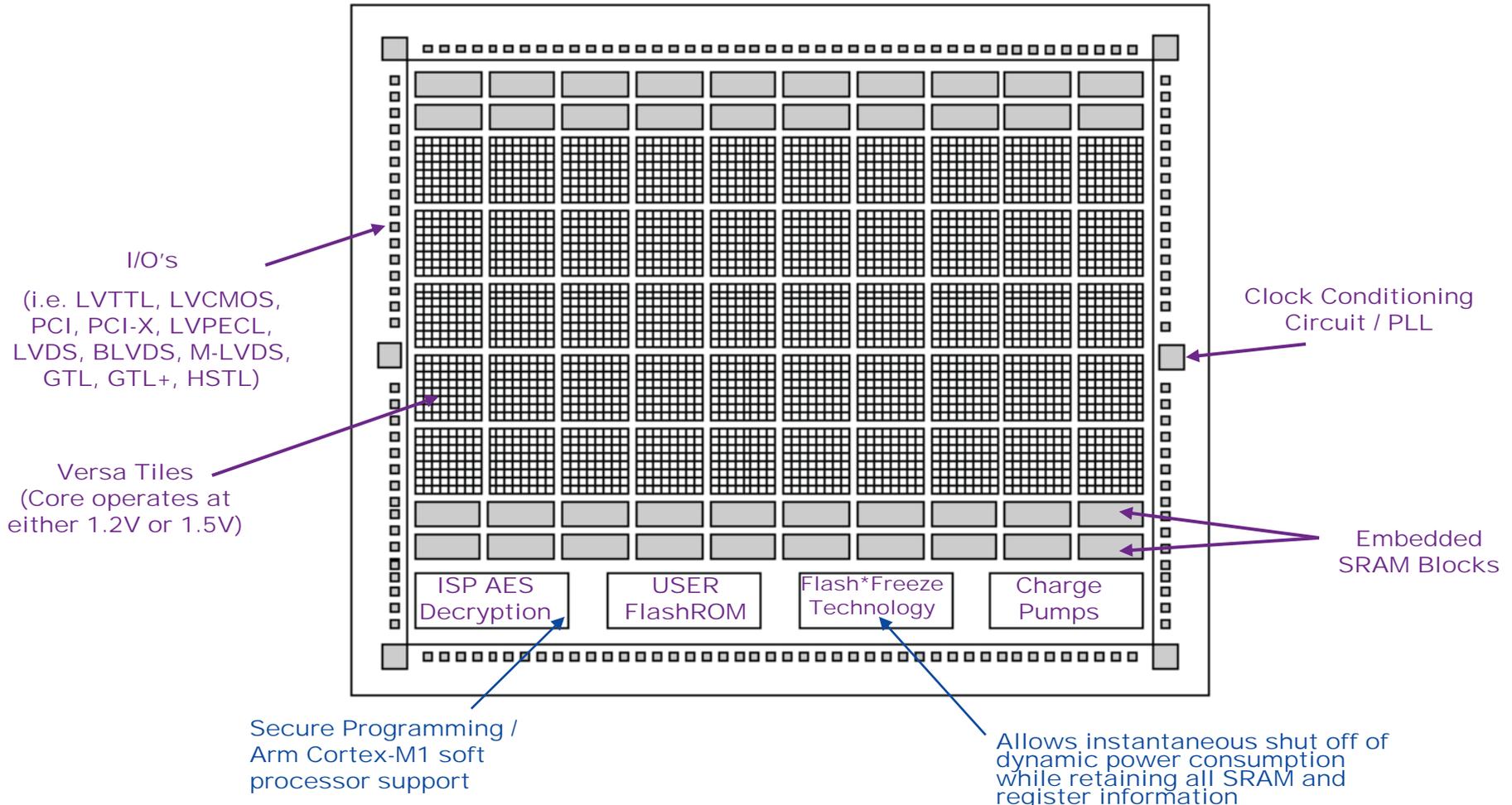
Presentation Outline

- **RTProASIC3 Highlights**
- **Flash Switch Architecture and Operation**
- **Production Test Methodology**
- **Qualification Results Summary**
- **Conclusion**

RTProASIC3 Highlights

RTProASIC3 Highlights

- 130nm Flash based LVC MOS process
- Firm Error (FER) Immune



RTProASIC3 Highlights

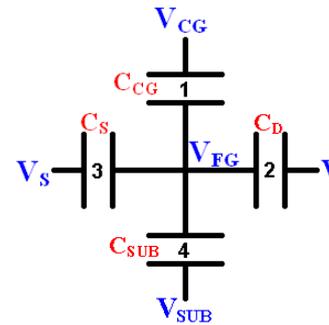
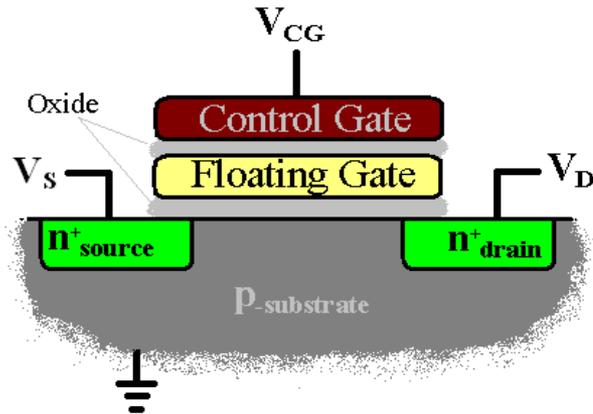
Features Summary

RT ProASIC3 Devices	RT3PE600L	RT3PE3000L
ARM Cortex-M1 Devices	N/A	M1RT3PE3000L
System Gates	600 k	3 M
VersaTiles (D-flip-flops)	13,824	75,264
RAM kbits (1,024 bits)	108	504
4,608-Bit Blocks	24	112
FlashROM Bits	1 k	1 k
Secure (AES) ISP	Yes	Yes
Integratred PLL in CCCs	6	6
VersaNet Globals	18	18
I/O Banks	8	8
Maximum User I/Os	270	620
Package Pins	CG/LG484 CQ256	CG/LG484, CG/LG896 CQ256

Flash Switch Architecture and Operation

Flash Switch Architecture

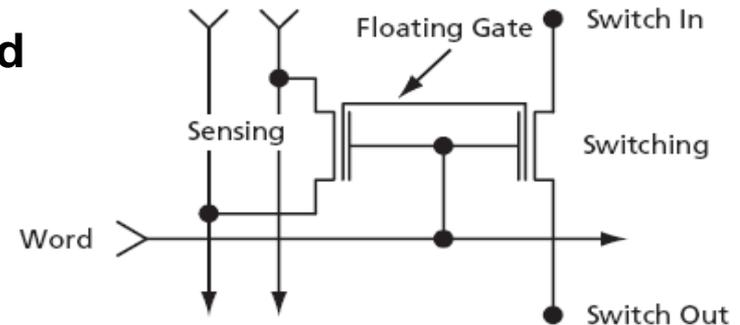
- The Flash switch (Non-Volatile Memory cell) is a floating gate transistor



$$V = \frac{Q}{C_T} + \sum_{k=1}^K \frac{C_k}{C_T} V_k$$

$$C_T = C_{CG} + C_D + C_S + C_{SUB}$$

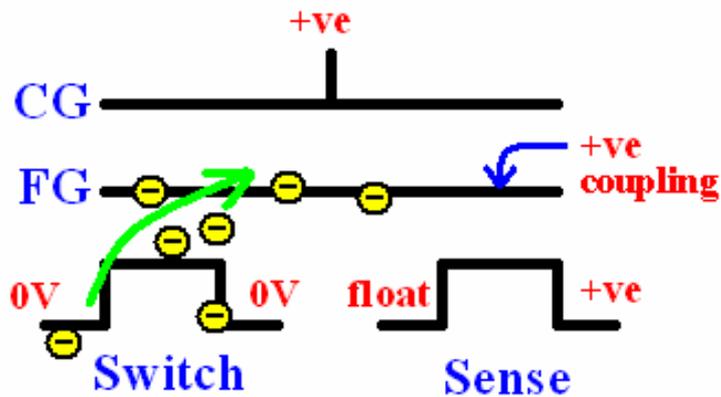
- The RTProASIC3 Flash cell is composed of 2 transistors sharing a common floating and control gate



- Used for logic head configuration and routing tracks connection/isolation

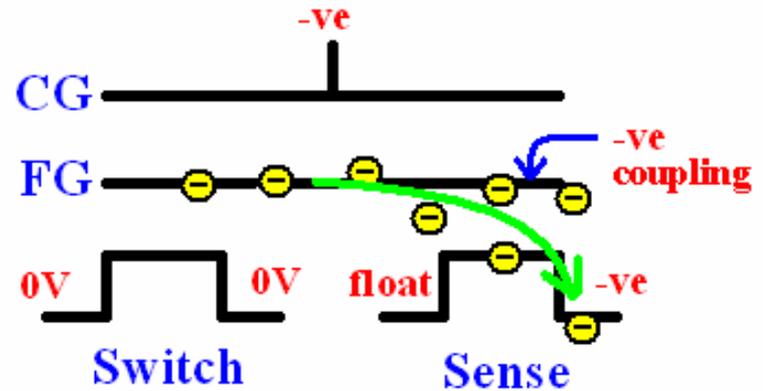
Program & Erase Operation

PROGRAM



After uncoupling
 V_{FG} is -ve
(switch is *OFF*)

ERASE



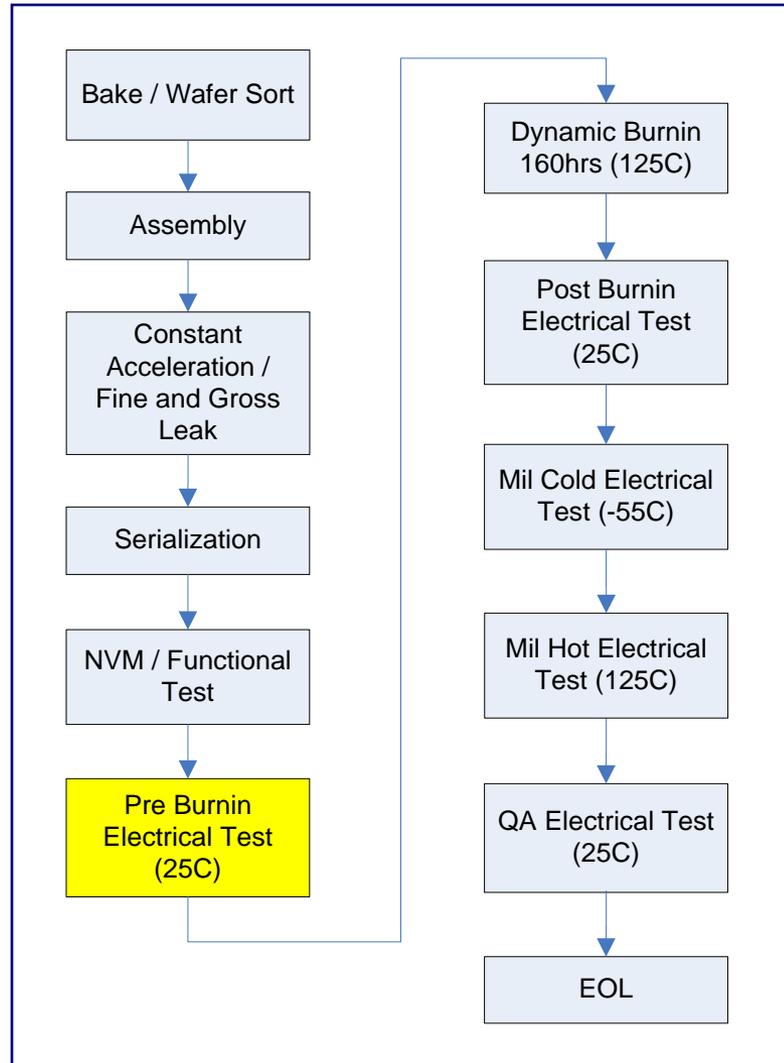
After uncoupling
 V_{FG} is +ve
(switch is *ON*)

- Internal charge pumps provide the high positive/negative voltages required

Production Test Methodology

Production Test Methodology

Per MIL-STD-883E Production Flow



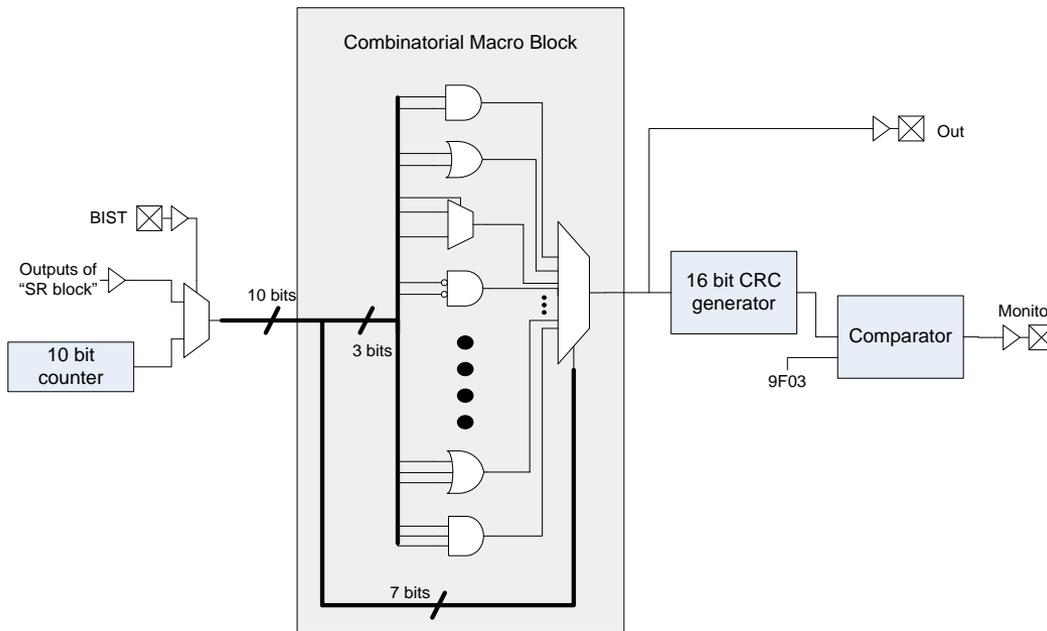
Burn-In Electrical Test

- **High utilization Burn-In test design used in both production flow and qualification (Group C test)**
- **Coverage of test**
 - **Electronic serialization based on Lot/Wafer/Die X,Y information**
 - **Standby I_{dd} on individual power domain**
 - **Full DC parametric testing for all configurations on all bonded I/Os**
 - **Functional test for Burn-in design**
 - **PLL functional test**
 - **Delay Line Test (speed performance)**

Burn-In Design Overview (1 of 3)

■ Clock Source

- External clock is fed into the PLLs of the device
- PLLs deliver the clock signals through global (low skew) networks



■ Combo Block

- Utilizes every combinatorial macro in the A3P library

■ Register & Latch Block

- Utilizes every sequential macro in the A3P library.

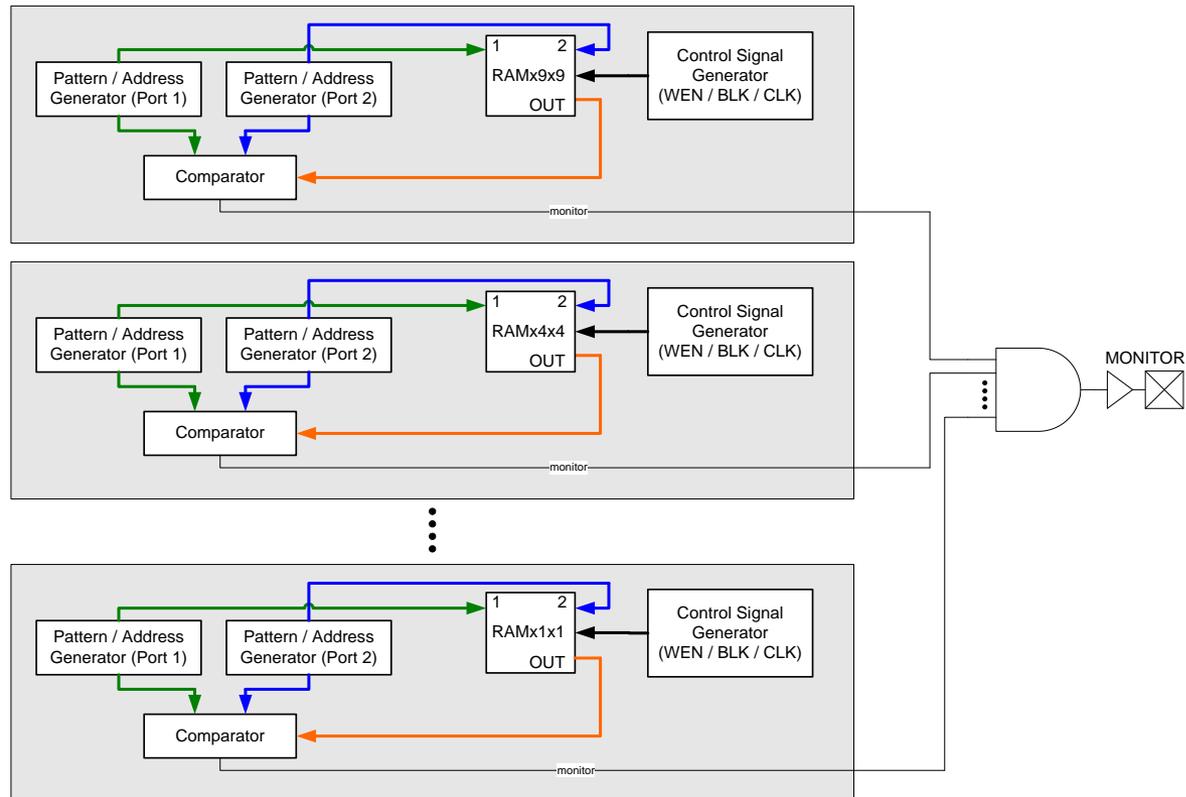
■ USER FlashROM (UFROM)

- Pre-determined Combo Block output pattern is stored into the UFROM
- Content is compared during burn-in

Burn-In Design Overview (2 of 3)

■ Embedded SRAM Blocks

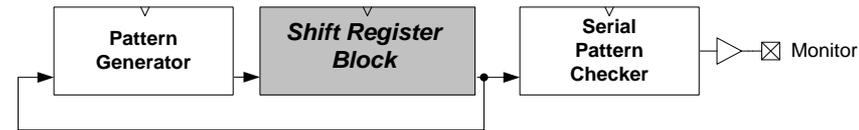
- Full test coverage on all SRAM cells
- Dual Port / Two Port / FIFO configurations
- Varying depth and width configurations



Burn-In Design Overview (3 of 3)

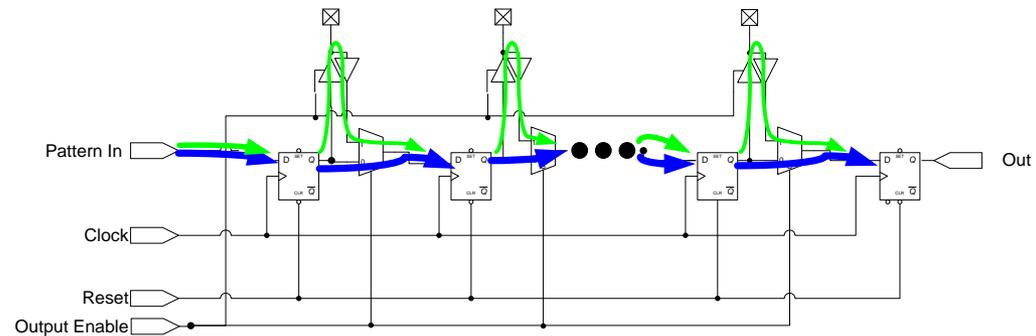
■ Shift Register Block

- Scalable block for maximizing core utilization
- Controlled simultaneous switch rate (SSR)



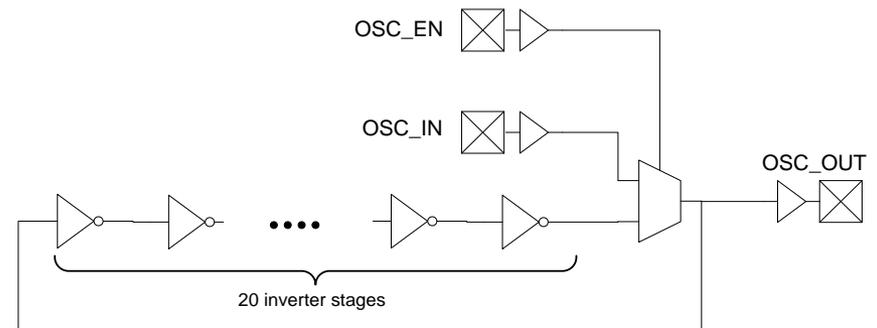
■ IO Block

- Scalable block for maximizing I/O utilization
- Utilizes all possible I/O configurations
- Controlled simultaneous switching outputs (SSO)



■ Oscillator Block

- Free running oscillator to monitor silicon performance



Qualification Results Summary

Qualification Results Summary

Qualification Vehicle: RT3PE3000L–CG896

Stress Test	Reference	Test Condition	# of Qual Lots	# Failures / Sample Size	Results
Group A	MIL-STD-883	$T_A = -55^{\circ}\text{C} / 25^{\circ}\text{C} / 125^{\circ}\text{C}$	1	0/116	PASSED
Group C (HTOL)	MIL-STD-883 (TM1005)	$T_A = 125^{\circ}\text{C}$ $V_{CC} / V_{CC_PLL} = 1.6\text{V}$ $V_{CCI} / V_{PP} / V_{JTAG} = 3.6\text{V}$	1	0/79 (+2 spares)	PASSED 2500 hrs ¹
Group D3/D4	MIL-STD-883 (TM1005)	$T_A = -65^{\circ}\text{C} \text{ to } 150^{\circ}\text{C}$	1	0/15	PASSED 100 cycles
ESD	MIL-STD-883 (TM3015)	HBM	1	0/3	PASSED ²
Latchup	JEDEC 78	$T_A = 125^{\circ}\text{C}$	1	0/6	PASSED
Capacitance Test	MIL-STD-883 (TM3012)	$T_A = 25^{\circ}\text{C}$	1	0/3	PASSED
Characterization		$T_A = - 55^{\circ}\text{C} \text{ to } 125^{\circ}\text{C}$ Bias = min to max operating condition	1	5	COMPLETED

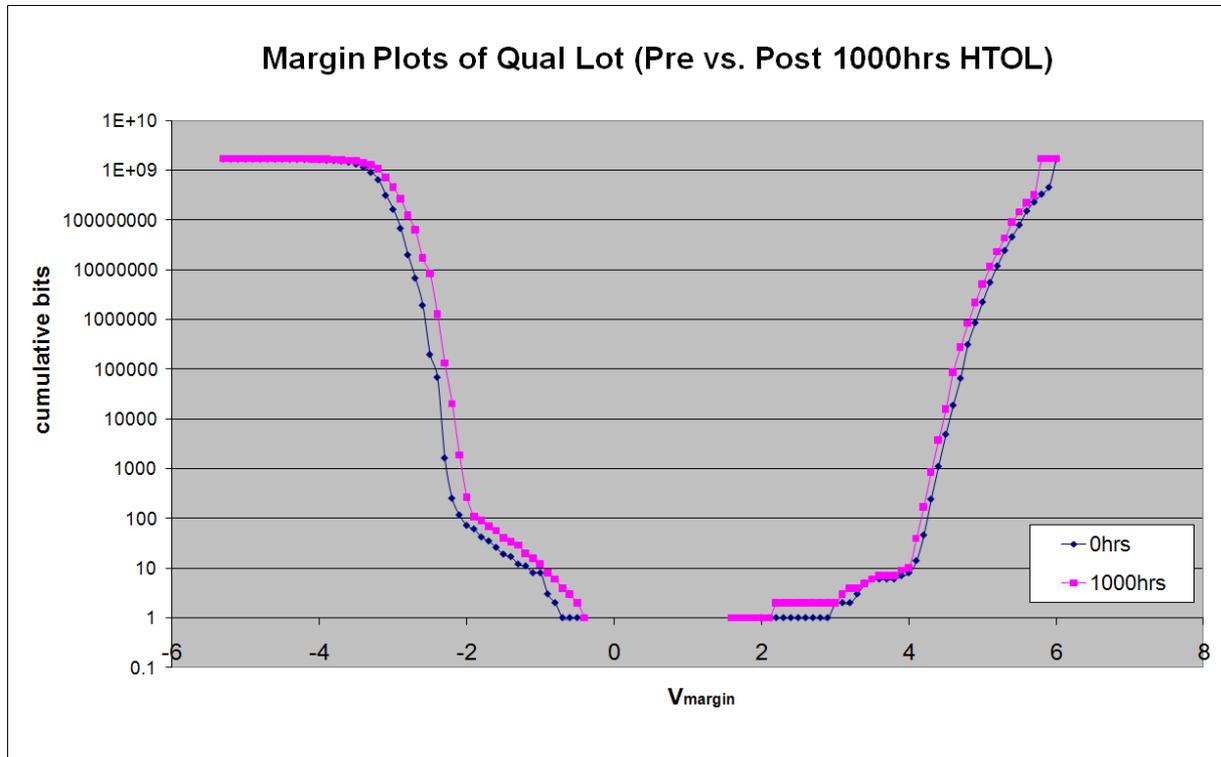
1) Note: Mil-STD-883 requires 1000hrs HTOL. As part of the on-going reliability process, HTOL will continue up to 6000hrs

2) Note: HBM passed for 500V (class 1B) on Vcc_Pll and 2000V (class 2) on all other power supplies and IOs

Group C – Endurance Result

■ Group C Flow

- Endurance test – 550 program / erase cycles
- Margining – complete characterization of all flash cells
- Pre – electrical / functional test
- 1000hrs HTOL
- Post – electrical / functional test
- Margining – monitor any V_t shift (charge leakage) in flash cell



Conclusion

- CMOS FIT Rate based on all 0.13um UMC Flash FPGA HTOL data is **16.6***
 (*Note: The calculated FIT is based on 60% confidence level @ 55°C using $E_a = 0.7\text{eV}$)

Product	Package	Wafer Lot	Date Code	Number of Units	Test Hours / Failures								
					Test Time	T _J (°C)	Test Time @ T _J 125°C	168	500	1000	2000	3000	Unit Hours
A3P600	FPGAG256 ¹	QH4H0	0728	81	1000	130	1288	0	0	0			104343
A3PE3000	FPGAG484 ¹	QHC9T	0806	1	2000	135	3298	0	0	0	0	1 ²	3298
			0808 0809	128	6000	135	9895	0	0	0	0	0	1266552
RT3PE3000L	CGA896	QHR8G	0925	82	1000	142	2307	0	0	0	0		189203
TOTAL Units for 0.13 μm FPGA =				292	Total Test Time Hours							1563396	
TOTAL Failures for 0.13 μm FPGA = 1													

- The following die/package combinations are qualified per the MIL-STD-883B in the RTProASIC3 family and are available for customer use as of today:

Package Type	RT3PE600L	RT3PE3000L
CG/LG484	✓	✓
CG/LG896	N/A	✓
CQ256	TBD	TBD

Acknowledgement

Thank you to the following people who helped made this presentation possible

Tejpal Sahota
Solomon Wolday
Antony Wilson