Virtex-5QV

Launching Tomorrow's Architecture Today

Compendium of XRTC Radiation Results on All Single-Event Effects Observed in the Virtex-5QV

Gary Swift and Carl Carmichael (Xilinx), Greg Allen (JPL), George Madias & Eric Miller (Boeing), Roberto Monreal (SwRI) and all active members of the XRTC

August 22, 2011

SEE Testing Overview

- **The XRTC (Xilinx Radiation Test Consortium)**

- **Static Results**
  - Configuration Cell
  - Single Event Latchup
  - Single Event Functional Interrupts
  - Flip-Flops (FFs) and Single Event Transients (SETs)
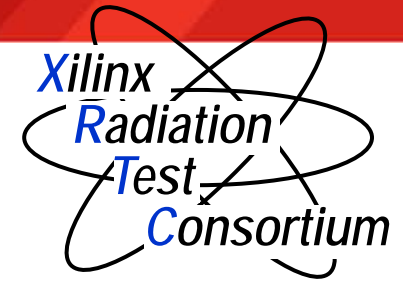 - Block Memory (BRAM)

- **Dynamic Results**
  - Block Memory EDAC
  - FF SET Filter Effectiveness
  - Clock Management (PLL & DCM)
  - Multi-Gigabit Transceivers (MGTs)
  - Digital Signal Processors
  - IODELAY

- **Leftovers and Conclusions**

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Xilinx Radiation Test Consortium

- **Thanks to active members, esp. testers from**

and many others…

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Virtex-5QV - Static Result Summary

	XQR5VFX130	Units	Details
Single-event latchup	**none**	**--**	**Spec Sheet Guarantee**
Total Dose	**1,000,000**	rad(Si)	**Spec Sheet Guarantee**
STATIC Upsets in Geosynchronous Orbit (GEO)			
SEFIs	**9,930**	**years/Device**	**Mean Time to SEFI**
CLB-FF (filters on)	**3**	upsets/century	**all 81,920 bits**
CLB-FF (filters off)	**1-2**	upsets/year	**all 81,920 bits**
Configuration Bits	**5***	upsets/year	**all 34.1 million bits**
Block Memory (EDAC off)	**13**	upsets/day	**all 10.9 million bits**

* - More than 10 needed to cause design malfunction, on average;
thus, MTTF is greater than <u>2 years</u>.

Dramatic Improvements from Upset Hardening

- ~1000x improvement on SEU rate (per bit vs. Virtex-4QV)
- ~100x improvement on SEFI rate (per device vs. Virtex-4QV)

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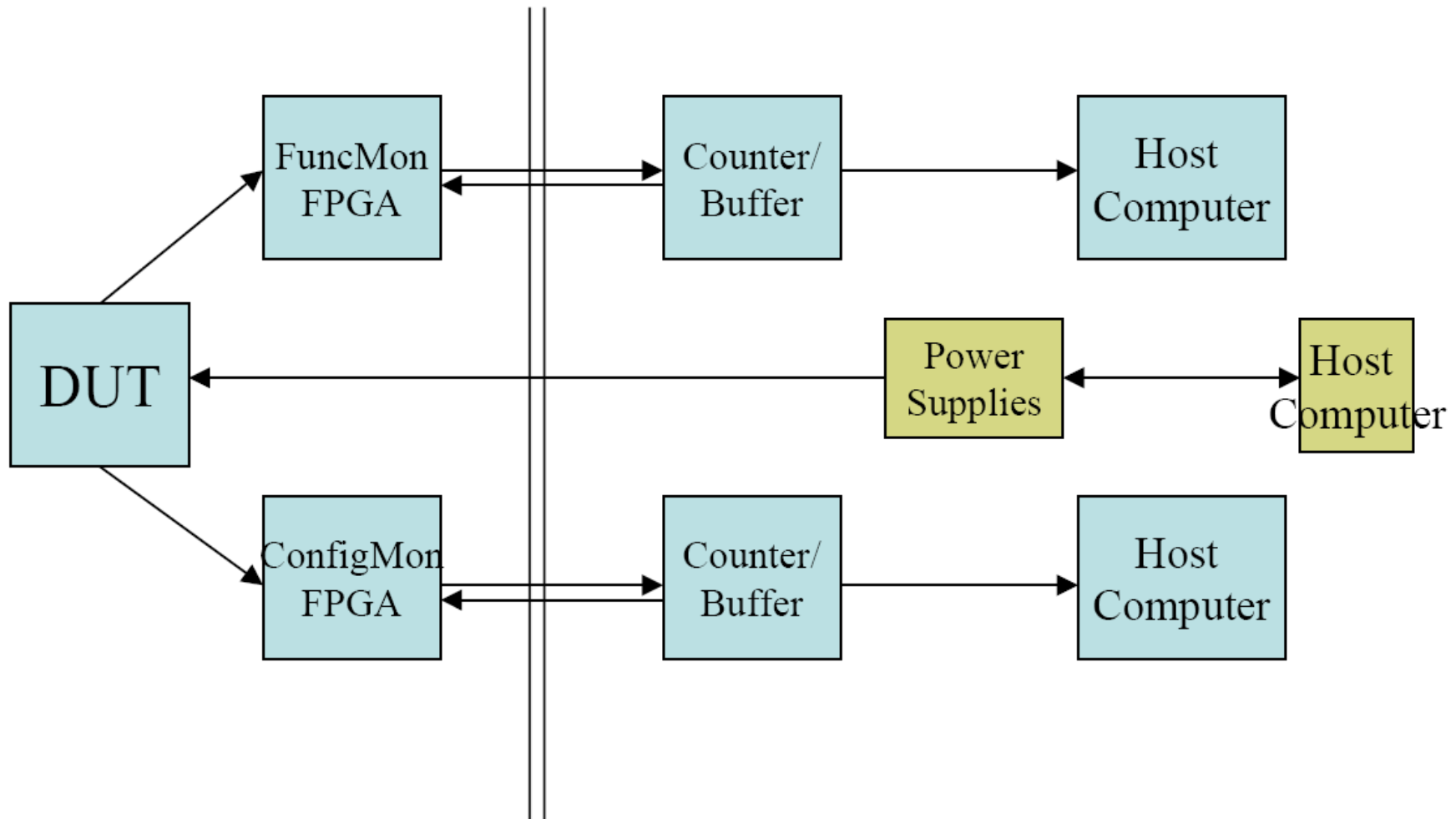
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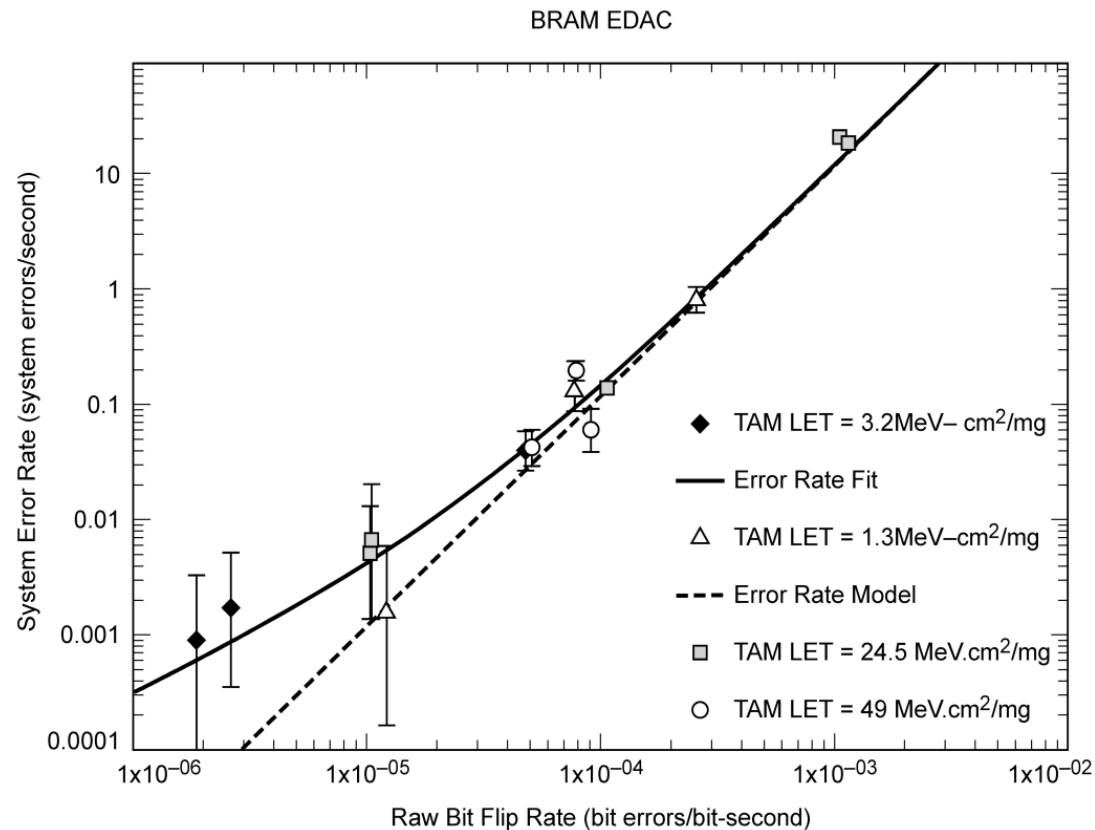
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XRTC Test Setup

Simplified: Three Main Strip Charts

BRAM Error-Detect-and-Correct (EDAC)

- **Built-in error correction (one bit) and detection (two bits) using (64,72) Hamming code to effectively mitigate upsets and enhanced with writeback mode to prevent their accumulation.**

- **Upset modes**
  - Cells (unhardened) upset
  - EDAC hits

- **Expected GEO rates:**
  - Cells: 12.7 per day
  - EDAC hits yield errors:
    less than one per decade

- **Proton susceptible; data available.**

BRAM EDAC

Legend:
- TAM LET = 3.2MeV– cm²/mg
- Error Rate Fit
- TAM LET = 1.3MeV–cm²/mg
- Error Rate Model
- TAM LET = 24.5 MeV.cm²/mg
- TAM LET = 49 MeV.cm²/mg

Y-axis: System Error Rate (system errors/second)
X-axis: Raw Bit Flip Rate (bit errors/bit-second)

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SET Filters for User Flip-Flops

- **Intended to lower SET upsets in FF's**

- **Inputs must "agree" to alter register state**
  - Dual inputs facilitate temporal filters
  - Only *long* SETs get thru
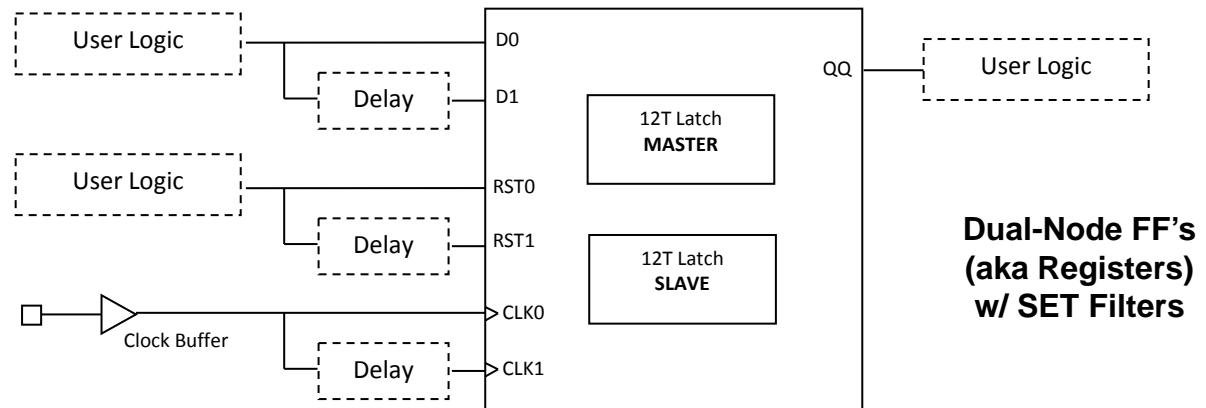
- **Improvement in GEO ranges from 2x to 100x, depending on pattern, levels of intervening logic, and frequency**

- **SET filters should discriminate well against proton-induced transients; definitive proton data is TBD**

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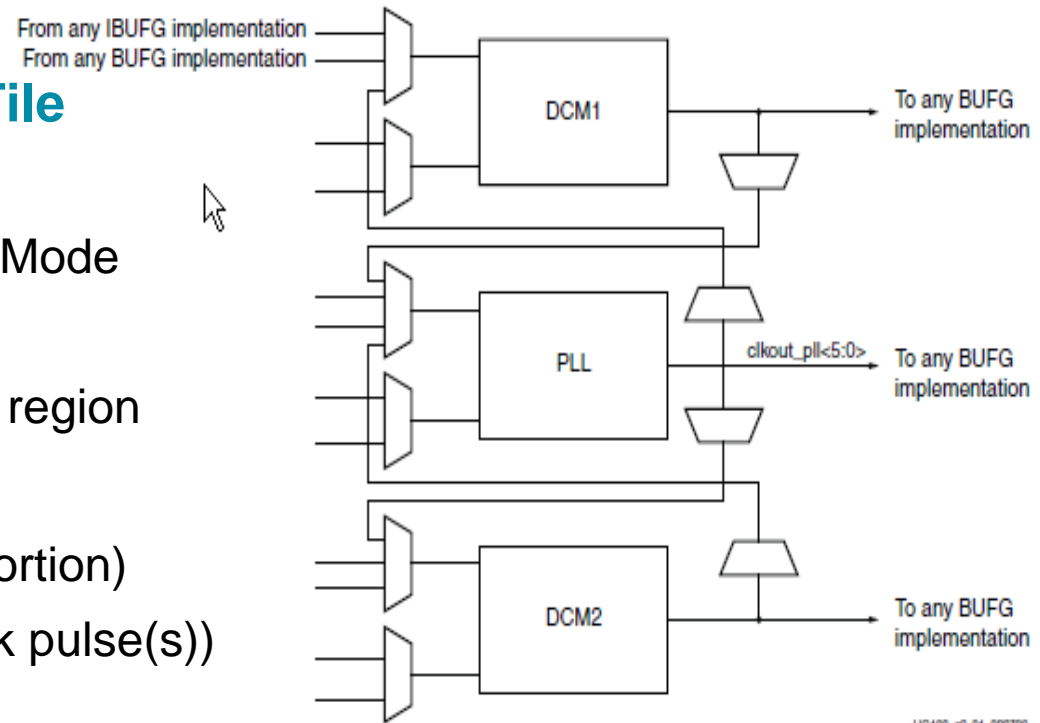
Clock Management (PLL & DCM)

- **CMT – Clock Management Tile**
  - 2 DCM + 1 PLL (with PMCD)
  - Independent use or Cascade Mode
  - 12 DCM + 6 PLL in SIRF
 - 10 BUFG output max in clock region

- **Upset Modes:**
  - SET glitch (extra clock or distortion)
  - SET long pulse (swallow clock pulse(s))
  - "Scramble" requiring reset
  - Unreliable "lock" signal

- **Glitch rate is worst-case; for GEO, that's less than one per century**

- **Proton susceptibility projected to be small; proton data TBD**

From any IBUFG implementation
From any BUFG implementation

DCM1 — To any BUFG implementation

PLL — clkout_pll<5:0> — To any BUFG implementation

DCM2 — To any BUFG implementation

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IODelay is …

- **A programmable delay line on each input and output which gives a per-bit de-skew capability that greatly eases interfacing to modern high-speed memories, like QDR SRAM & DDR3 DRAM**

- **Unhardened and subject to:**
  - Delay upsets
  - Controller upsets

- **Expected GEO rates:**
  - Delay: 2.8 hits/100 yrs
  - Controller:
    - 0.3 hits/100 yrs

- **Probably proton hits will increase the rates**

- **Mechanism not fully understood; proton measurements needed.**

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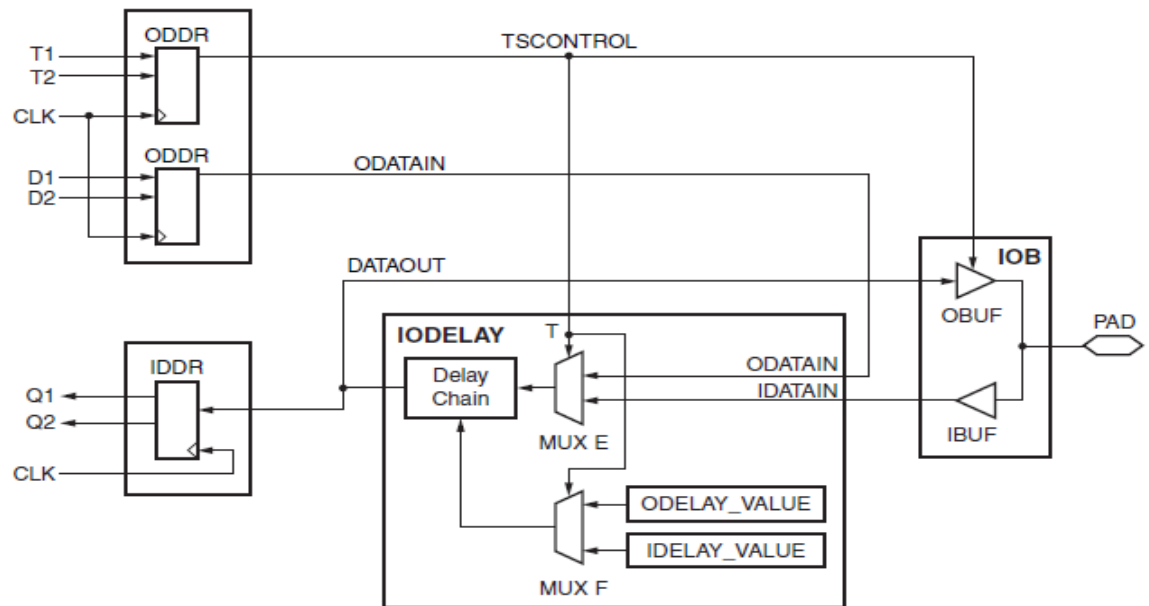
Dynamic Results Summary Table

XQR5VFX130	MTTU*	Units	Upset & Op Details
DYNAMIC Upsets in Geosynchronous Orbit (GEO)			
DCM, PLL	130	years per DCM or PLL	**Glitch, 12 DCMs + 6 PLLs**
MultiGigabit Tranceivers	20	years/GTX	**LOL**, 18 GTX's, 3.125 GHz**
Block Memory (EDAC on)	12	years/Device	**all 10.9 million bits**
CLB-FF (filters on)	2.5	years/Device	**all 81,920 bits, 200 MHz**
CLB-FF (filters off)	2	months/Device	**all 81,920 bits, 200 MHz**
DSP48E	5***	years/DSP	**320 DSP's in Device**
IODELAY	32	years/bit	**836 IO's in Device**
EMAC	TBD	--	
PCIe	TBD	--	

* - MTTU = mean-time-to-upset   ** - LOL=Loss-of-Link   *** - extrapolated to high frequency, 450 MHz

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Remaining Test Plan

- **Complete Proton Radiation for Static & Dynamic FPGA Tests**
  - Next test is October at UC-Davis

- **Continue Evaluation of V5QV Features**
  - DSP *
    - High Speed Testing
    - New Ideas re: Mitigation
  - EMAC & PCIe *
  - Embedded Processing (LEON, MicroBlaze*)

* - not actively under development; awaiting primary experimenter

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Concluding Remarks

- **Virtex-5QV is big and powerful and fast and <u>complex</u>**
  - 65nm, 836 IO's, lots of "fabric" plus complex "hard silicon IP" blocks

- **XRTC has performed an unprecedented amount of testing**
  - More than a thousand hours of beam time used

- **Upset-hardened elements work well**
  - Cause arguments about "What is engineering zero?"

- **Unhardened elements work surprising well also**
  - Hardened configuration removes most previously seen error modes
  - Writeback-enhanced EDAC effectively takes care of BRAM upsets
  - Data "flush through" makes errors short for many cases

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Current Publications & Reports

Title	Author	Publication	Materials
SEU Rate Estimates for Devices Exhibiting Dual Node Susceptibility	Larry Edmonds (JPL)	JPL Pub 11-6, June 2011	White Paper
Radiation Hardened Memory Cell Study in 90nm Technology	Gary Swift	NSREC '09	Slides, Manuscript
Characterization & Filtration of Single Event Transient Effects in 65nm CMOS Technology	Carl Carmichael Eric Miller (Boeing)	SEE Symposium '10	Slides, Manuscript
Study of Single Event Effect manifestations observed in Digital Signal Processor elements embedded in Field Programmable Gate Arrays	Roberto Monreal (SWRI)	SEE Symposium '10	Slides, Abstract
Investigation of the Single Event Effects and Subsequent Recovery Mechanisms induced by Multi-Gigabit Transceivers (MGT)	Roberto Monreal (SWRI)	SEE Symposium '10	Slides, Abstract
Single-Event Upset (SEU) Results of Embedded Error Detect and Correct Enabled Block Random Access Memory (Block RAM) within the Xilinx XQR5VFX130	Greg Allen (JPL)	NSREC '10	Slides, Manuscript
Single-Event Characterization of the Multi-Gigabit Transceivers (MGTs) in the Space-Grade Virtex-5QV FPGA	Roberto Monreal (SWRI)	NSREC '11	Poster, Manuscript
SEL & SEFI Characterization of the 65nm Virtex-5QV Field Programmable Gate Array	Gary Swift Greg Allen (JPL)	NSREC '10	Slides, Manuscript
Virtex-5QV Static SEU Characterization Summary Report	Gary Swift Greg Allen (JPL)	Ver. 0, July 2011	White Paper
Virtex-5QV Dynamic SEU Characterization Summary Report	Gary Swift Greg Allen (JPL)	In Progress	White Paper

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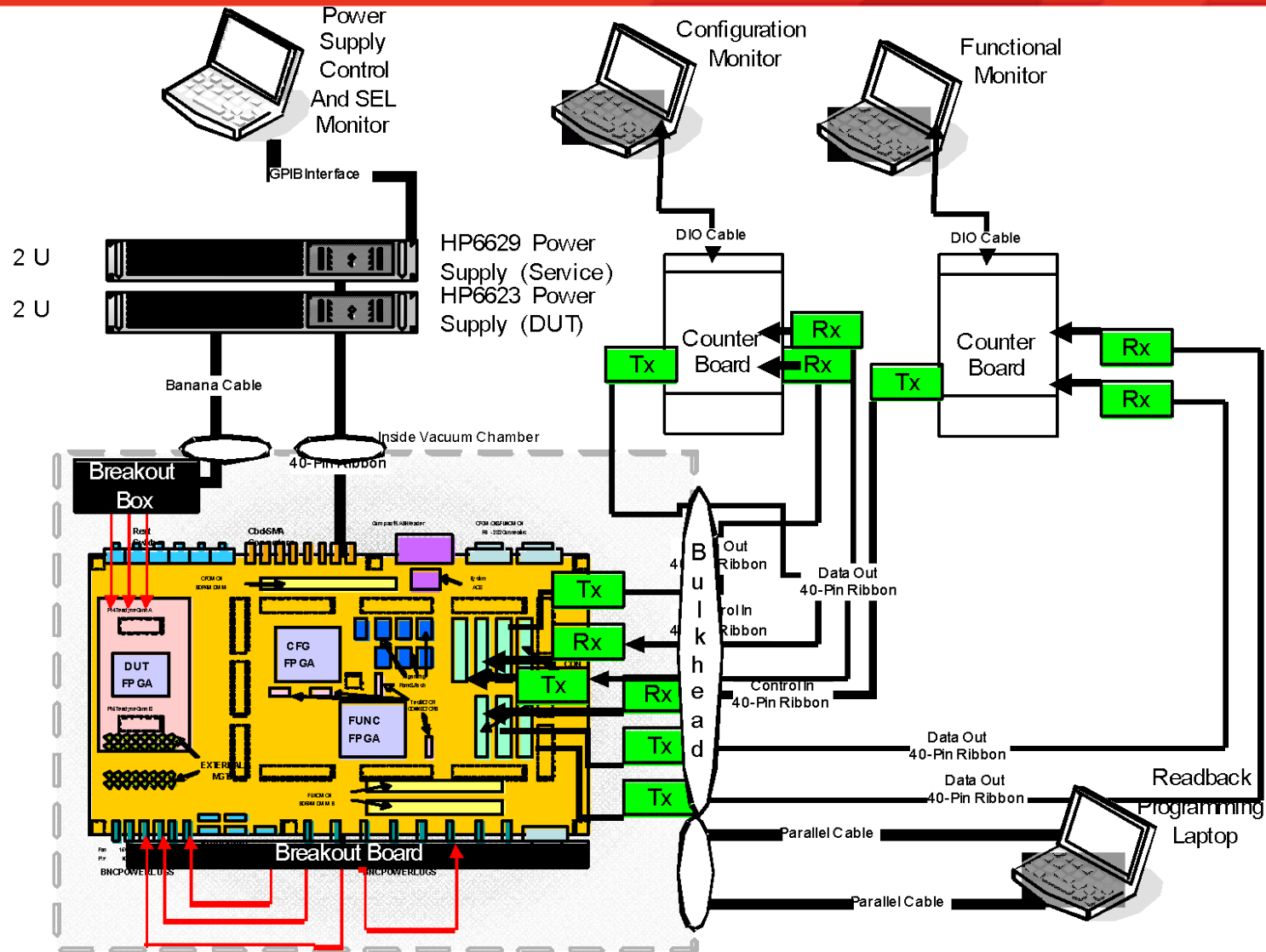# APPENDIX – Additional Details

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Single Event Latchup

- **Test Methodology**
  - High biases = core:1.05V, aux:2.75V, io: 3.45V
  - High LET ions, in vacuum to ensure adequate range
  - High fluences, greater than 10^8 ions/cm^2
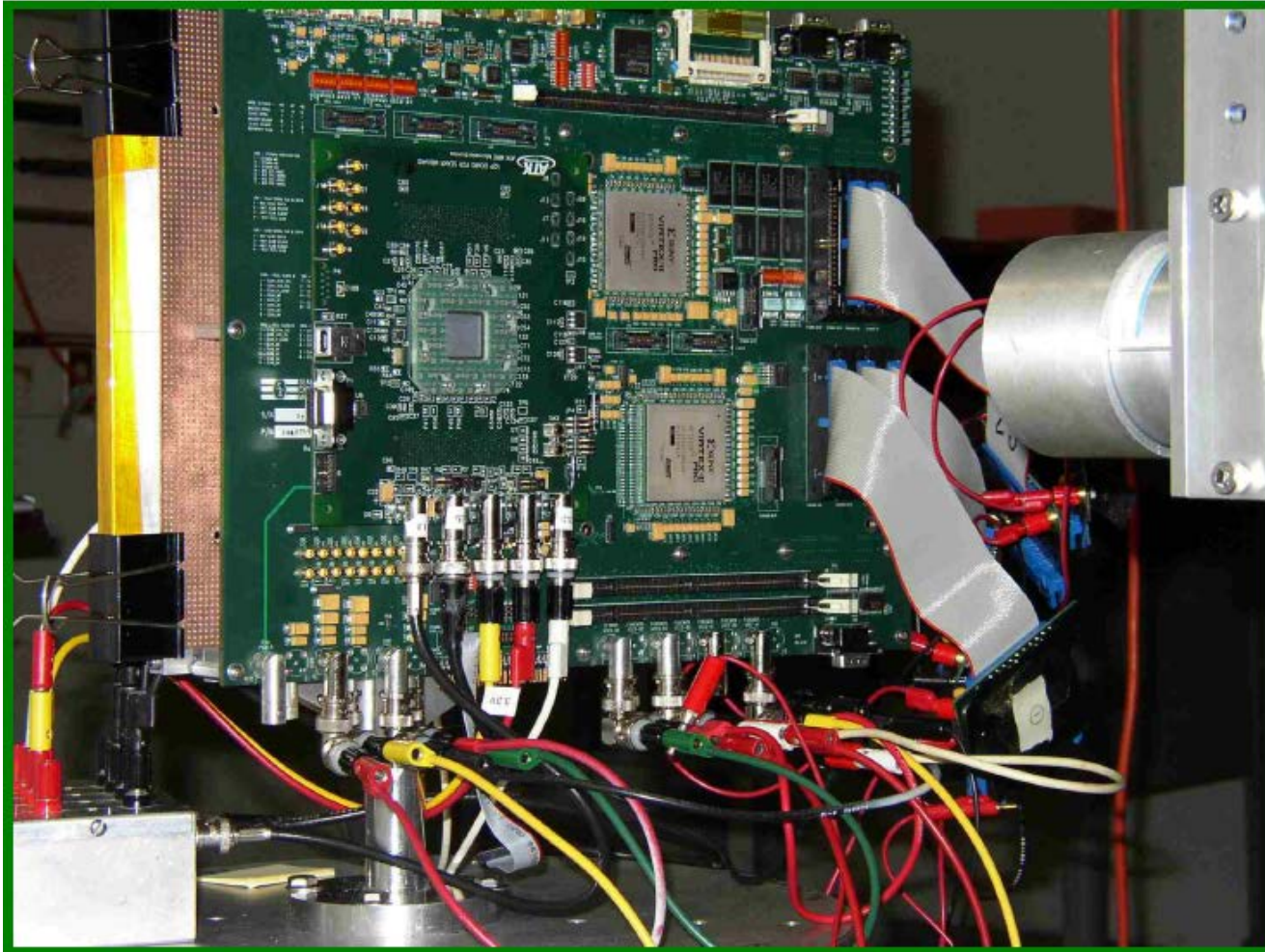 - High temperature using "self-heater" design + Heating Strips

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Consortium Test Setup

ReSpace/MAPLD 2011

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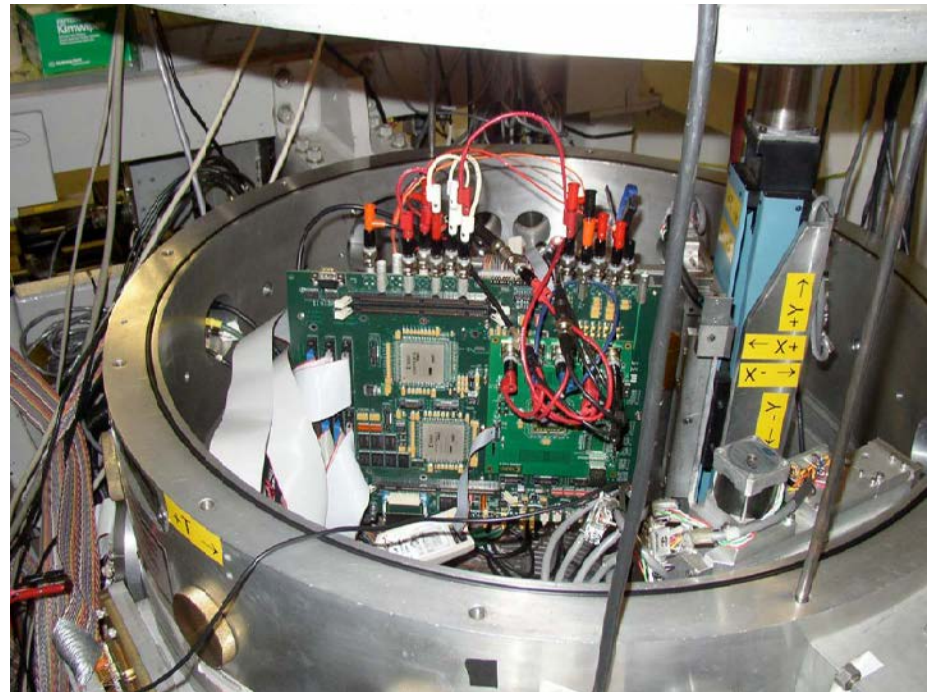
XRTC Test Setup

At Texas A&M Cyclotron:

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SEFI Taxonomy

- **"Baskets" of upsets whose signature is similar**

- **Design Intrusive SEFIs**
  - POR SEFI – main indicator is DONE pin goes off
  - Global Signal or GSIG SEFI – beam activation of a global signal, like reset

- **Visibility Loss SEFIs**
  - FAR SEFI – read and/or write and/or auto-increment of the configuration Frame Address Register doesn't work
  - SMAP SEFI – malfunction of the SELECT_MAP port that can read and write the configuration memory while the user design continues to operate

- **Fake SEFI**
  - Shutdown or SD SEFI – DONE drops but design operates and a "Startup" command restores the DONE signal

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Heavy Ion SEFI Results

Testing conducted at Texas A&M cyclotron in March and May 2010:
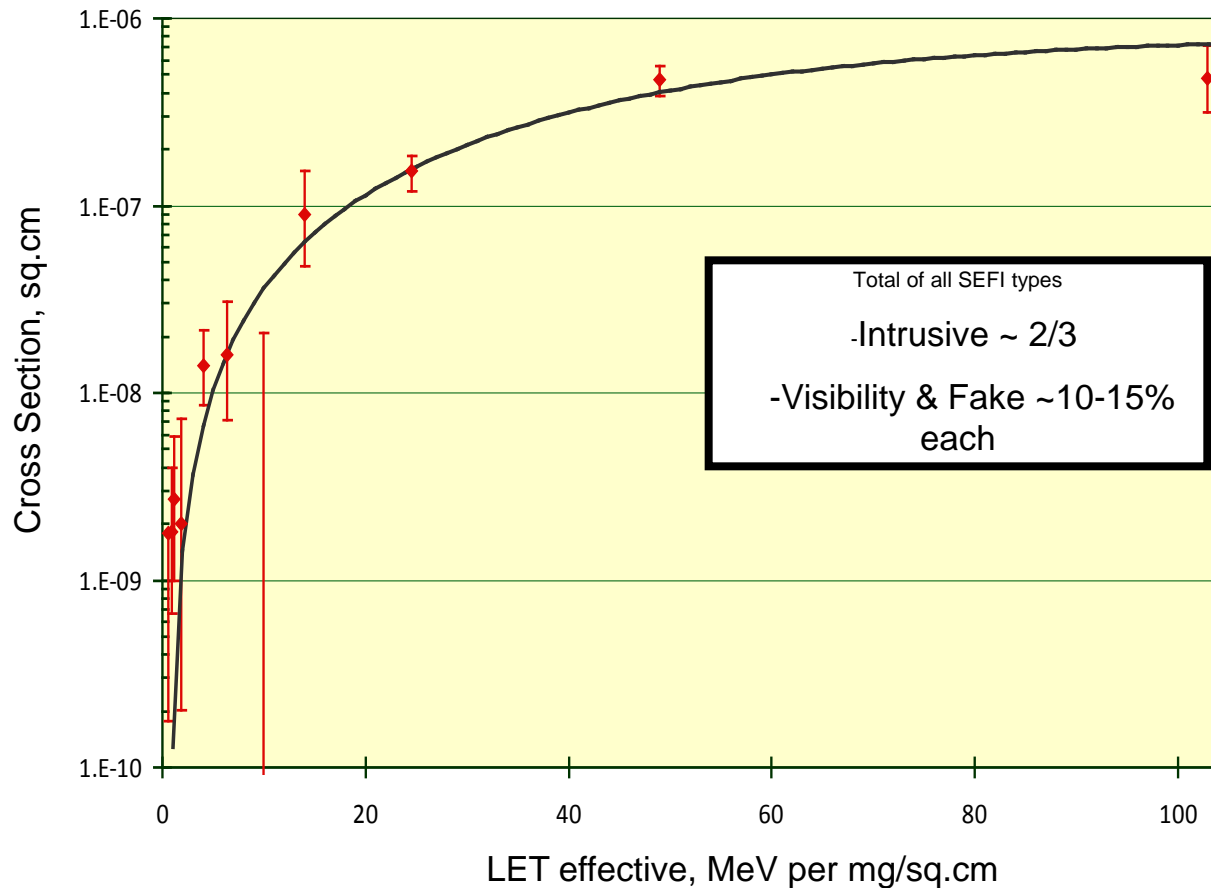
Proton SEFI Testing

- **Conducted at UC-Davis cyclotron in last month (June 2010) with 63 MeV protons**

- **A total of three samples were irradiated**
  - Total fluence of over 5×10^{13} protons per cm^2 and approximately two POR SEFIs were observed.
  - This is well over 10 Mrad(Si) of protons and is equivalent to hundreds of millions of years in LEO.

- **Low energy (1 MeV), in vacuum testing was performed to rule out direct ionization SEFIs and configuration upsets.**

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SEFI Conclusions

- **Test and rate calculations assume simple single-node upset mechanism**
  - Handy, because CRÈME-96 can calculate rates
  - Some measurements are high: TMRed registers (e.g., GSIG SEFI) where a flux dependence is introduced
  - Some low: dual-node registers (e.g., 18 SMAP configuration bits seen in fault injection) where particular grazing angles (not normal incidence) will contribute the most to the space rate

- **Extremely low susceptibilities make SEFI testing tedious and difficult; plus it consumes a large number of samples**

- **Proton results may be high due to "false" SEFI detections**
  - Definitive experimentation requires more upset-robust support equipment
  - Probably not worth the effort and beam time as heavy ions dominate the (very low) space SEFI rates

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Configuration Memory is …

1. **Approx. 34.1 million bits that control function and routing; they are key to the <u>reconfigurability advantage</u>: you can change (or fix) a design without h/w re-work or part replacement - even on orbit.**

   – Architecture allows reading & writing the "bitstream" <u>while</u> design runs

2. **Subject to both direct upset and indirect (or transient-induced)**

   – "Geometrically hardening" to greatly reduce direct upset susceptibility

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Configuration Memory Results

3. **From test chip data and Edmonds modeling/fitting, GEO rates:**

   – Direct-upset zeros: 5.3×10^{-11} upsets/bit-day (0.65 per device-year)

   – Direct-upset ones: 2.1×10^{-10} upsets/bit-day (2.6 per device-year)

   Single-node, CREME96-style estimation for SET-induced inadvertent writes to configuration cells:

   – Zeros-to-ones events: less one per five years

   – Ones-to-zeros: less one per year

4. **Essentially proton immune for direct upsets from reaction products as well as SET-induced writes.**

5. **Proton test indicative, not definitive; another test with more robust setup coming soon.**

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Non-Configuration Memory is …

1. **Approx. 4 million bits in the readback bitstream that do not control anything, but exist for testability and diagnostic reasons.**

    –   These bits don't control functionality so upsets have no effect

2. **Upset mainly via triggered capture(s) from a single-event transient**

    –   Transient location (leaf, branch or trunk) determines size of the resulting cluster of upsets (one or two, tens or hundreds,

    –   Also have a small <u>direct</u> upset susceptibility, similar to the configuration bits because they have identical geometrical hardening to upset

3. **Upset in GEO at a rate of less than one per month**

4. **Small proton susceptibility should be offset by reduction in heavy ions in lower orbits**

5. **To refine this, more heavy ion analysis and perhaps data is needed; more definitive proton data is needed.**

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User Flip-Flops are …

1. **81,920 bits of upset-hardened master-slave flip-flops for state machine implementation and user registers**

2. **Pretty hard to upset directly due to the geometric hardening. However, transients can sneak in clock and control lines (not data, in the static case) and create upsets.**

3. **Upset from SETs at about a rate 2×10^{-7} upsets per bit-day in GEO (200 MHz) or about 6 per device-year if all bits are used.**

4. **Some proton static SET susceptibility is possible based on LET threshold.**

5. **Definitive heavy ion tests, but no definitive proton tests yet.**

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User Block Memory (BRAMs) is …

1. 10.9 million bits of user memory organized as 298 blocks of 36k bits allowing massive on-chip storage and buffering.

2. Upset directly by ion strikes that hit collection nodes, as the cells are unhardened

3. Upsets both ones and zeros about the same with a rate of about 12.7 per device-day in GEO

4. Upset with such a low threshold LET that protons certainly contribute significantly to the total upset rate in proton-rich environments. However, upsets from ionization trail of protons is non-existant (or extremely rare)

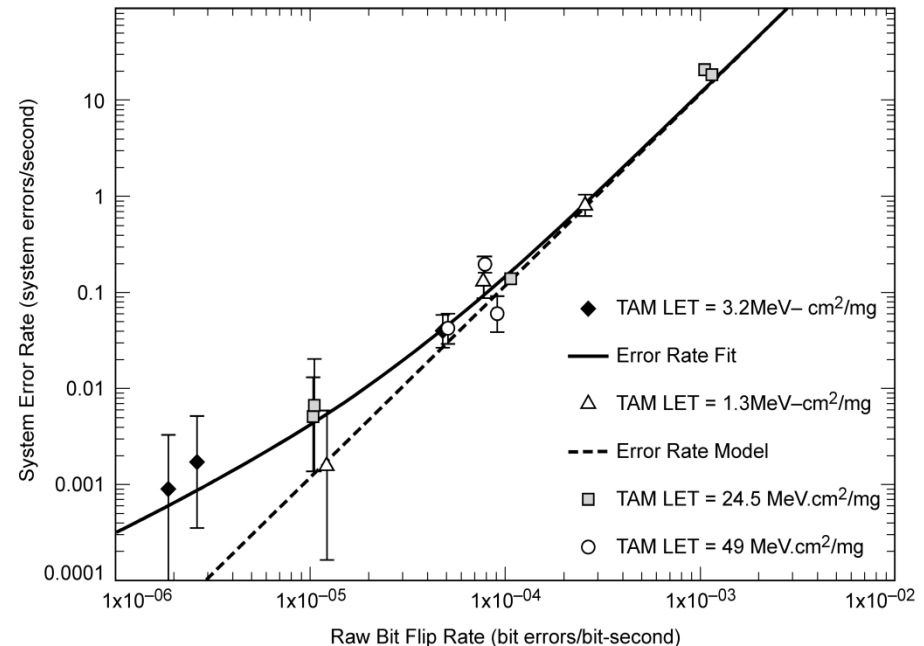5. Current results are definitive.

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BRAM EDAC Results

"…interleaved bits are spaced sufficiently enough apart, that the spacing in conjunction with the epitaxial layer should prevent a significant increase in the EWER at angle."

– Greg Allen, JPL

BRAM Cells Cross-Section versus Effective LET
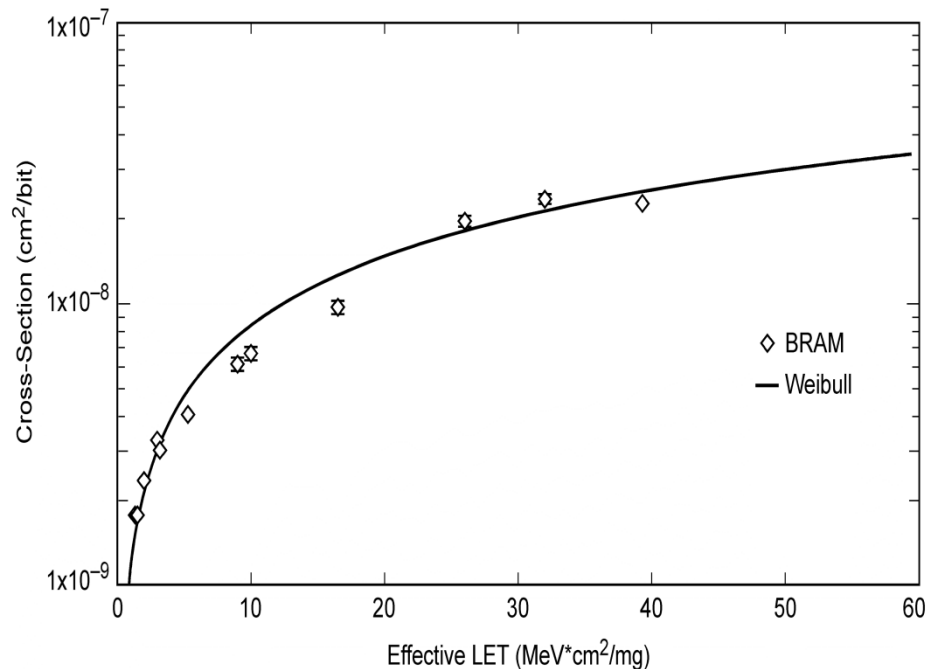
BRAM EDAC

First IODELAY Test

- **First IODELAY SEE experiment was performed at TAMU between July 29 and August 1, 2009**
  - Configure IODELAYs into a ring oscillator that outputted a 16Mz clock
    - Instantiated 58 ring oscillator instances in FX-1 device
    - Funcmon reference clock used to lock ring oscilators to 16Mhz
    - IODELAY Adjustment Circuitry uses FX1-1 CLB logic
    - Assumed low configuration bit error rate of FX-1 CLB RHBD cells
    - IODELAY ring oscillators automatically reset when errors detected
      - IODELAY Error counts logged in Funcmon FPGA
    - Instantiated 13 instances of IDELAYCTRL used to calibrate IODELAY's
      - - IDELAYCTRL 's automatically reset when errors detected
        - » - IDEALYCTRL Error counts logged in Funcmon FPGA
    - Needed to use DCM in FX-1 to create 200Mhz IDELAYCTRL reference clock
  - IODELAY Oscilloscope Test
    - Fed 200Mhz clock into first instance of IODELAY daisy chain
    - Routed last instance of IODELAY daisy chain to SMA connector
    - Instantiated 3 instances of IDELAYCTRL used to calibrate IODELAY's
    - Monitored 200MHz input clock and output of last IODELAY instance on oscilloscope

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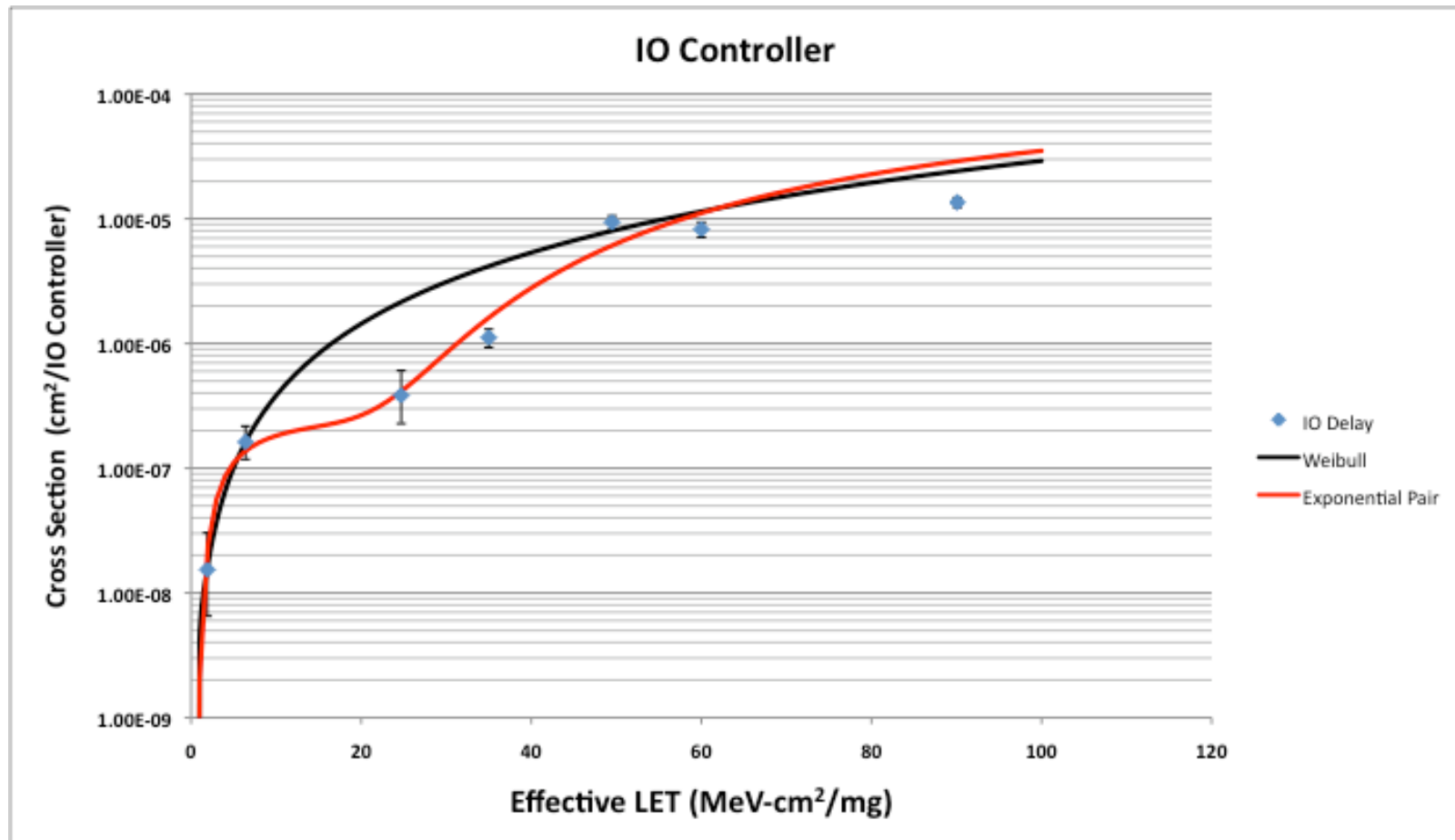
July 2009 Rate Estimates (GCR orbit)

- ## IO Delay:

  - Weibull
    - Best Estimate: 7.7e-5/IODelay-Day, or 2.8/IODelay-Century
    - Worst Case:1.1e-4/IODelay-Day, or ~4/IODelay-Century

  - Exponential
    - Best Estimate: 2.8e-5/IODelay-Day, or ~1/IODelay-Century
    - Worst Case:4.0e-5/IODelay-Day, or ~1.5/IODelay-Century

- ## IO Controller

  - Weibull
    - Best estimate:9.1e-6/IOController-day, or ~3 failures per IOController per 1000 years
    - Worst case: 1.8e-5/IOController-day, or ~7.5 failures per IOController per 1000 years

  - Exponential
    - Best Estimate: 7.14e-6/IOController-day, or ~2.6 failures per IOController per 1000 years
    - Worst case: 1.34e-5/IOController-day, or ~5 failures per IOController per 1000 years.

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