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Peeling the Onion: Understanding the Layers of Apparent Upsets in the Configuration Readback of the RHBD Virtex-5QV

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Outline

- Background
  - Device overview
  - Standard method of measuring SEU susceptibility and calculating rates
  - RHBD approaches
- Layer 1—Direct Upsets to Configuration Cells
  - Why standard test methodologies and analysis are no longer applicable
  - Different approaches to the problem
    - MC Simulation
    - Data, Data, Data…
    - Analytical Modeling and Data
- Layer 2/3—Single-Event Transient Induced Configuration Bit Flips
- Discussion and Results
- Conclusion

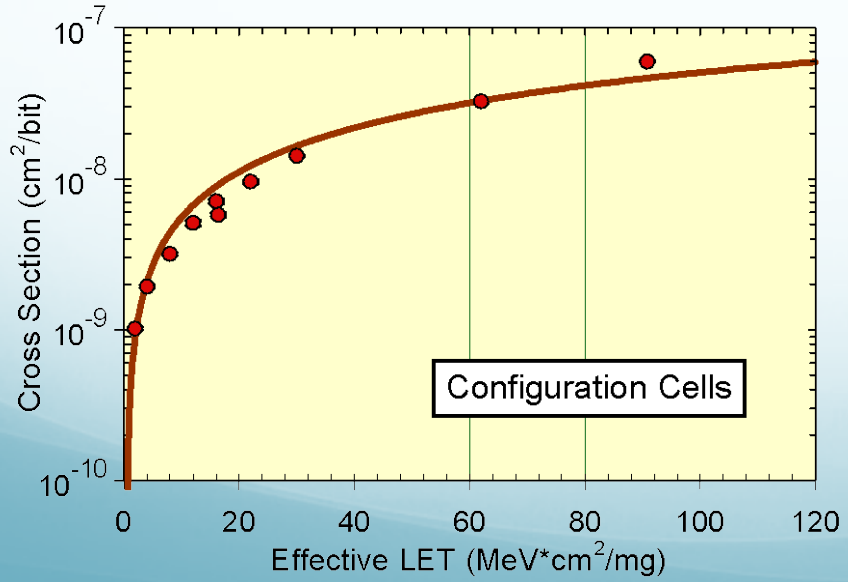
Device Overview

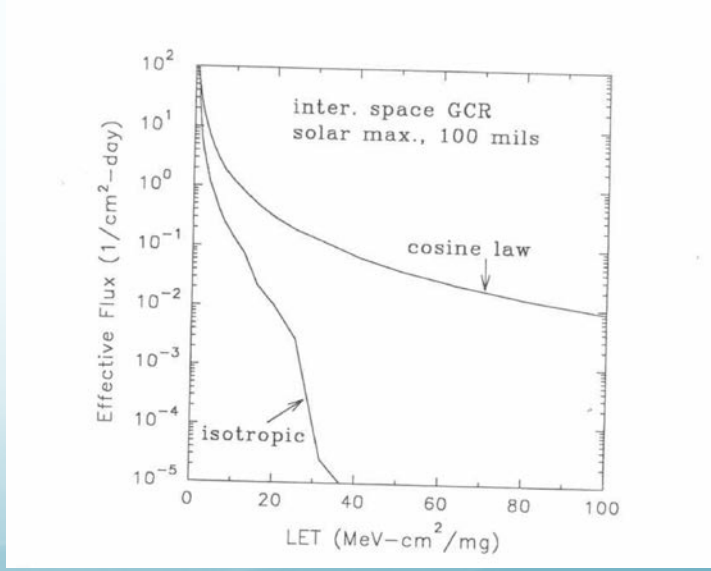
Functional Block	Available Resources	SEU Mitigation
Logic Cells	131,072	RHBD
6-Input LUTs, CLB-FFs	81,920	RHBD
Distributed RAM (kBit)	1,580	RHBD
BRAM Blocks (36 Bit)	29[illegible]	EDAC
Total BRAM (kBit)	10,368	EDAC
Clock Tiles	6 (4 PLL, 2 DCM)	None
DSP48E Slices	320	None
MGT-GTX Channels	18	None
PCI Express Blocks	3	None
Ethernet MACs	6	None
User IO (MGT)	836 (18)	None

CONFIGURATION BITS
~3E7

Space Rate Calculations

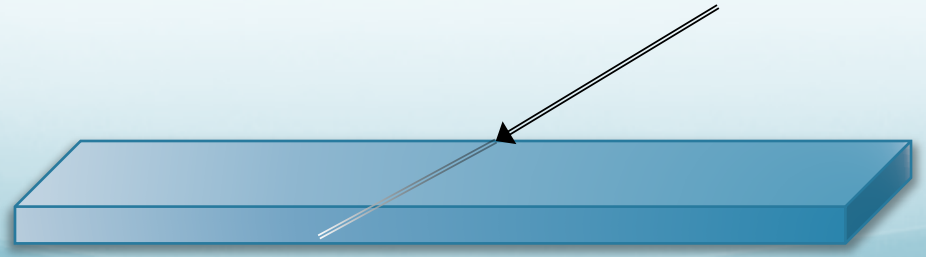
- What's needed to calculate a rate?
  - Susceptibility measurements—count ions and count events as a function of LET (or Energy)
  - Environmental description—how much of what LET do we expect to observe for a particular orbit or destination



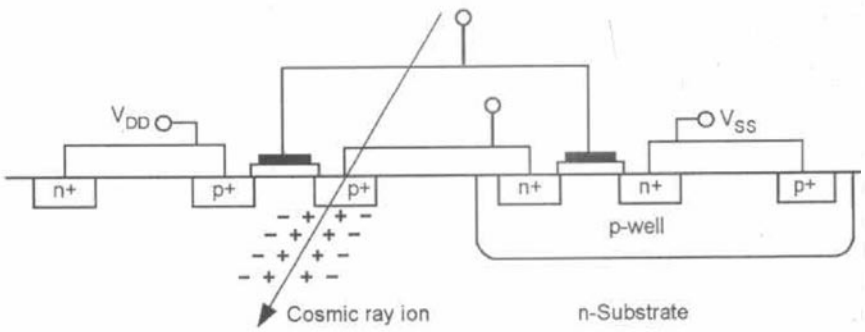


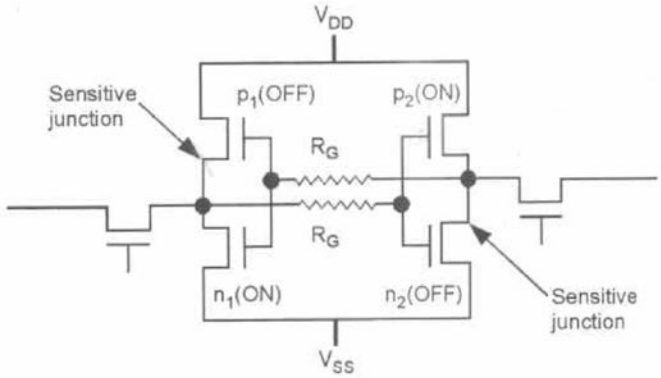
Space Rate Calculations

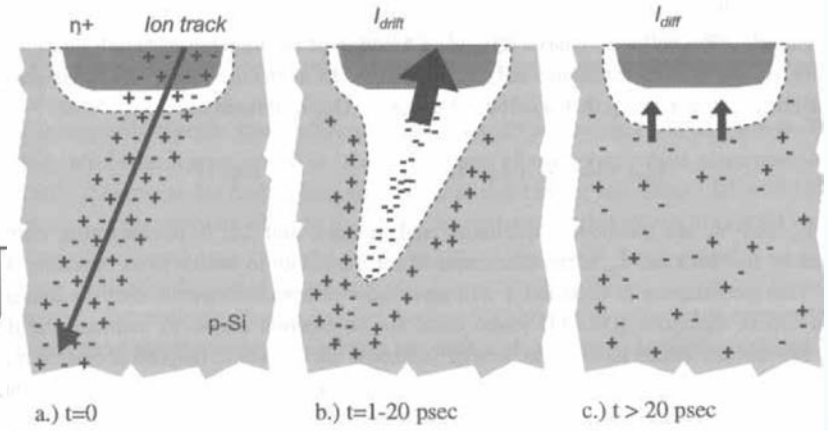
- What's needed to calculate a rate?
  - Charge Collection/angular response "sensitive volume" model—assumes charge collected from an ion track track at a device node equals the charge liberated by the track in some well-defined sensitive volume with that node
  - RPP Model typically used—a device is assumed to contain a collection of geometrically identical rectangular parallelepiped (RPP) shaped sensitive volumes with an associated critical charge

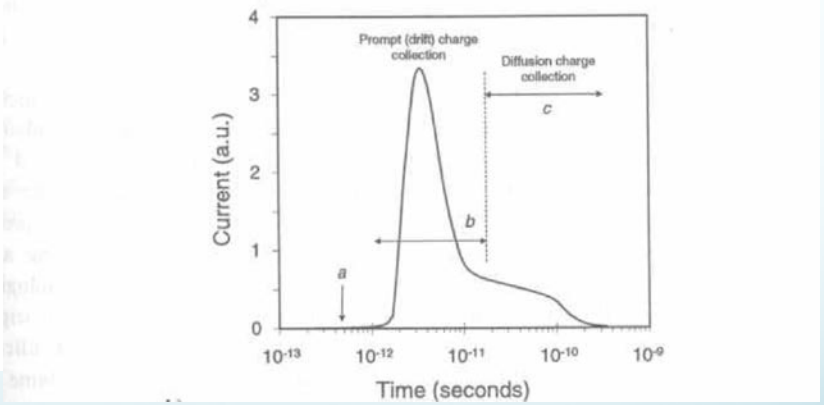


SEU in a standard SRAM









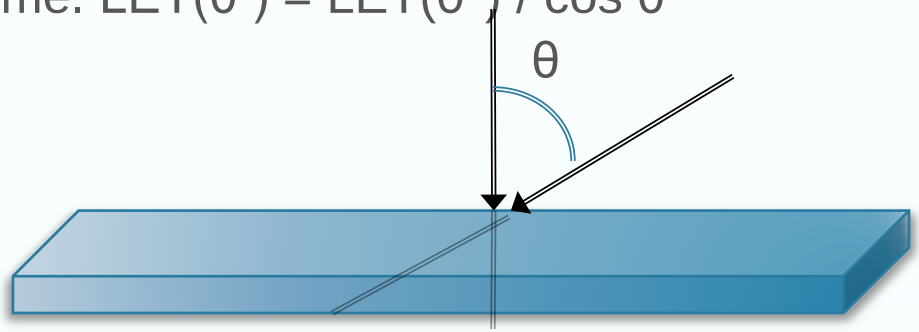
$$I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}})$$

$$\begin{cases} Q_{crit} = \int_0^{t_{th}} I_{drain}(t)dt \\ V = \frac{Q}{C} \end{cases}$$

$$V = \frac{1}{C}\int_0^{t_{th}} I_{drain}(t)dt$$

Simplifying Concepts

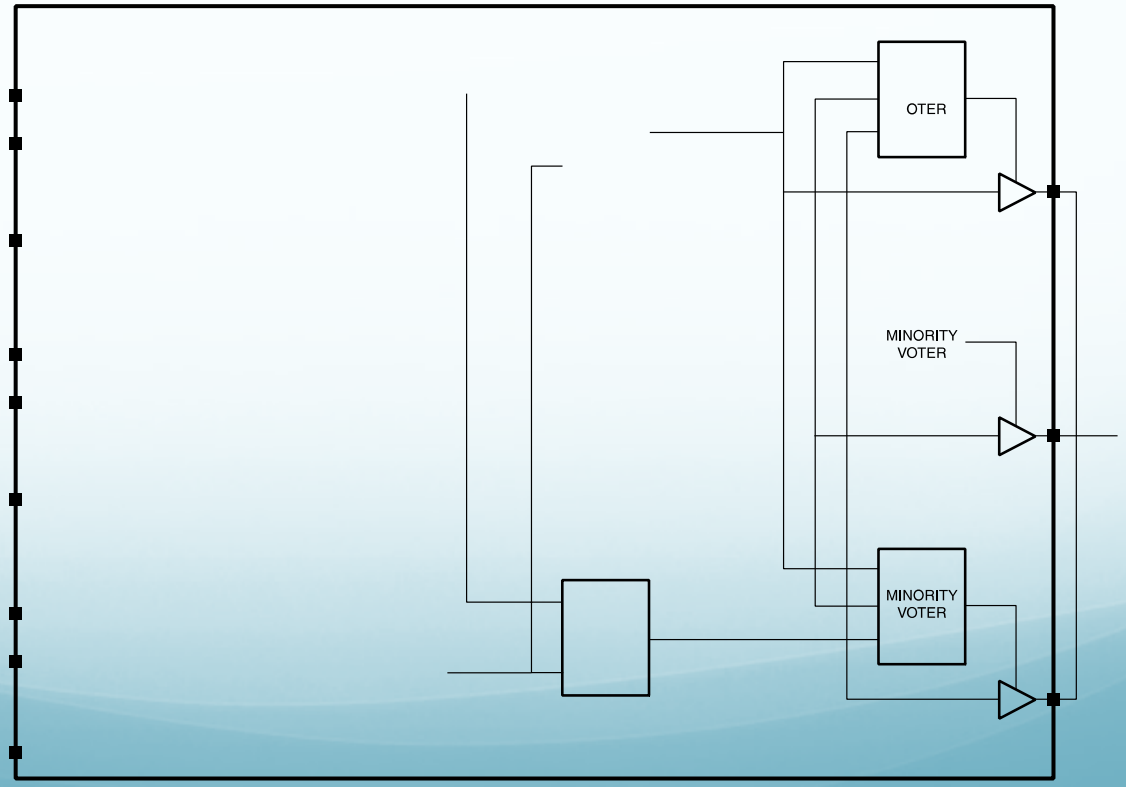
- Effective LET
  - The linear energy transfer (LET) modified to account for the change in total energy transferred from an incident ion as it traverses a sensitive volume when the path of the ion is not normal to the surface of that volume. LET(θ) = LET(0°) / cos θ



- Critical Charge
  - If a node collects more charge than the critical amount, the cell will upset
- RPP charge collection volume (a fitting tool)
  - All charge deposited in the RPP goes to the node, while all the charge outside does not

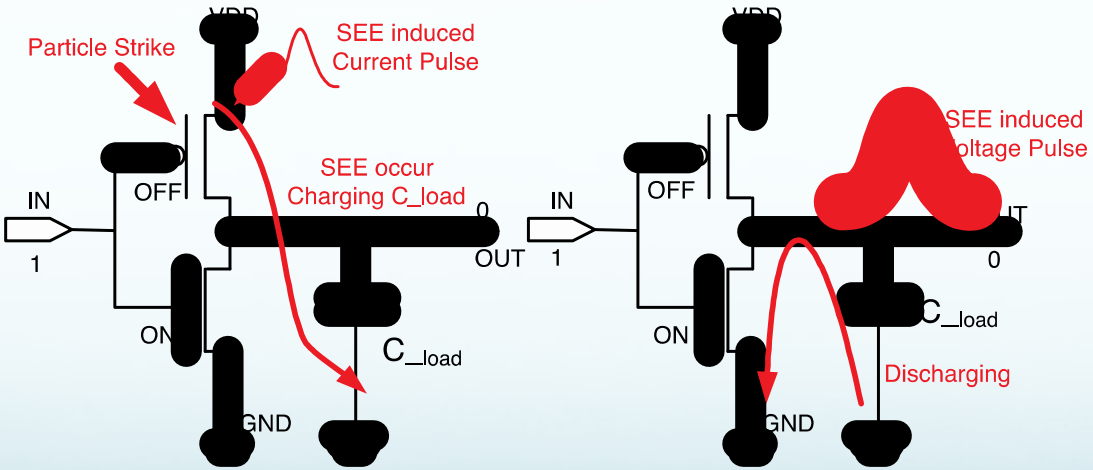
Soft Error Mitigation

- Can either implement prevention or recovery
  - Recovery: Fault tolerance (software), Redundancy (TMR, ECC/Parity, etc.)



Soft Error Mitigation

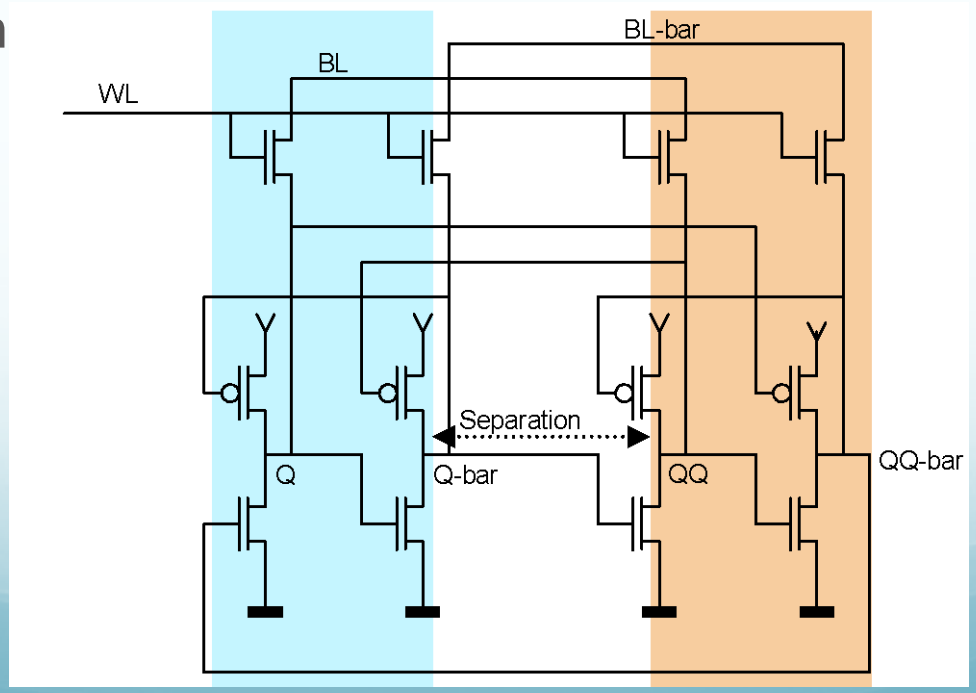
- Can either implement prevention or recovery
  - Prevention:
    - **Increase Q_{CRIT}: add passive elements to feedback path**



$$I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}\left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right)$$

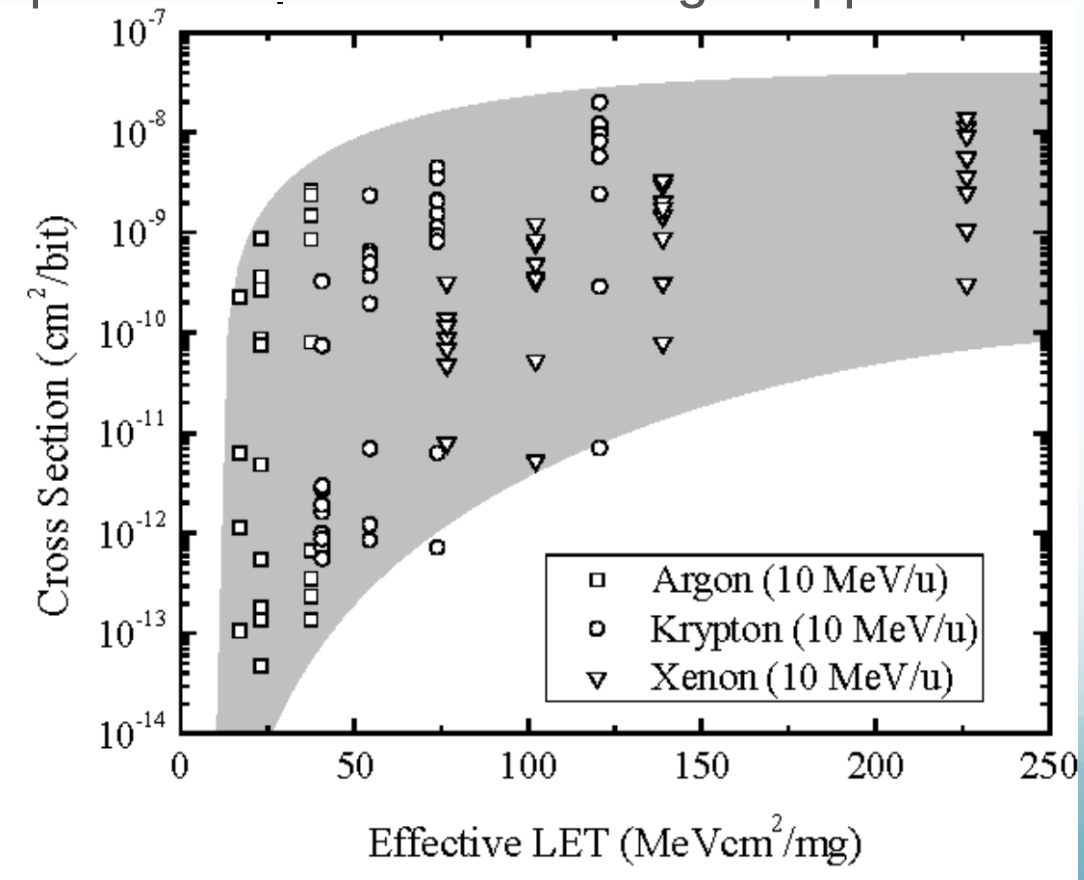
Soft Error Mitigation

- Can either implement prevention or recovery
  - Prevention:
    - Increase Q_{CRIT}: add passive elements to feedback path
    - **Add redundancy on the cell level—require charge deposition in two separate, spaced out sensitive volum**



Now what…?

- So we have a RHBD cell, how do we measure the SEU susceptibility?
  - Concept of effective LET no longer applies…



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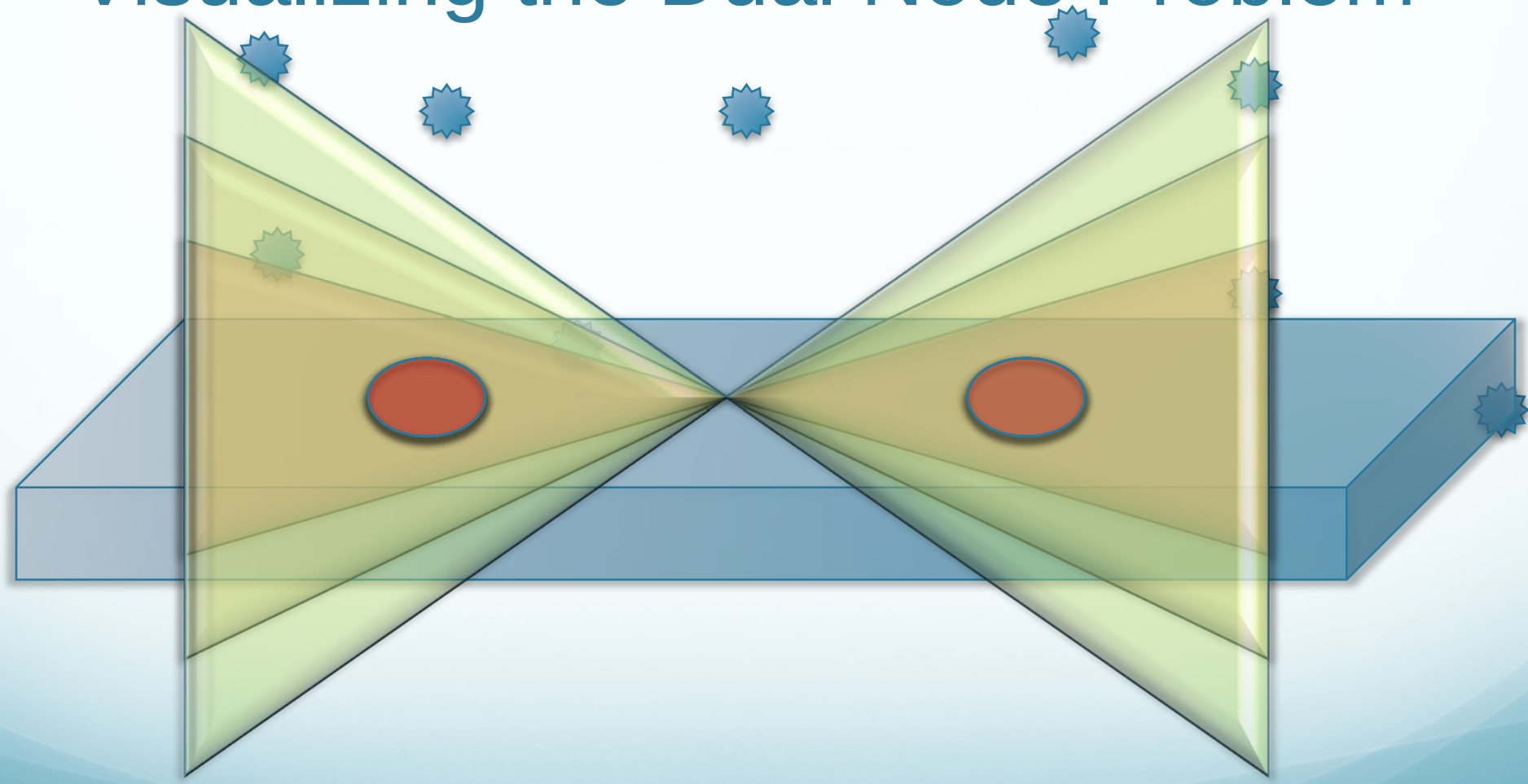
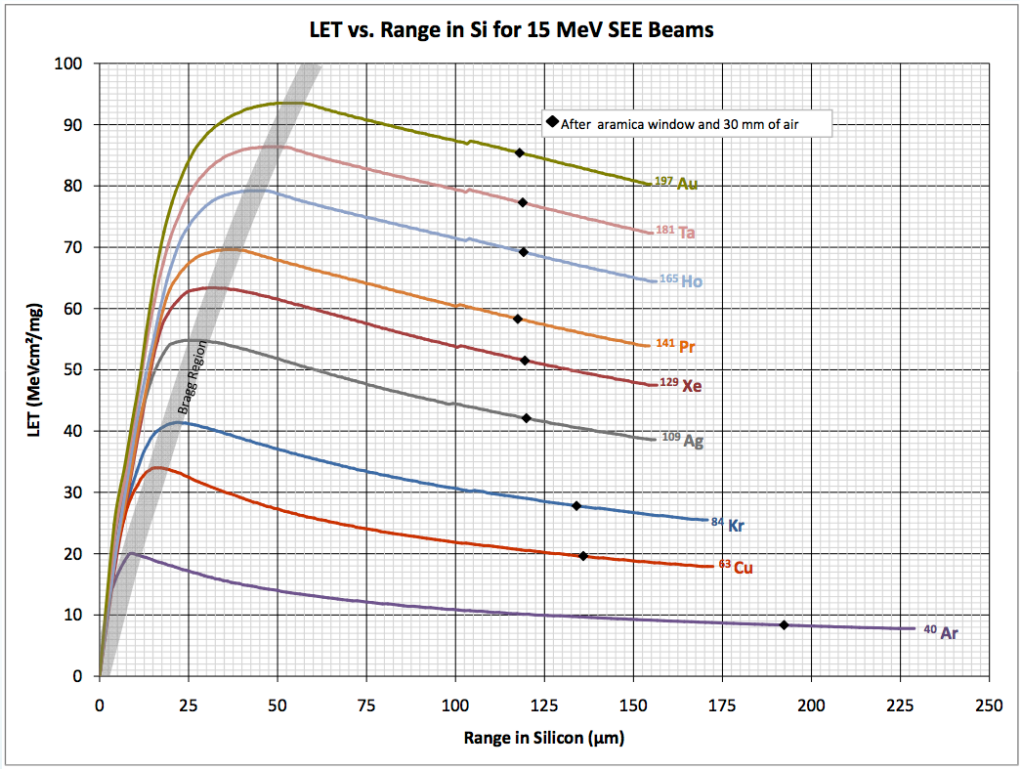
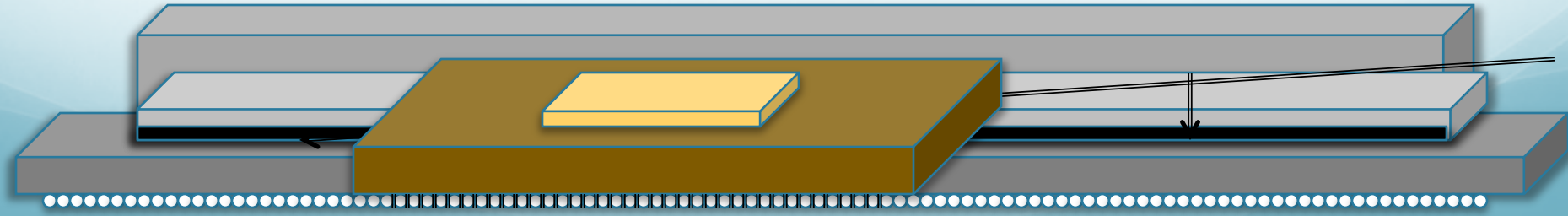
Visualizing the Dual Node Problem



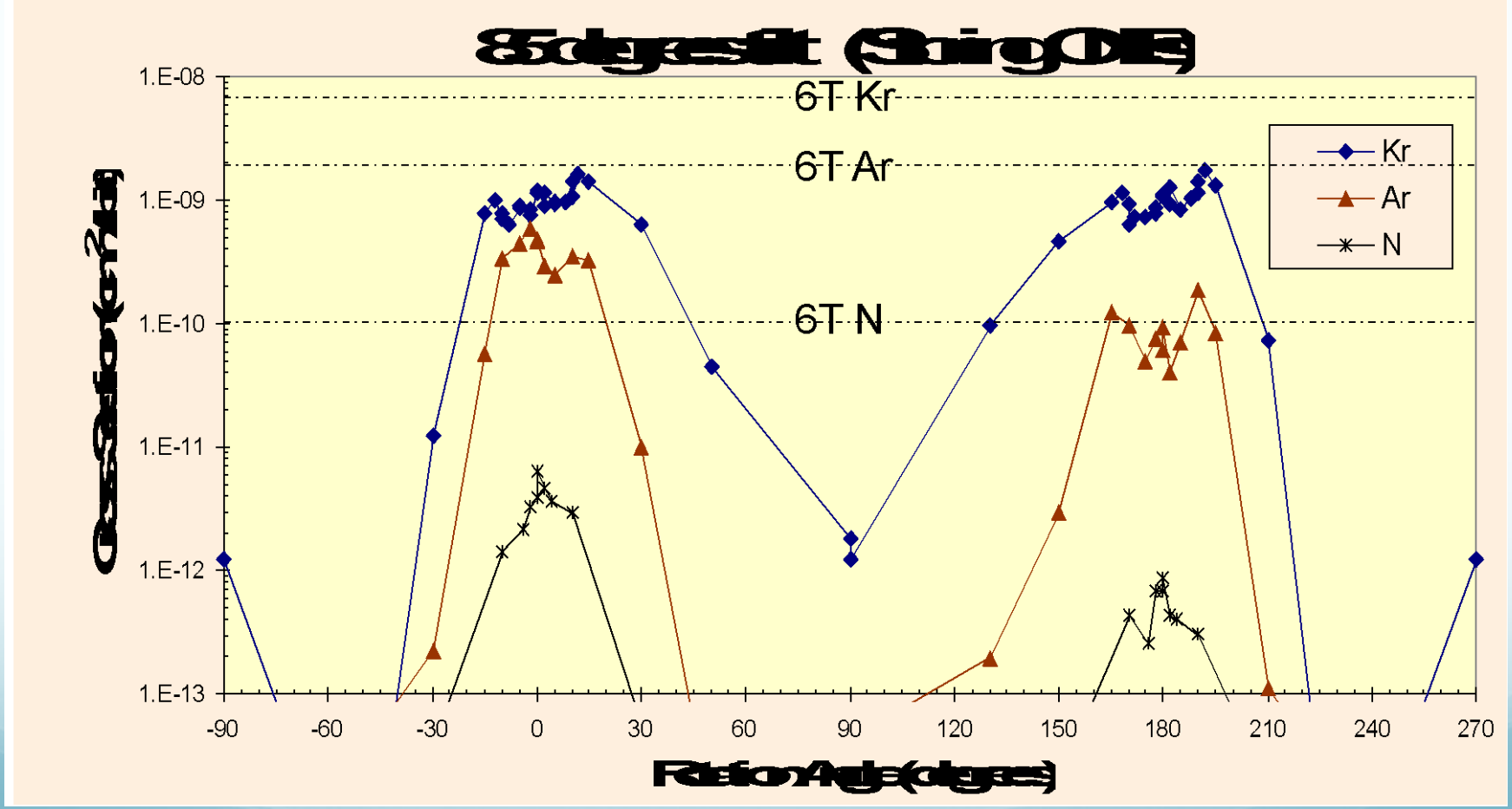
Taking data…

- Data taken on a test chip due to limited ion range at high angle on the flip chip FPGAs (usually thinned to 100um, but at angle we are severely limited).





Sample Results

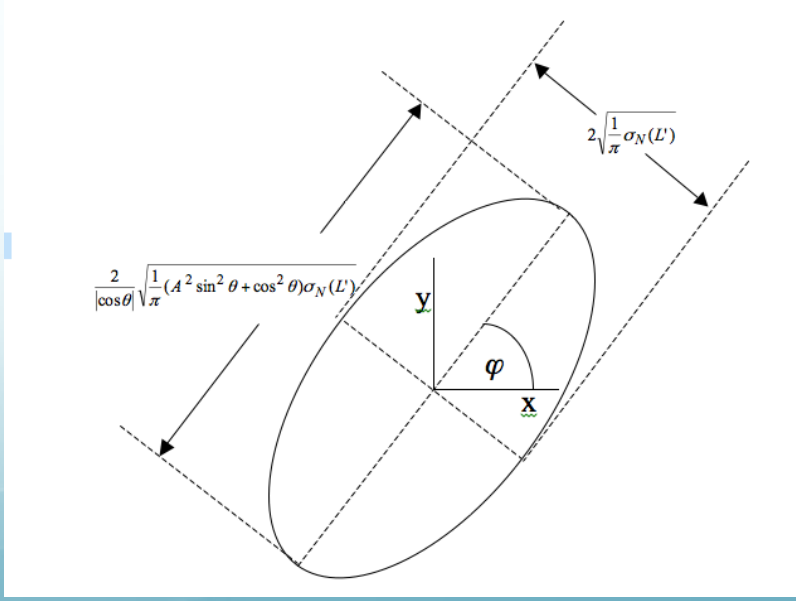


Options…

- Monte Carlo Simulation
  - TCAD/SPICE, GEANT 4, radiation environment models, etc.
- Brute force method
  - The brute-force method numerically integrates measured data without any benefits from physical models
- Fit data to a beam alignment measurement
  - This method is a data fitting method. However, the curve fit is not derived from a proposed physical model. Instead, it is derived from a fairly lenient assumption that is expected to apply (roughly) to a variety of physical models, at least for devices exhibiting simple trends as discussed under the brute-force method.
- Fit data to a physical model
  - This method is another data fitting method, but in this case the curve fit is derived from a proposed device-physics model

Fitting the data to a model

- Start with a charge collection efficiency model
  - Assume each node has a charge collection efficiency function dependent both on the physical construction of the node in question and surrounding structures
  - Ellipsoid was used for simplification of analytical computations $A^2x^2 + B^2y^2 + z^2 = \text{constant}$ (defines a constant-Ω surface)
  - Expand this to a dual node model with a definable geometric relationship



End up with this…

- The fitting parameters are φ_{off}, A, B, $L_{0,1}$, $L_{0,2}$, $\sigma_{0,1}$, $\sigma_{0,2}$, P, T, and h
- The arguments at which the directional cross section is evaluated are L, θ, and φ_{data}

$$\varphi = \varphi_{off} + \varphi_{data}$$

$$\alpha(\theta,\varphi) \equiv \sqrt{\left(A^2\cos^2\varphi + B^2\sin^2\varphi\right)\sin^2\theta + \cos^2\theta}$$

$$\sigma_1(L,\theta,\varphi) = \sigma_{0,1}\,\alpha(\theta,\varphi)\exp\left(-\left[\frac{L_{0,1}\,\alpha(\theta,\varphi)}{L}\right]^P\right)$$

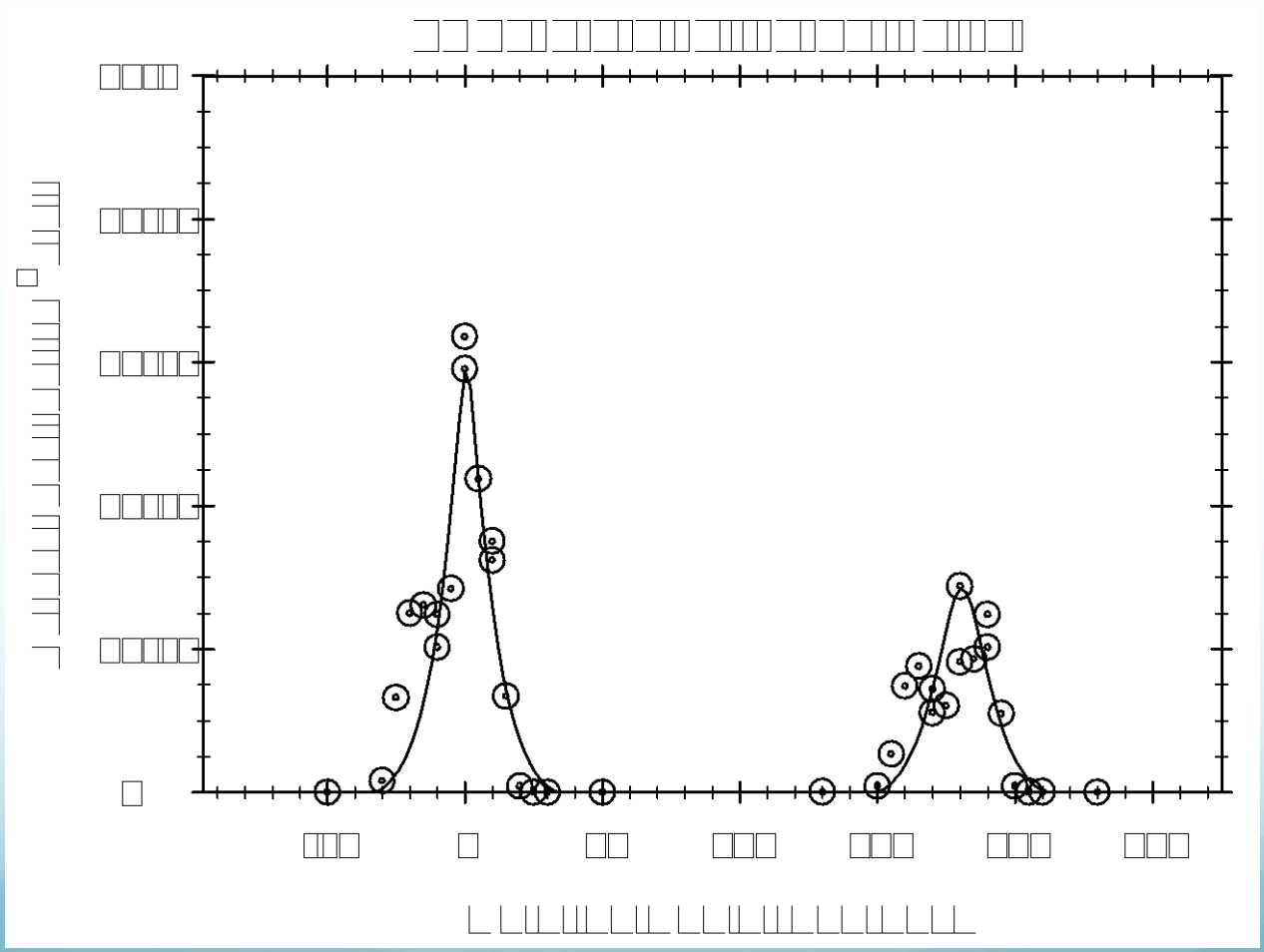
$$\sigma_2(L,\theta,\varphi) = \sigma_{0,2}\,\alpha(\theta,\varphi)\exp\left(-\left[\frac{L_{0,2}\,\alpha(\theta,\varphi)}{L}\right]^P\right).$$

$$R_1(L,\theta,\varphi) \equiv \left[\frac{\sigma_1(L,\theta,\varphi)}{\pi}\right]^{1/2}, \quad R_2(L,\theta,\varphi) \equiv \left[\frac{\sigma_2(L,\theta,\varphi)}{\pi}\right]^{1/2}.$$

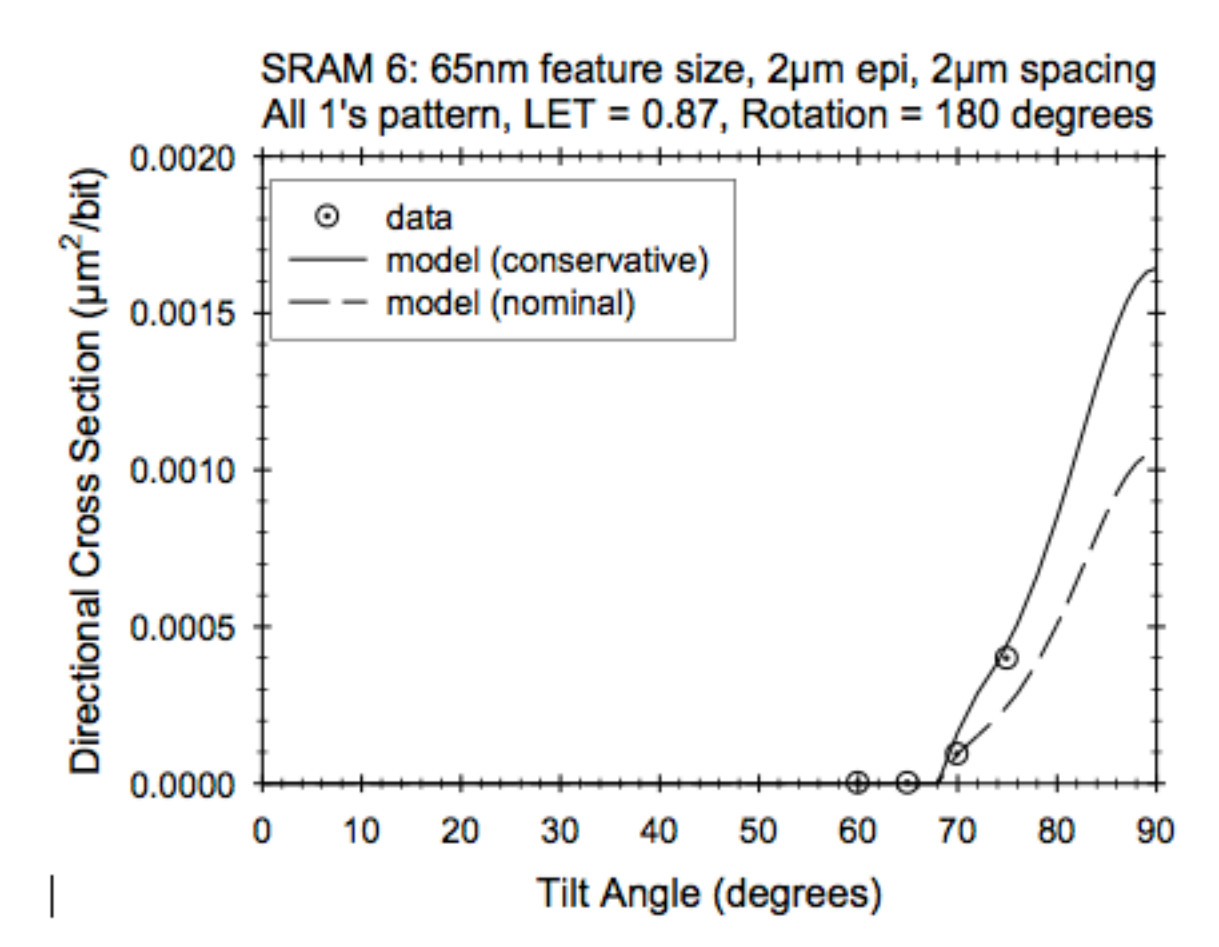
$$D(\theta,\varphi) = \left[\frac{\alpha^2(\theta,\varphi) - \cos^2\theta}{A\,B\,\alpha(\theta,\varphi)}h^2 + \frac{2A}{B\,\alpha(\theta,\varphi)}\cos\theta\sin\theta\cos\varphi\,h\,T + \frac{A}{B\,\alpha(\theta,\varphi)}\left(B^2\sin^2\theta\sin^2\varphi + \cos^2\theta\right)T^2\right]^{1/2}$$

$$\sigma(L,\theta,\varphi) = I\left(R_1(L,\theta,\varphi), R_2(L,\theta,\varphi), D(\theta,\varphi)\right)$$

Fitting the model to data…



Extrapolation is Necessary…



Test Chip Analysis

- Fitting parameters for zero and one bit flips were defined
- A rate of 4.2×10^{-11} /bit-day was calculated in GCR (solar min) behind 100mils Al. for zero->one bit flips and 2.05×10^{-10} /bit-day for one->zero bit flips
- Directional average cross sections were calculated and Weibull parameters fit for standard CREME96 calculations (to be provided in a later publication). Recall that the directional-average cross section has the directional dependence of device susceptibility already built into it, so this cross section is integrated with a raw (meaning that no directional effects are built into it) heavy-ion flux (as a function of LET) to obtain the upset rate. The rate calculation is the same calculation that would be used if device susceptibility were isotropic. Therefore, the rate calculation that uses this curve should reflect an isotropic device. CREME96 uses the RPP model for rate calculations, so RPP dimensions should be chosen to represent an isotropic device. This is done by selecting the RPPs to be cubes (i.e., all three RPP dimensions are equal), which are not perfectly isotropic but are as close to isotropic as the RPP model can be.

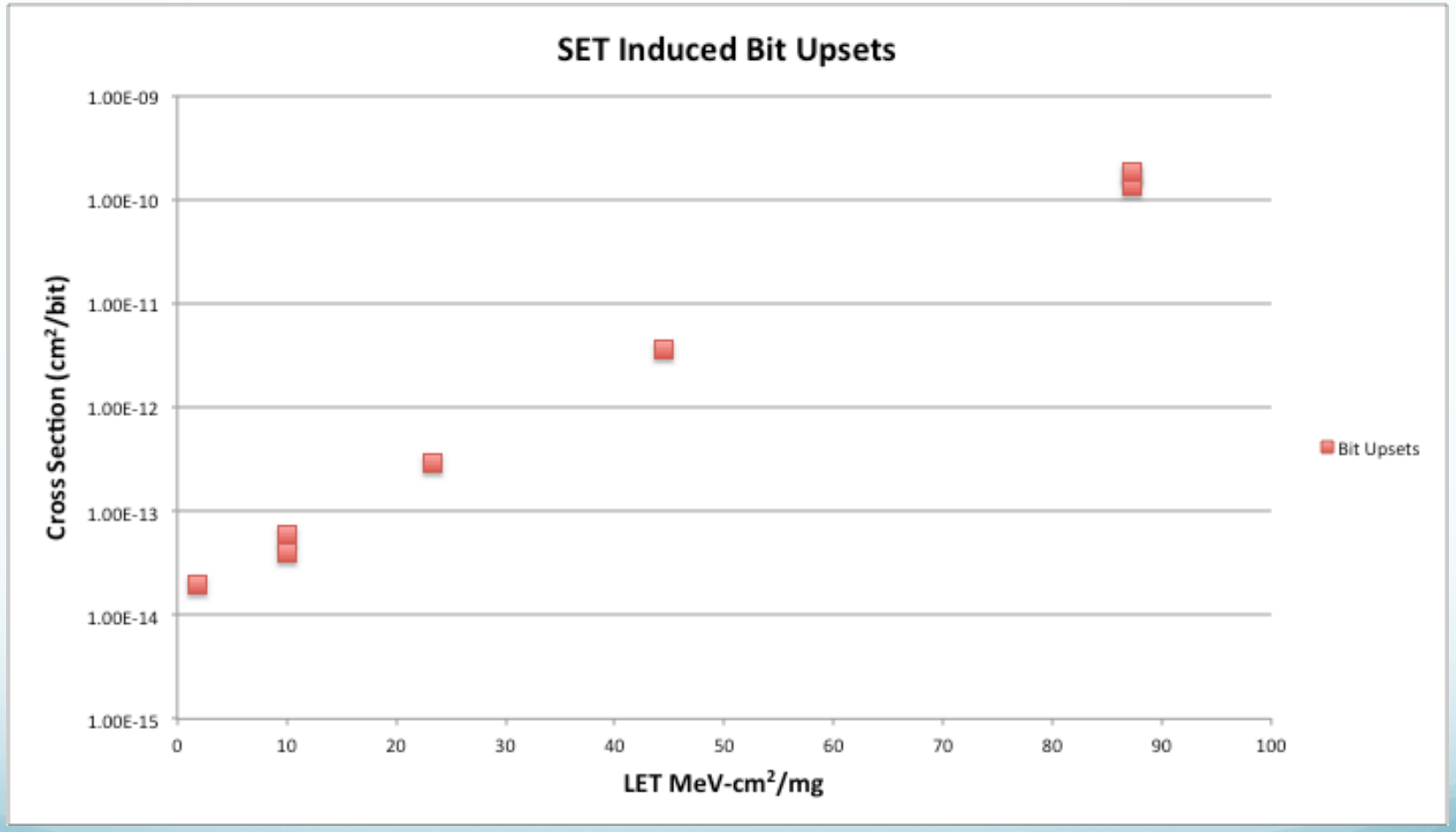
Comparison to actual FPGA—Peeling back the layers

- Direct upsets on the dual node cells
- SET Induced Initialization and Capture bit flips (masked out)
- “Lightly loaded” address line (asynchronous write commands) bit flips

SET Induced Bit Flips

- Capture and Initialization cell upsets
  - Cells are innocuous to the design, not used to route or control anything
  - However, if not masked out, will cause “erroneous” readback errors
- SET Induced writes to real configuration cells
  - SET on asynchronous control lines (e.g. reset or write signals) induce bit flips on certain groups of configuration cells that

SET Induced Bit Flips



- 4.8×10^{-11} SET induced upsets per bit-day
- ~1 configuration upset per device per 2 years

Conclusions

- JPL developed model under contract from Xilinx; will be published and reviewed by community
- Many layers to the “onion” that will fold into the overall system error rate estimation, and various error modes that designers need to be aware of
- Did not observe upsets due to protons on the test chip. Confirmation to take place on the final FPGA