ReSpace/MAPLD 2011 Presentation

Sandia Rad-Hard, Fast-Turn Structured ASIC

The ViArray

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NNSA National Nuclear Security Administration

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Outline

- Motivation of ViArray development
- ViArray architecture and platforms
- ViArray features
- Trusted ViArray
- Future direction
- Conclusion

Motivation of ViArray Development

- Sandia's Microelectronics Program provides high-reliability, radiation-hardened Application Specific Integrated Circuits (ASICs) for system applications. Typical customer has
  - Multi-year development program with spiral design process
  - Low-volume production requirement, if any
- The schedule to design, layout, fabricate and package a cell-based ASIC is long, and the development cost is escalating.

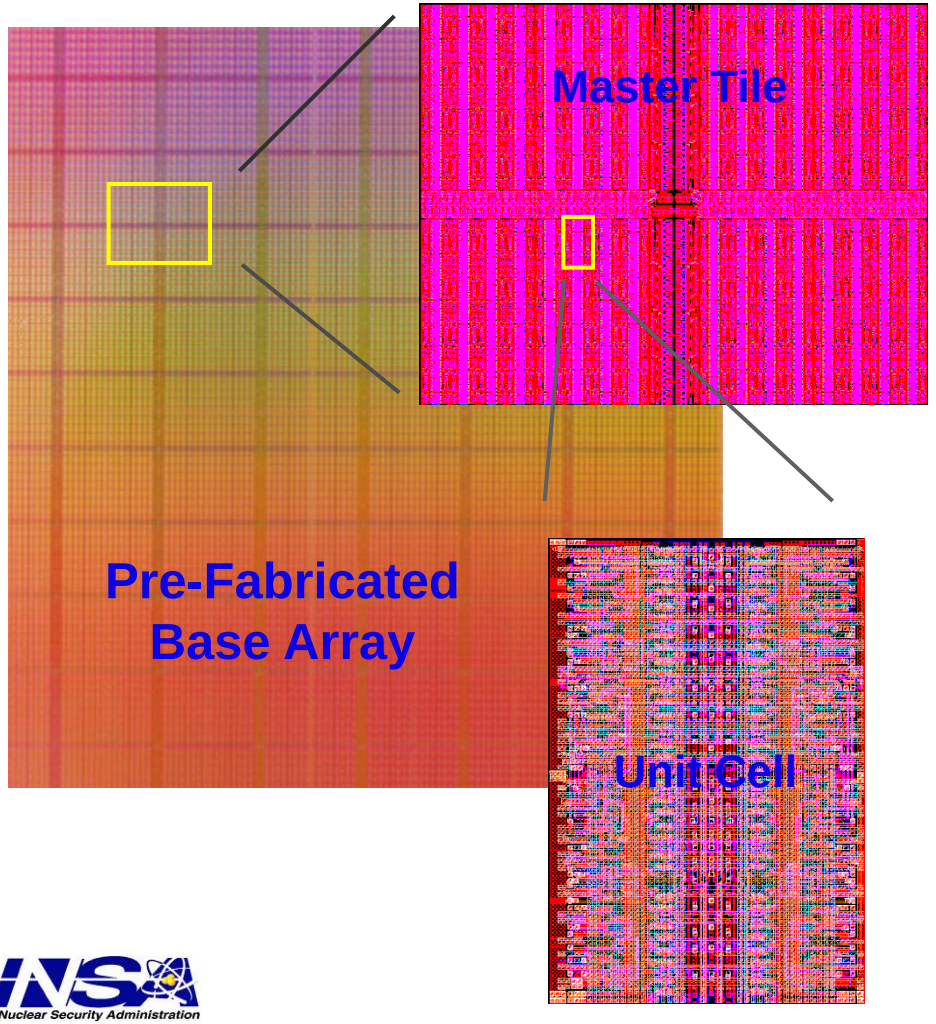
⇒ **Designers using FPGAs for design iterations**

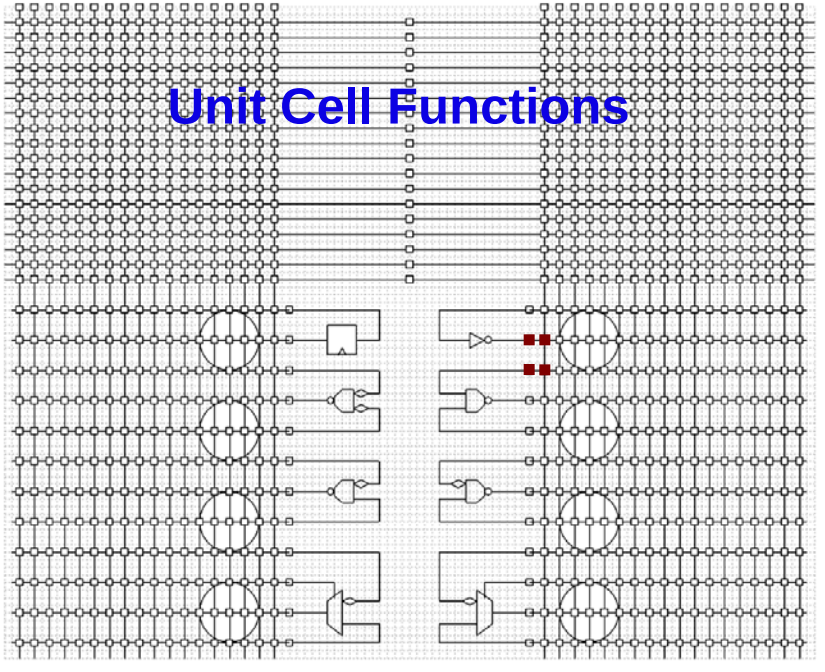
⇒ **FPGA to ASIC conversion issues**

We need a faster and cheaper way to design and develop ASICs

ViArray Architecture

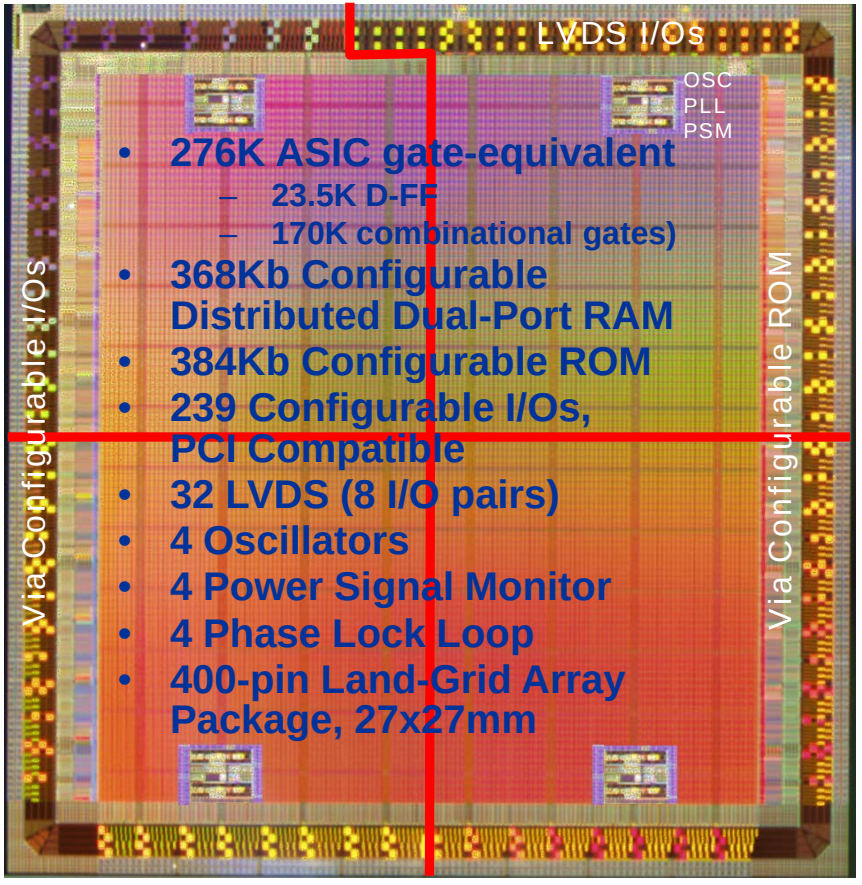
- Structured architecture
- Pre-fabricated base-array of repetitive functional fabrics
- Pre-determined vertical and horizontal signal routing channels
- One-mask metal-via configuration based on ViASIC® ViaMask™





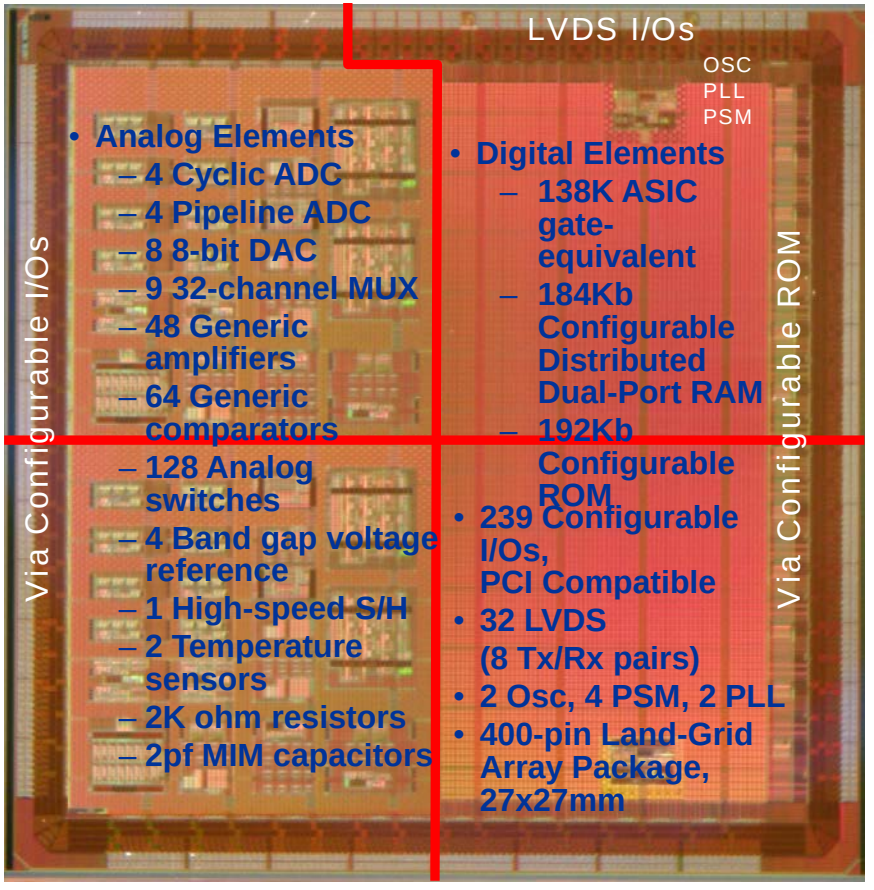
ViArray Platforms

Eiger
– A Digital ViArray Platform



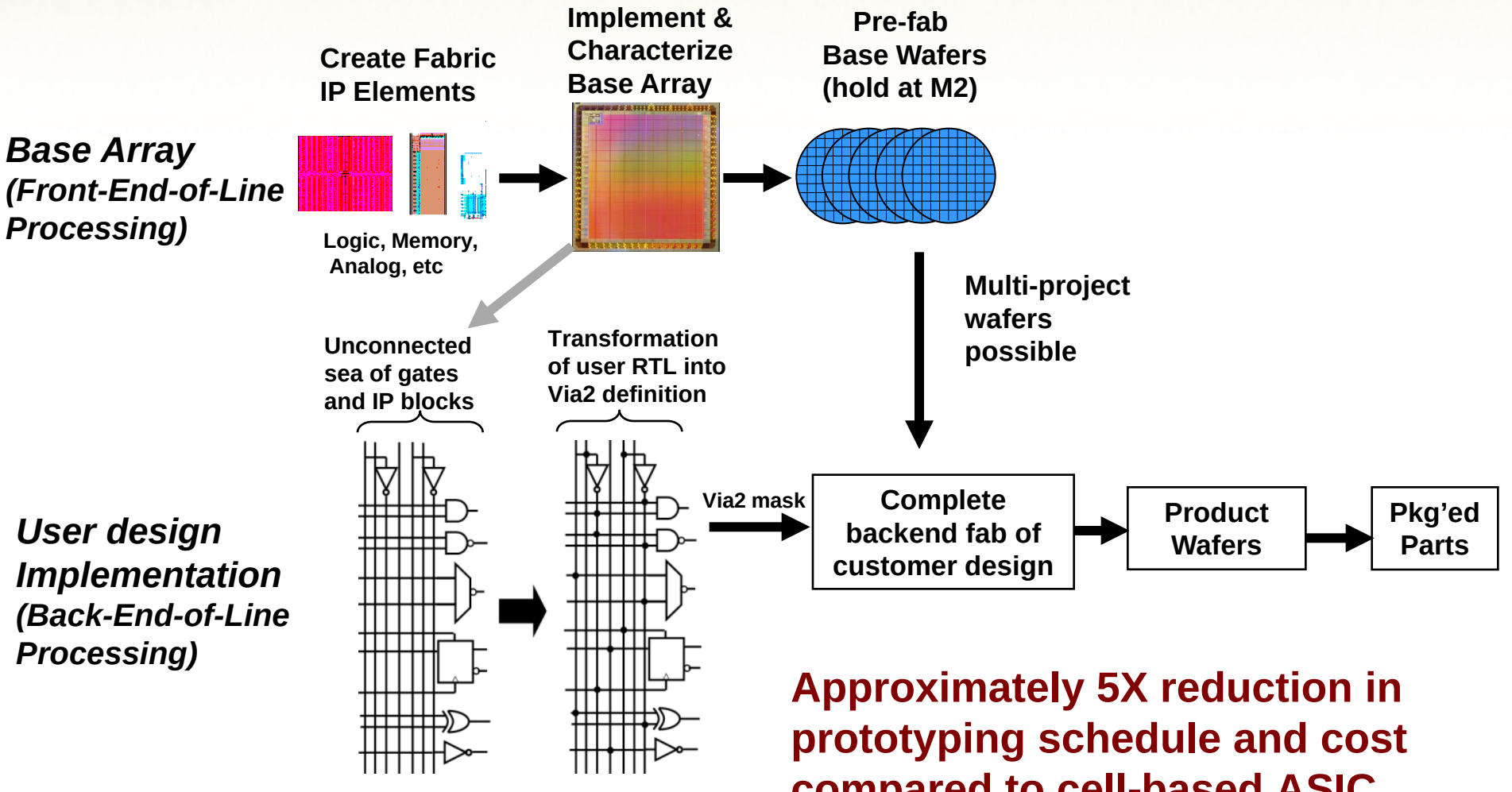
- 276K ASIC gate-equivalent
  - 23.5K D-FF
  - 170K combinational gates)
- 368Kb Configurable Distributed Dual-Port RAM
- 384Kb Configurable ROM
- 239 Configurable I/Os, PCI Compatible
- 32 LVDS (8 I/O pairs)
- 4 Oscillators
- 4 Power Signal Monitor
- 4 Phase Lock Loop
- 400-pin Land-Grid Array Package, 27x27mm

Whistler
– A Mixed-Signal ViArray Platform



- Analog Elements
  - 4 Cyclic ADC
  - 4 Pipeline ADC
  - 8 8-bit DAC
  - 9 32-channel MUX
  - 48 Generic amplifiers
  - 64 Generic comparators
  - 128 Analog switches
  - 4 Band gap voltage reference
  - 1 High-speed S/H
  - 2 Temperature sensors
  - 2K ohm resistors
  - 2pf MIM capacitors
- Digital Elements
  - 138K ASIC gate-equivalent
  - 184Kb Configurable Distributed Dual-Port RAM
  - 192Kb Configurable ROM
- 239 Configurable I/Os, PCI Compatible
- 32 LVDS (8 Tx/Rx pairs)
- 2 Osc, 4 PSM, 2 PLL
- 400-pin Land-Grid Array Package, 27x27mm

ViArray Implementation Flow



Approximately 5X reduction in prototyping schedule and cost compared to cell-based ASIC approach

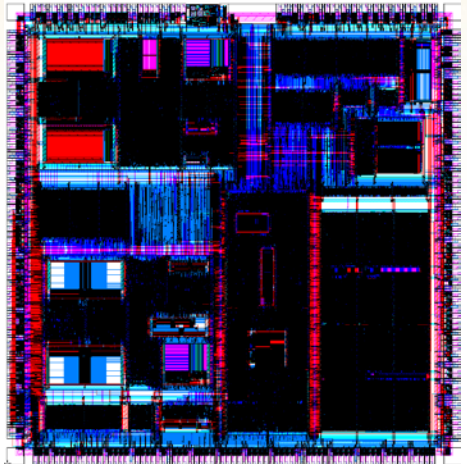
ViArray vs. Cell-based ASIC Comparison – Speed

ViArray Operating Speed

- For pipelined logic circuits with no static random access memories (SRAMs)
  - up to 100 MHz
- For pipelined logic circuits with SRAM
  - Up to 50 MHz

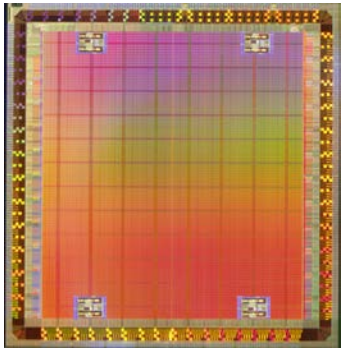
- Cell-based ASIC and ViArray have comparable speed because they have similar cell performance
- It is possible to operate at a higher speed with highly customized ASIC design

Cell-based ASIC vs. ViArray Comparison – Density



Typical Sandia CMOS7 0.35 μm rad-hard SOI cell-based ASIC density

- **Logic: 8K – 10K gate equivalent per mm^2**

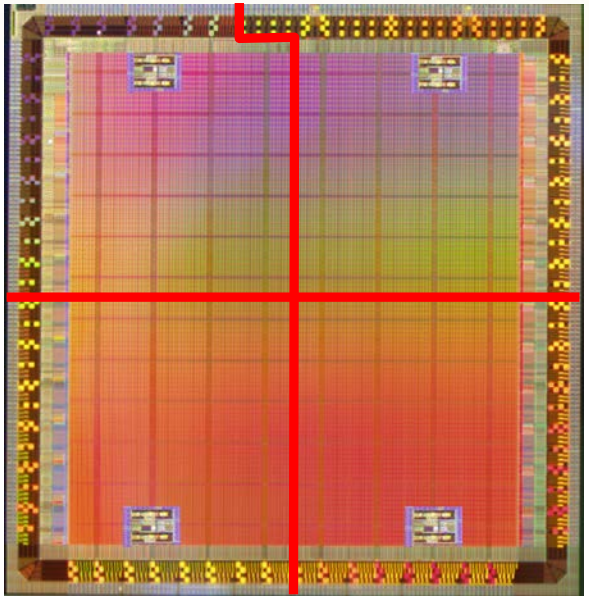


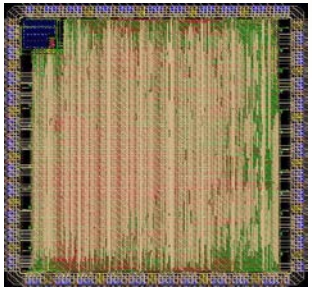
Sandia CMOS7 0.35 μm rad-hard SOI Eiger ViArray density

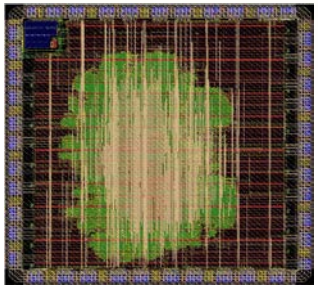
- **3.1K gate equivalent + 4.1Kbits Distributed DP RAM per mm^2**

Cell-based ASIC and ViArray have comparable transistor density

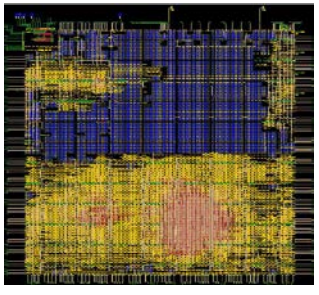
ViArray Power Management Features – Power Partitioning

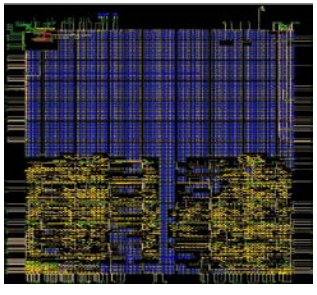






Examples

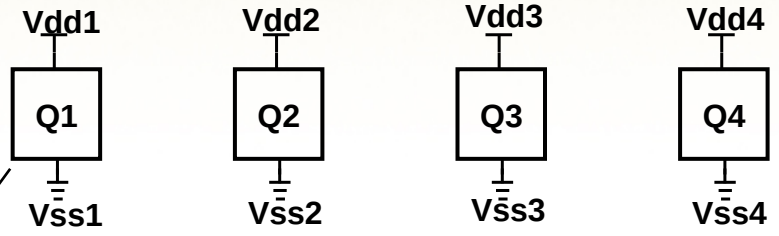




- **Partitioned Vdd enables**
  - **Power sequencing**
  - **Redundancy**
  - **Sleep-mode operation**
  - **Multiple applications**

ViArray Power Management Features – "Off-grid" Unused Resources

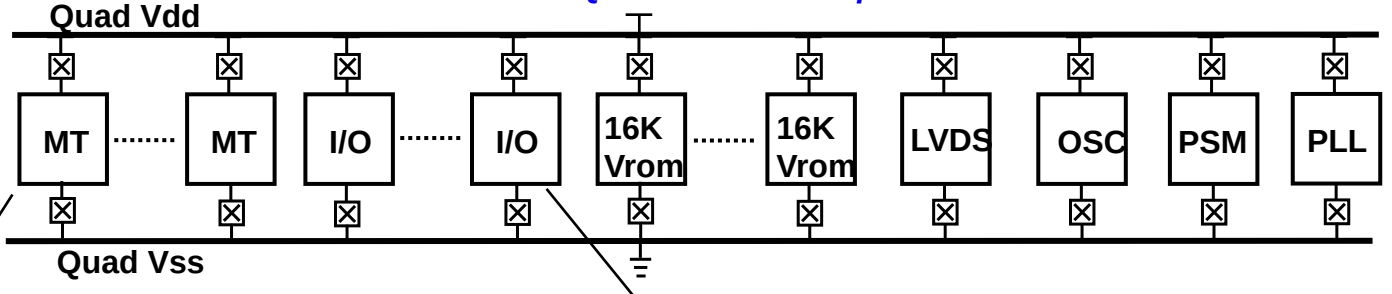
Chip level:



Quadrants are partitioned

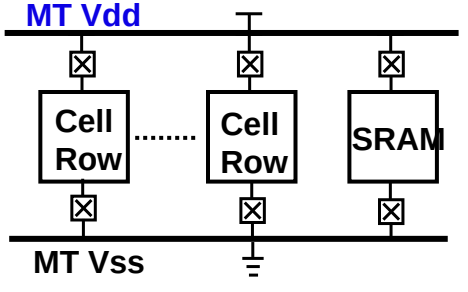
Blocks within Quadrants can be partitioned

Quadrant level:



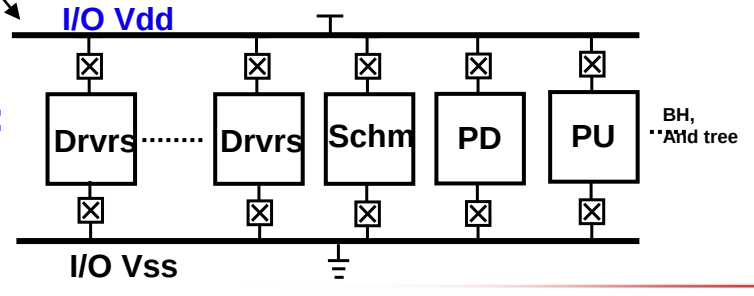
Cell rows & SRAM within MT can be partitioned

MT level:



Sub-blocks within I/O pad can be partitioned

I/O level:



Trusted ViArray

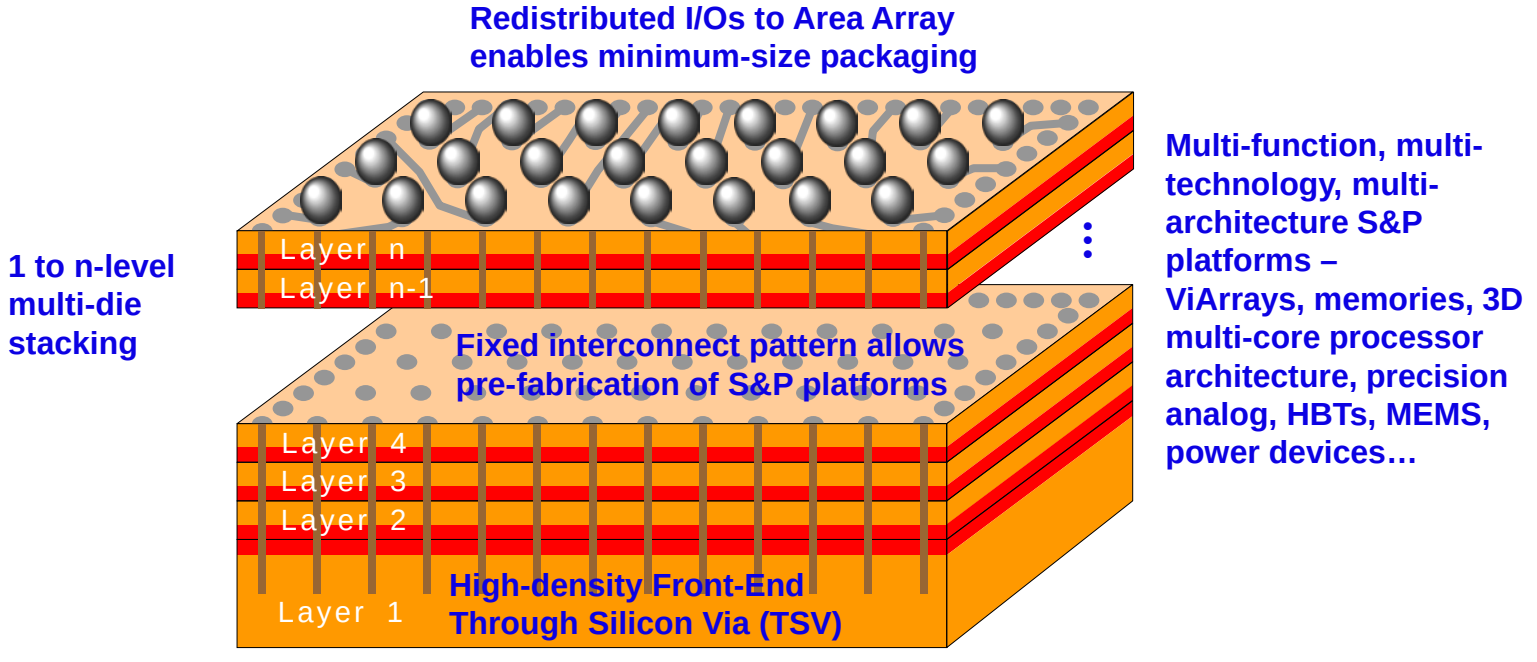
The ViArray has an open architecture with

- **highly compacted and optimized repetitive functional fabrics that are tightly laid out. Minor modifications could affect the overall layout.**
- **fine-grain configurable architecture. Resources in the ViArray are uncommitted until implementation of a specific application, i.e., until via-2 mask is defined.**
- **power management features. Resources in the ViArray may not be connected to power and ground.**

⇒ The ViArray could achieve certain degree of trustworthiness even if the base-array is fabricated in an uncontrolled environment, IF back-end-of-line fabrication for specific application is controlled.

Future Direction

- Additional ViArray Platforms
  - Increase resources
  - Special applications in extreme radiation environment
  - Precision analog functions
- Stack & Pack



Conclusion

- Beginning in 2004, Sandia has developed the ViArray family of structured ASIC base arrays for its internal 350-nm radiation-hardened SOI foundry
- The ViArray architecture is highly efficient, competitive to custom designed cell-based ASIC in speed, power, and circuit density
- The ViArray has unique features to enhance power management, reliability and redundancy architecture for embedded applications
- The ViArray could achieve certain degree of trustworthiness even when the base arrays are fabricated in an uncontrolled environment
- The ViArray implementation approach achieves approximately 5X reduction in schedule and NRE costs compared to cell-based ASIC
- Sandia has a long-term plan to support the ViArray product family