ReSpace/MAPLD 2011

MAPLD Track Overview

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Historically Speaking…

- The Military/Aerospace Programmable Logic Device (MAPLD) Conference began in 1998 and has addressed the following PLD topics:
  - Devices (FPGAs, Non Volatile Memories, Support Devices)
  - FPGA Design and Verification Approaches
  - Military/Aerospace PLD Applications
  - Reliability Issues
  - Radiation Effects and Mitigation
- Past Venues
  - Albuquerque, NM
  - NASA Goddard Space Flight Center – Greenbelt, MD
  - JHU Applied Physics Laboratory – Laurel, MD
  - Washington, DC (Ronald Reagan Building)
  - Annapolis, MD
  - Palm Beach, FL (MAFA)

PLDs Everywhere…

- PLDs have become the workhorse within the digital design community.
- Much more of the board design is migrating into the FPGAs, especially with SOC increasing in popularity.
- FPGAs can be found in all the major spaceflight subsystems including:
  - Command and Data Handling
  - Power Distribution Units
  - Guidance Navigation and Control
  - Attitude Control
  - Propulsion
  - Ground System Electronics

PLD Challenges…

- FPGA devices are becoming more dense which allows for larger, more complex designs.
- FPGA designers with incomplete knowledge of target device technology and appropriate spaceflight usage to mitigate radiation effects.
- Archaic verification techniques mask corner case bugs.
- High pin count devices need signal integrity analysis.
- Board-level decoupling schemes need power integrity analysis.
- FPGA design community (at least within each organization) needs to become more collaborative, rather than designing in a vacuum.
  - Promoting code reuse
  - Sharing Bus Functional Models for commonly used interface devices
  - Creation of IP Libraries
  - Implementation of Revision Control Systems
  - Standardized review process

MAPLD Track Structure

Session	Title	Time	Session Chairs
A (Combined)	PLD Devices	Tues 1– 3:20PM	Keith Avery, Air Force Research Laboratory Paul Murray, SEAKR Engineering
B	Verification And Validation Of FPGAs and PLDs	Wed 1-4:10PM	Doug Sheldon NASA Jet Propulsion Laboratory Marco Figueiredo, Muniz Engineering
C	Designing with FPGAs and PLDs	Wed 4:10-5:25PM Thurs 8-11:20AM	Tim Gallagher, Lockheed Martin MyThi To, Sandia National Laboratories

Program Updates…

Session	Presentation Title	Time	Presentation Authors
A (Combined) Pg 8	Peeling the Onion: Understanding the Layers of Apparent Upsets in the Configuration Readback of the RHBD Virtex-5QV	Tues 2:40PM	Greg Allen, Larry Edmunds, Gary Swift and Y. C. Wang, JPL
C Pg 14	Over 3 Gbps Universal Lossless Compressor for Space Use	Thurs 10:55AM	Lowell Miles, Penshu Yeh, Joe Feeley, David Fisher, Sterling Whitaker and Gary Maki, ICS

Final Thoughts…

Enjoy the Conference!

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