Applying OVM (UVM) to GOES-R C&DH Development
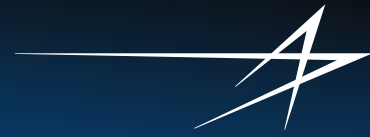
Dr. J. David Foggy
GOES-R Verification Lead
Lockheed Martin SSC

Doug Krening
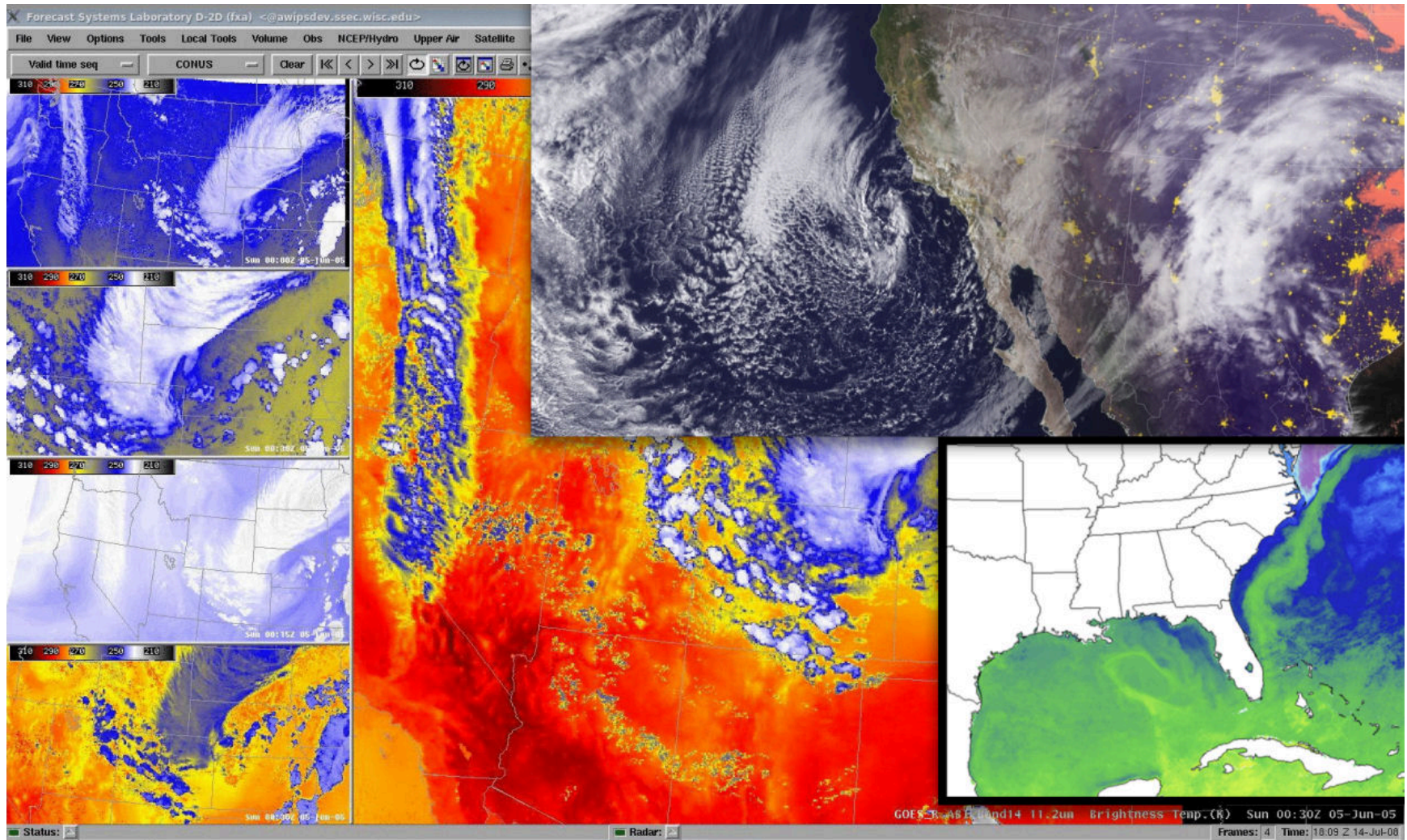Verification Consultant

Michael Horn
Principal Verification Architect
Mentor Graphics

Tim Gallagher
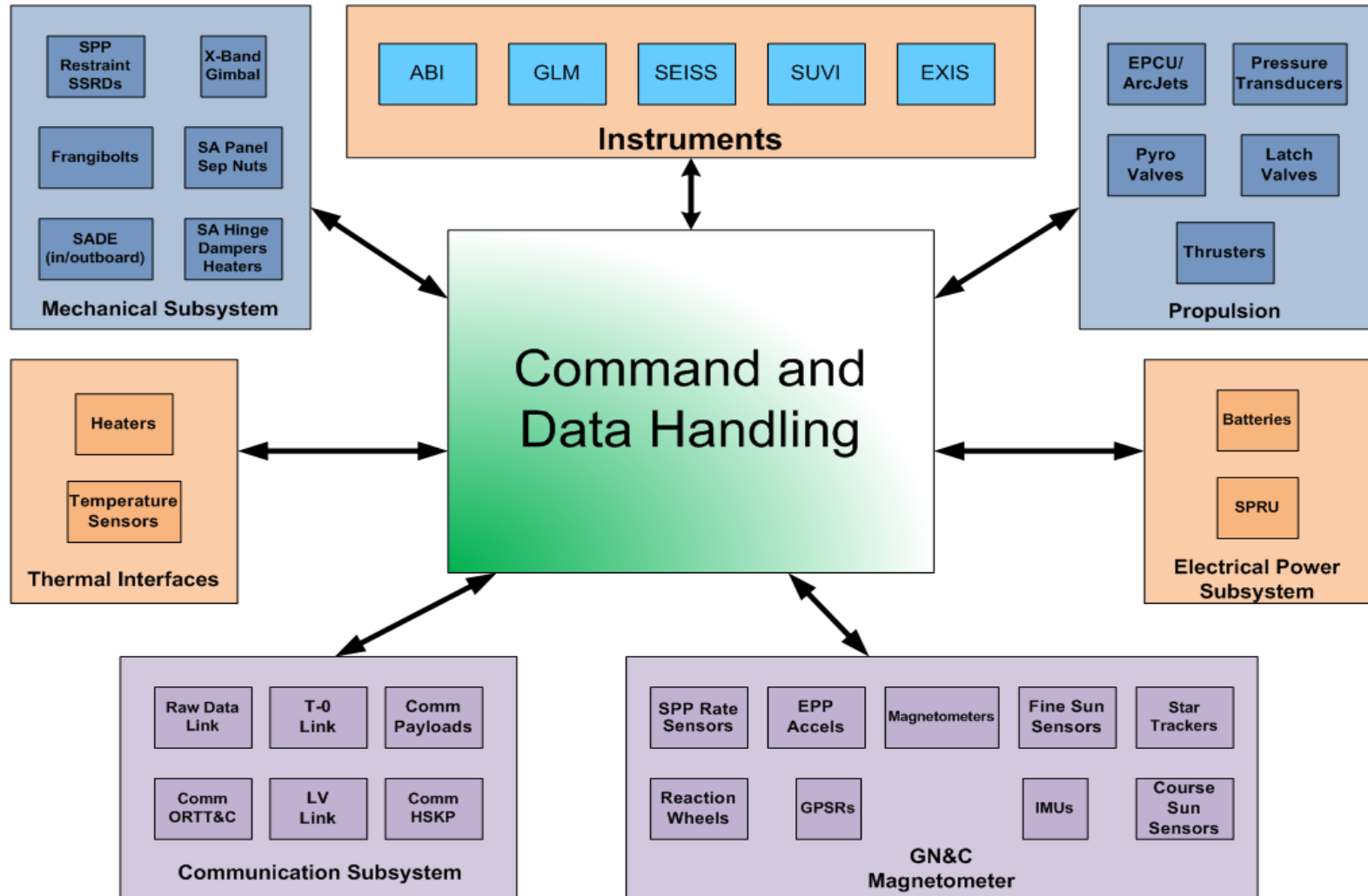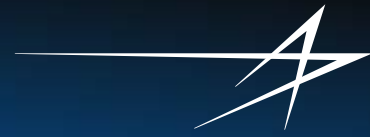LM Fellow
Lockheed Martin SSC

*Source: Mentor Graphics

GOES-R

*Courtesy: NOAA

GOES-R Weather Images

*Courtesy: NOAA

Command & Data Handler (C&DH)

*Source: LM GOES-R Program

# *Why*

Why Verification?

Design Phase	Requirements	Specifications	Logic Design	Verification	HW-SW Verification	Post-Si Test	Customer Return	Total Bug Detection Cost (based on 1000 Bug Project)
Cost of Finding Bug (units)	1	10	100	1,000	10,000	100,000	1,000,000	
Bug Injection Distribution	10%	30%	60%	0%	0%	0%	0%	
Bug Distribution Best In Class	5%	10%	20%	64%	1%	0.10%	0.01%	961,050
Bug Distribution Example 1	5%	10%	20%	54%	10%	1%	0.10%	3,561,050
Bug Distribution Example 2	5%	10%	20%	44%	15%	5%	1%	16,961,050
Bug Distribution Example 3	5%	10%	20%	38%	20%	10%	5%	32,401,050

*Source: Mentor Graphics

The Compounding Problem

Design Complexity Trends

Standard Moore's Law Curve
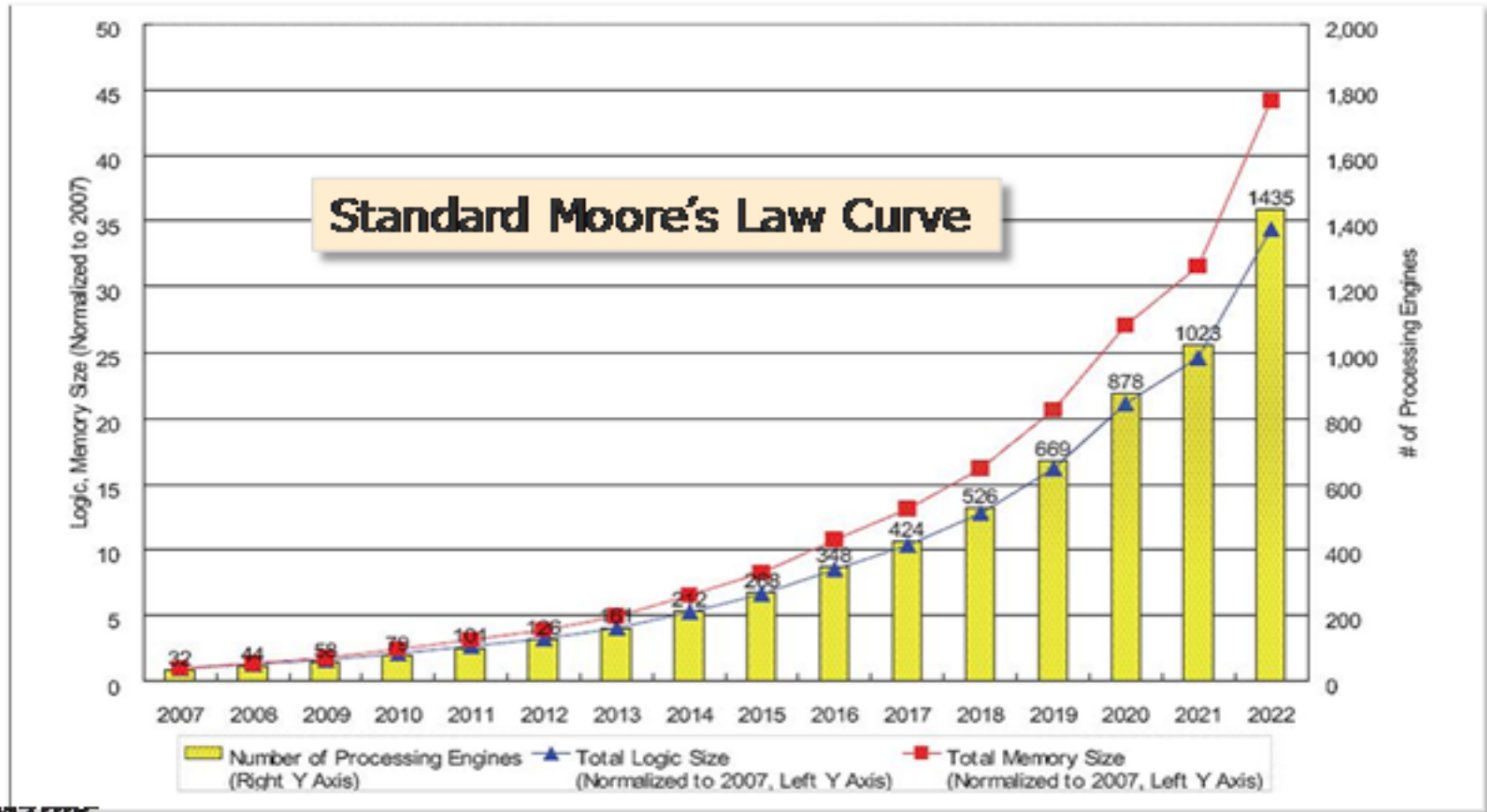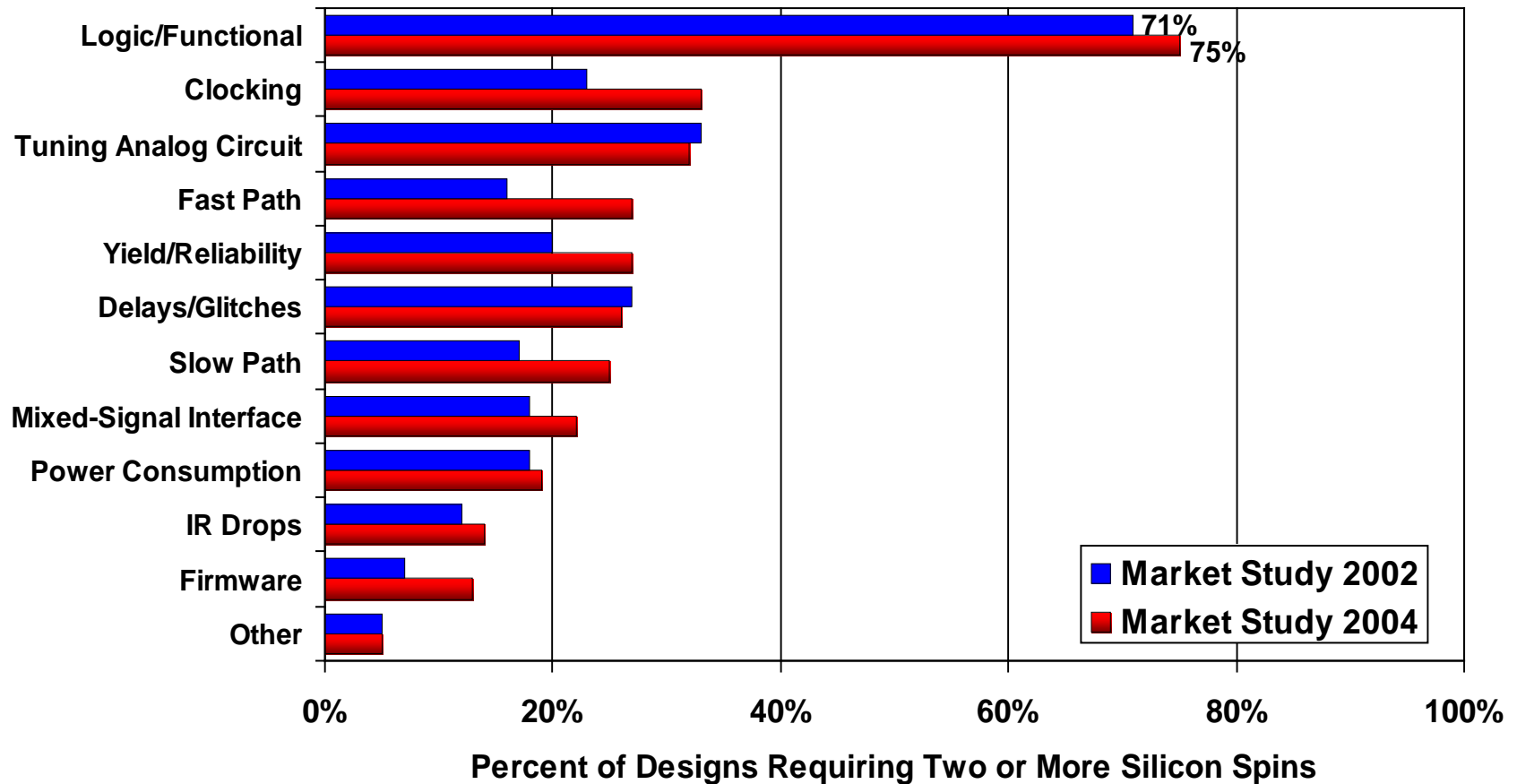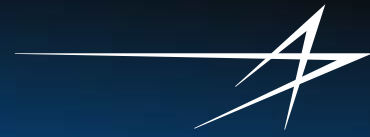
FPGA/ASIC Verification Trends
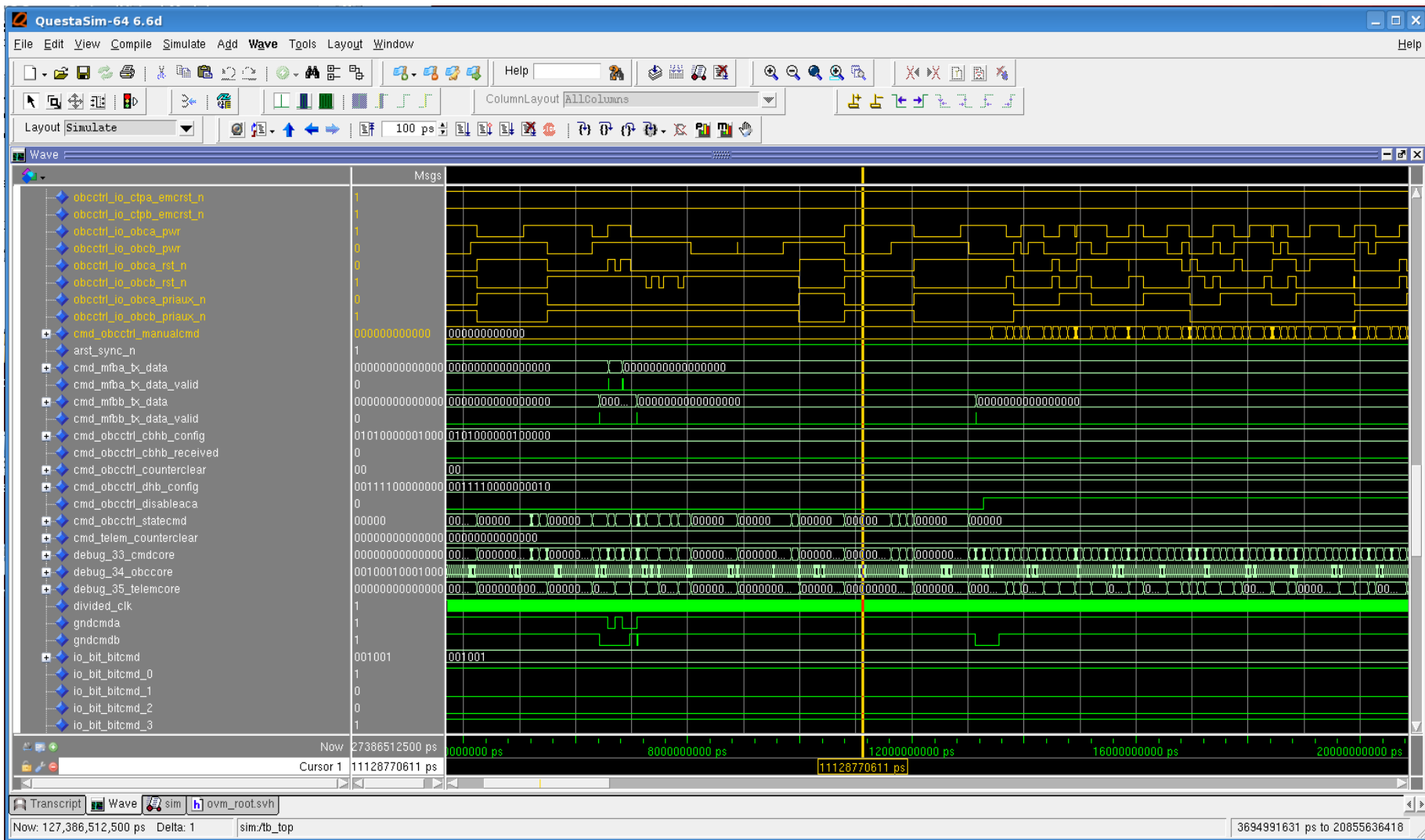

IC/ASIC Designs Requiring Re-Spins by Type of Flaw

Source: 2004/2002 IC/ASIC Functional Verification Study, Collett *International* Research, Used with Permission
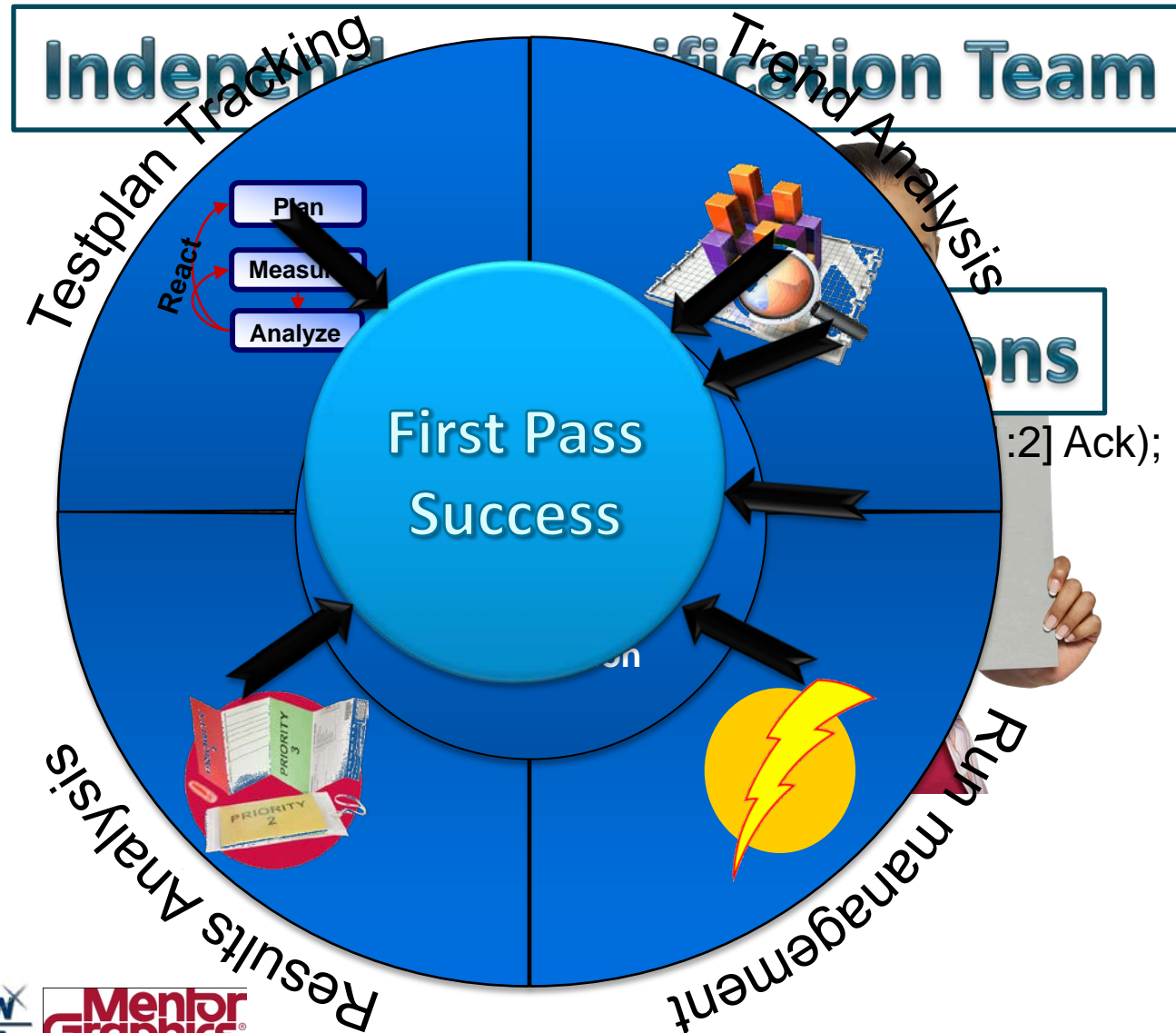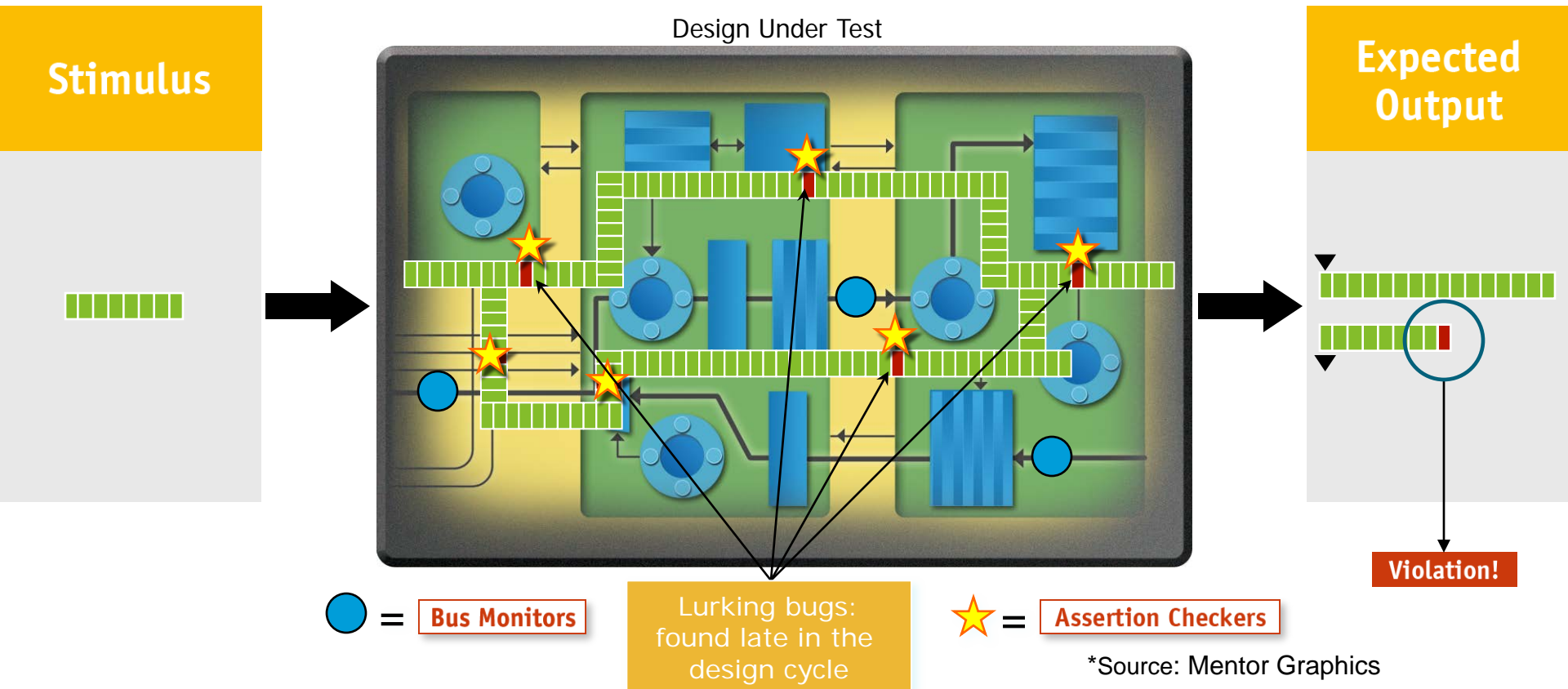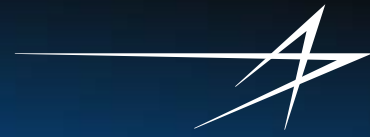
What

Yesterday

*Source LM GOES-R Program

13

C&DH Techniques/Technologies

*Source: Mentor Graphics

Advanced Functional Verification

Design Under Test

Stimulus

Expected Output

Violation!

🔵 = Bus Monitors

Lurking bugs: found late in the design cycle

⭐ = Assertion Checkers

*Source: Mentor Graphics

Today

*Source LM GOES-R Program

What and Why