RASTA – An FPGA-based Infrastructure for Development, Prototyping and Validation of On-board Systems

Sandi Habinc, Daniel Hellström,
Kristoffer Glembo, Marko Isomäki, Jiri Gaisler

Aeroflex Gaisler AB

sandi@gaisler.com
+46 31 775 86 50
www.Aeroflex.com/Gaisler

Kungsgatan 12, SE-411 19 Göteborg, Sweden

RESPACE/MAPLD 2011

Background

Many software and hardware components developed in R&D activities do not reach required maturity level for use in space projects, due to lack of a representative environment for validation & demonstration.

The RASTA (Reference Avionics System Testbed Activity) aims to fill this gap by providing a standard hardware and software infrastructure to integrate R&D activity results.

The RASTA objectives are to:

- **allow new technology to be validated in flight representative environment,**
- **support mission and spacecraft design,**
- **support on-board software verification and validation through the project life-cycle by means of a coherent emulations platform,**
- **maximize reuse of the existing avionics technologies and to be scalable.**

Hardware concept

RASTA development platform is today based on the Compact PCI (cPCI) bus. Communication between boards is performed via the PCI bus in the backplane.

For other protocols, such as SpaceWire and Mil-Std-1553B, connectors are provided on the front-panel of each board.

The trend is to use less the PCI and more the SpaceWire interfaces on the front-panels. Future RASTA systems will probably use an active or a passive SpaceWire backplane.

RASTA comprises processor and interface boards, and in the future also SpaceWire router boards. Standard parts are used for processors such as UT699 and GR712RC, FPGA boards are used to allow new functions to be incorporated.

The complete RASTA avionics solution is available from us.

Software concept

The on-board software and tools developed or adapted for RASTA are part of a complete set of layers and libraries allowing the integration of embedded real-time applications independently from the actual operating system used for the RASTA environment, with minimum modification.

Baseline operating system is open source RTEMS 4.10, but also VxWorks 6.5 is supported. To communicate with interface boards, device drivers are provided executing on any LEON3 processor, e.g. UT699 or GR712RC.

RTEMS has been extended with a Plug&Play capability to detect installed boards, including any IP cores residing inside the FPGA/ASIC devices on these boards.

Benefits and usefulness

RASTA allows quick and easy integration of complete avionics systems in lab environment, using standardized interfaces and connectors.

It provides easy access to LEON technology (through pre-programmed FPGA, ASIC or UT699 & GR712RC).

It offers ready-made configurations, but also custom made solutions. Examples of easily added functions are: Mil-Std-1553B buses, CCSDS telemetry and telecommand, etc.

It supports development and verification of on-board software and hardware (e.g. FPGA design using IP cores).

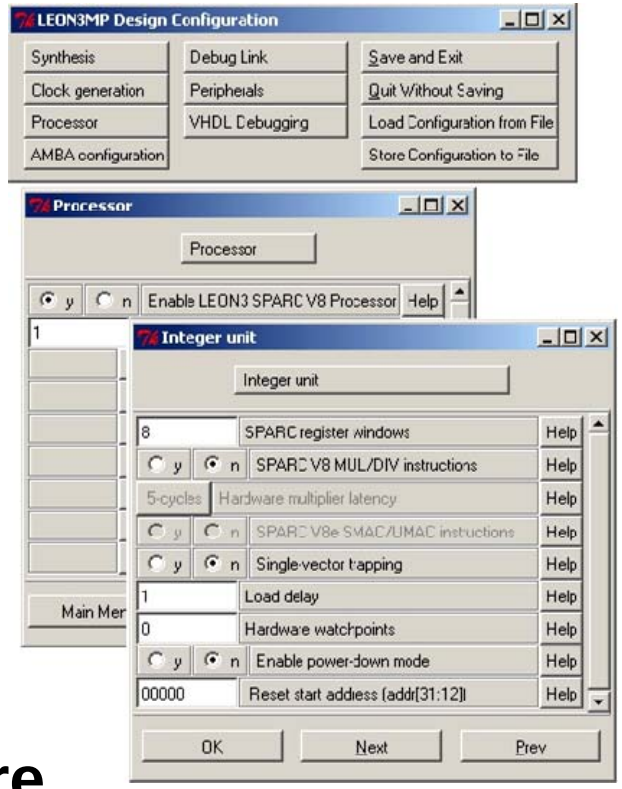
The tight integration between hardware and software allows users to get started and be productive immediately.

RASTA is often used as a building block in larger systems, such as S/W validation facilities and spacecraft testbeds.

GRLIB IP core library

GRLIB is a complete design environment:

- **Processors**
- **Peripherals**
- **Serial interfaces**
- **Parallel interfaces**
- **Memory controllers**
- **AMBA on-chip bus with Plug & Play support**
- **Fault tolerant and standard versions**



Support for tools & prototyping boards

Portability between technologies:
Actel, Aeroflex, Altera, Artisan, Atmel, DARE, eASIC/Nextreme, Eclipse, Lattice, Synopsys DesignWare Ramon Chips / RadSafe, TSMC, UMC, Virage, Xilinx, etc.

AEROFLEX GAISLER

GRLIB Plug-and-Play

Fully compliant with AMBA 2.0 AHB/APB buses, with additional sideband signals.

Plug&Play information allows for distributed address decoding, interrupt steering, cacheability information, etc.

No modification of centralized resources, e.g. address decoder, arbiter or interrupt controller, is required.

Automatic generation of table including vendor and device identifier for each core, including version and interrupt information.

Software can scan table to install corresponding drivers etc.

Hardware debuggers can use table for initializing various IP cores, etc.

Processors

- **Processors**
  - **LEON3 - High-performance SPARC V8 32-bit Processor**
  - **LEON3FT - Fault-Tolerant SPARC V8 32-bit Processor**
  - **DSU3 - LEON3 Hardware Debug Support Unit**
  - **LEON4 - High-performance SPARC V8 32-bit Processor**
  - **LEON4FT - Fault-Tolerant SPARC V8 32-bit Processor**
  - **DSU4 - LEON4 Hardware Debug Support Unit**
  - **MUL32 - Signed/unsigned 32x32 multiplier module**
  - **DIV32 - Signed/unsigned 64/32 divider module**
  - **SRMMU - SPARC Reference Memory Management Unit**
  - **IOMMU - I/O Memory Management Unit**
  - **L2CACHE - Level-2 Cache (with Fault-Tolerance option)**
- **Floating-point Unit (Std/FT)**
  - **GRFPU - High-performance IEEE-754 Floating-Point Unit**
  - **GRFPU Lite - IEEE-754 Floating-Point Unit**

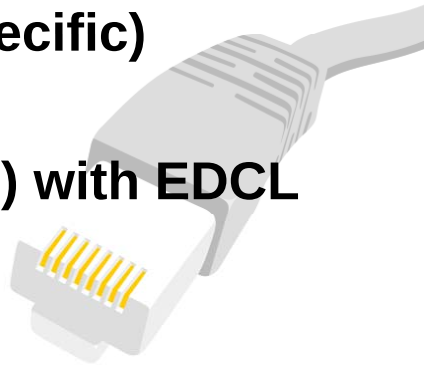
AEROFLEX GAISLER

Connectivity

- **Peripheral Chip Interconnect (PCI)**
  - **GRPCI - 32-bit PCI Initiator/Target with configurable FIFO and AMBA AHB backend**
  - **PCIDMA - DMA Controller for the GRPCI interface**
  - **PCIARB - PCI arbiter**
- **SpaceWire with RMAP target**
  - **GRSPW - SpaceWire codec with AHB master interface & RMAP**
  - **GRSPW2 - SpaceWire codec with AHB master interface & RMAP**
  - **GRSPWCODEC – SpaceWire encoder-decoder**
  - **GRSPWROUTER – SpaceWire Router IP**
- **Mil-Std-1553B**
  - **GR1553B - Mil-Std-1553B BC / RT / MT (new IP core)**
- **CCSDS/ECSS**
  - **GRTC - CCSDS Telecommand Decoder**
  - **GRTM - CCSDS Telemetry Encoder**
  - **GRCTM - CCSDS Time Manager (CCSDS Unsegmented Code)**

Connectivity

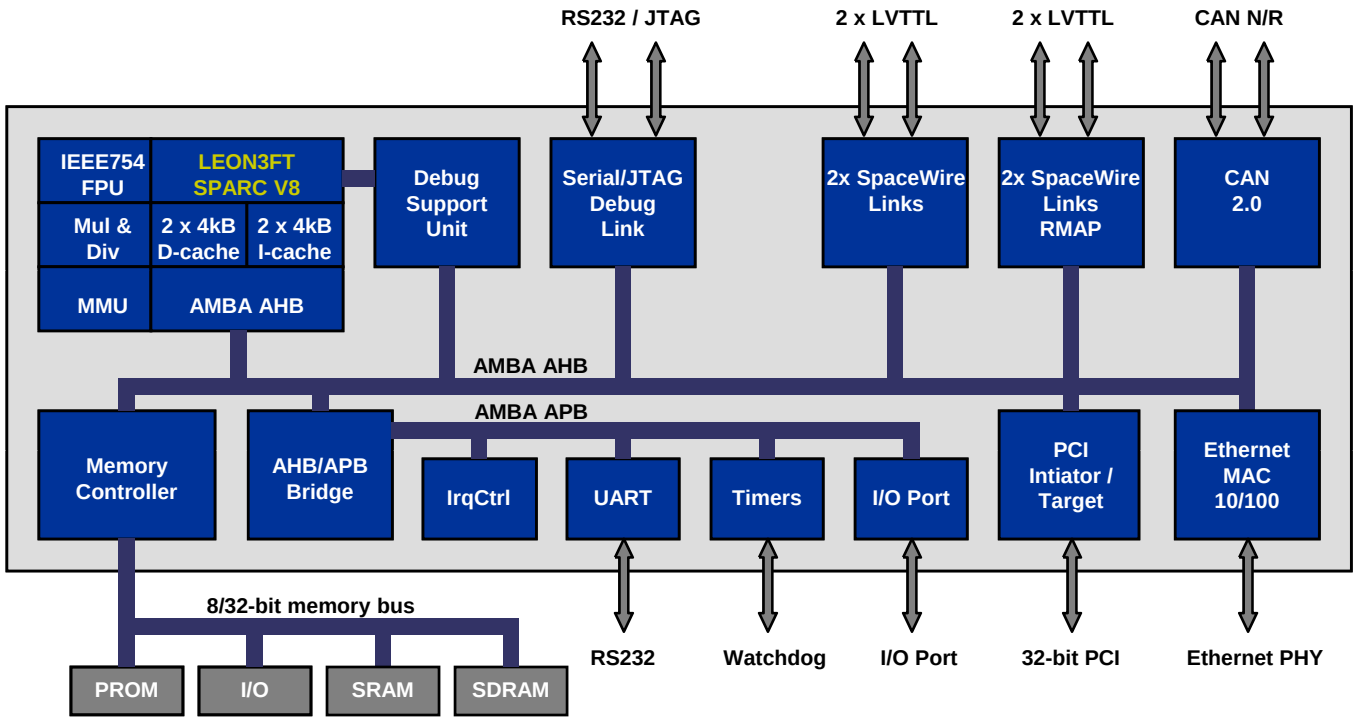
- **Universal Serial Bus (USB)**
  - **GRUSBDC - USB 2.0 Device Controller**
  - **GRUSBHC - USB 2.0 Host Controller**
- **Serial Peripheral Interface (SPI) bus**
  - **SPICTRL - SPI Controller**
  - **SPIMCTRL - SPI Memory Controller**
- **Inter Integrated Circuit (I^2C) bus**
  - **I2CMST - I^2C Master**
  - **I2CSLV - I^2C Slave**
- **Controller Area Network (CAN) bus**
  - **CAN_OC - GRLIB wrapper for OpenCores CAN interface core**
  - **GRCAN - CAN 2.0 Controller with DMA**
  - **GRHCAN - CAN 2.0 Controller with DMA (ESA specific)**
- **Ethernet 10/100/1000**
  - **GRETH - Ethernet Media Access Controller (MAC) with EDCL**
  - **GRETH_GBIT - Gigabit Ethernet MAC with EDCL**



Case 1: Multi-board distributed system

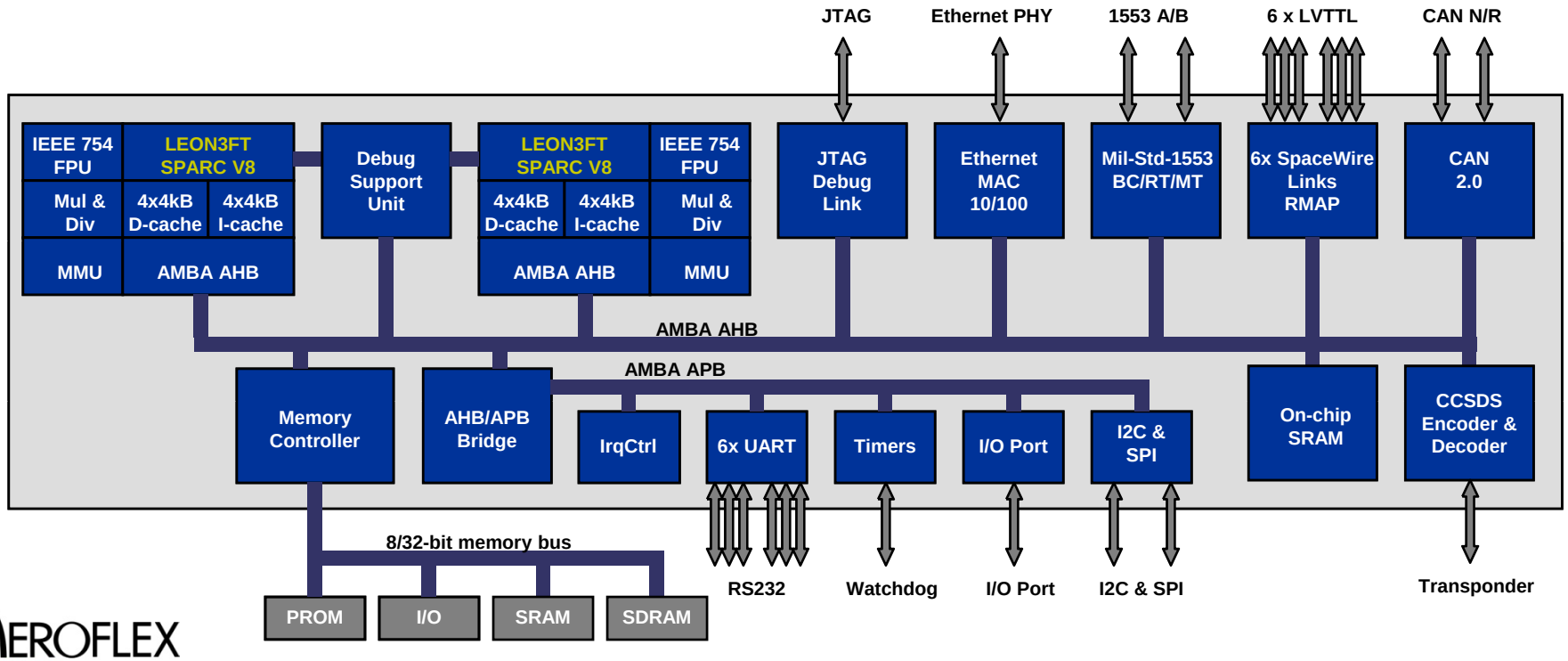
UT699: LEON3FT SPARC processor design based on IP cores from GRLIB, comprising LEON3FT processor with MMU & high-performance FPU, SpaceWire links with RMAP, CAN bus, Ethernet, PCI, etc.

In-house RASTA boards were used for early prototyping.



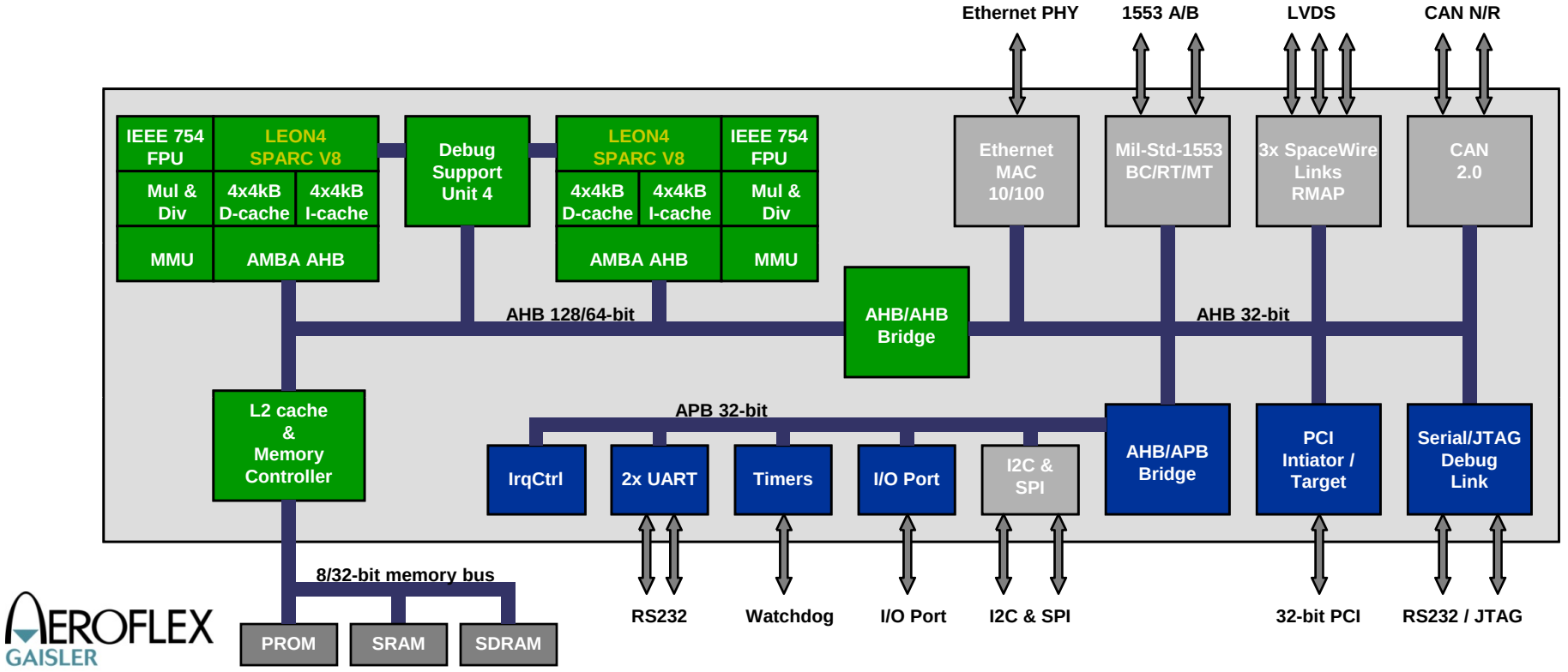
Case 2: Single Board Integrated System

GR712: The LEON3FT SPARC processor, with high-performance FPU & MMU, multiple SpaceWire links, CCSDS telemetry encoder and telecommand decoder, etc., is used in a multi-processor design based on Ramon Chips' radiation-tolerant 180 nm ASIC library.



Case 3: Next Generation Processor

A dual-core LEON4 system-on-chip prototype, together with standard peripherals and interfaces, can now be designed using the new GRLIB2 IP cores in combination with existing GRLIB IP cores. The example below shows how a future device could look like.



AEROFLEX GAISLER

Hardware elements: Components

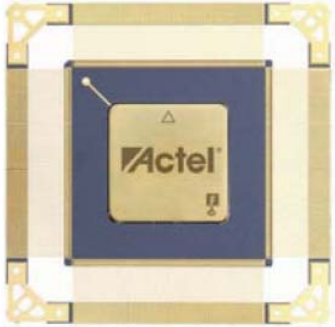
The RASTA concept covers both ASIC and FPGA components.

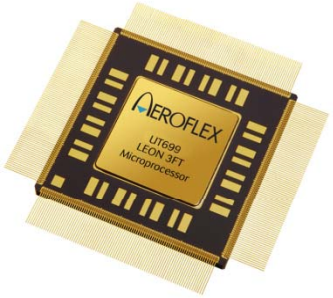
FPGAs:

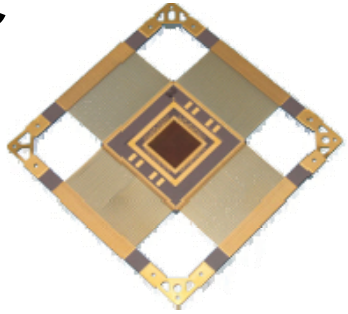
- **Xilinx Virtex-4 LX110/LX200**
- **Actel RTAX2000S/AX2000**

ASICs (standard parts):

- **Aeroflex GR712RC**
- **Aeroflex UT699**
- **Atmel AT697**
- **Atmel AT7913**

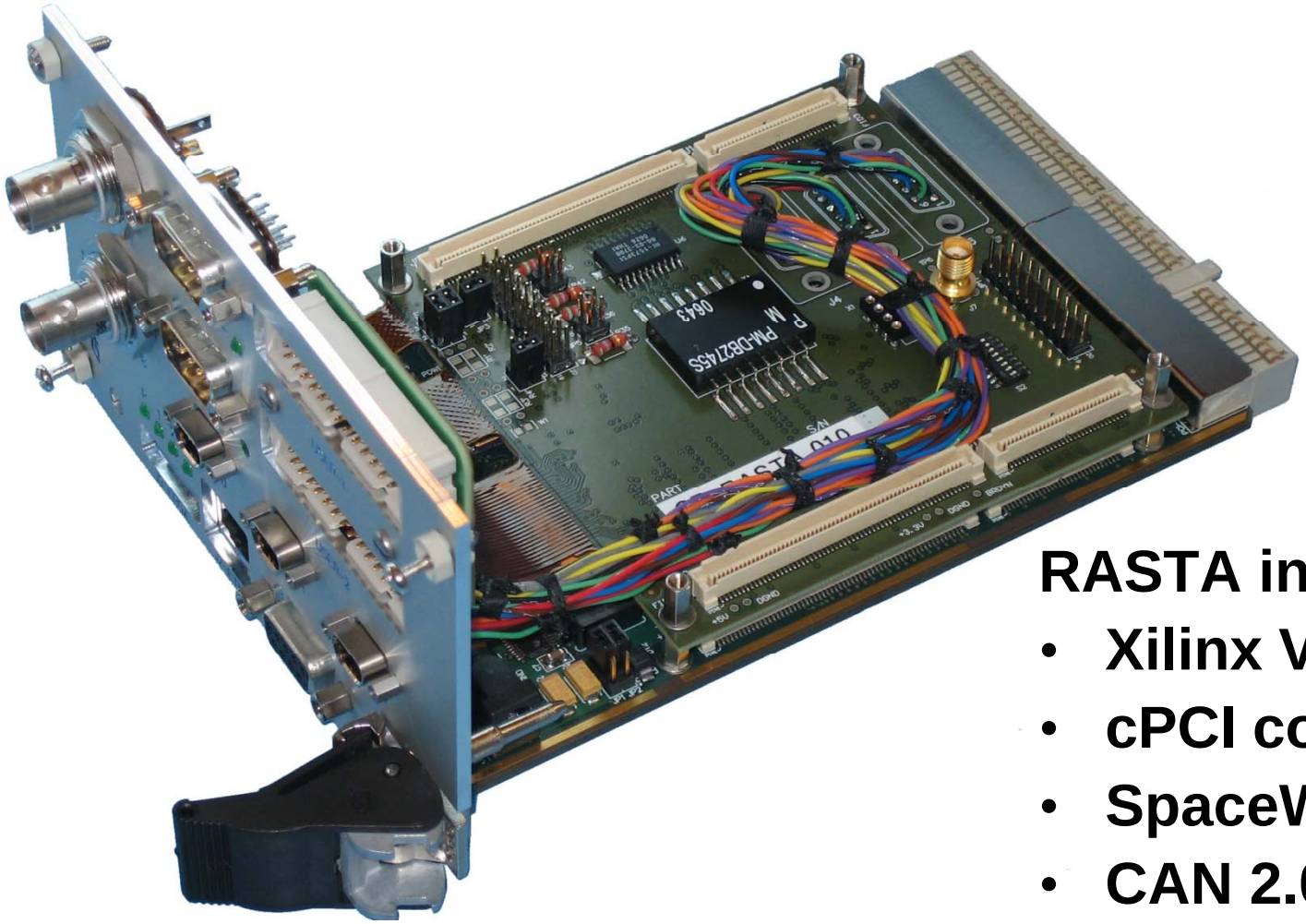






AEROFLEX GAISLER

RASTA interface board

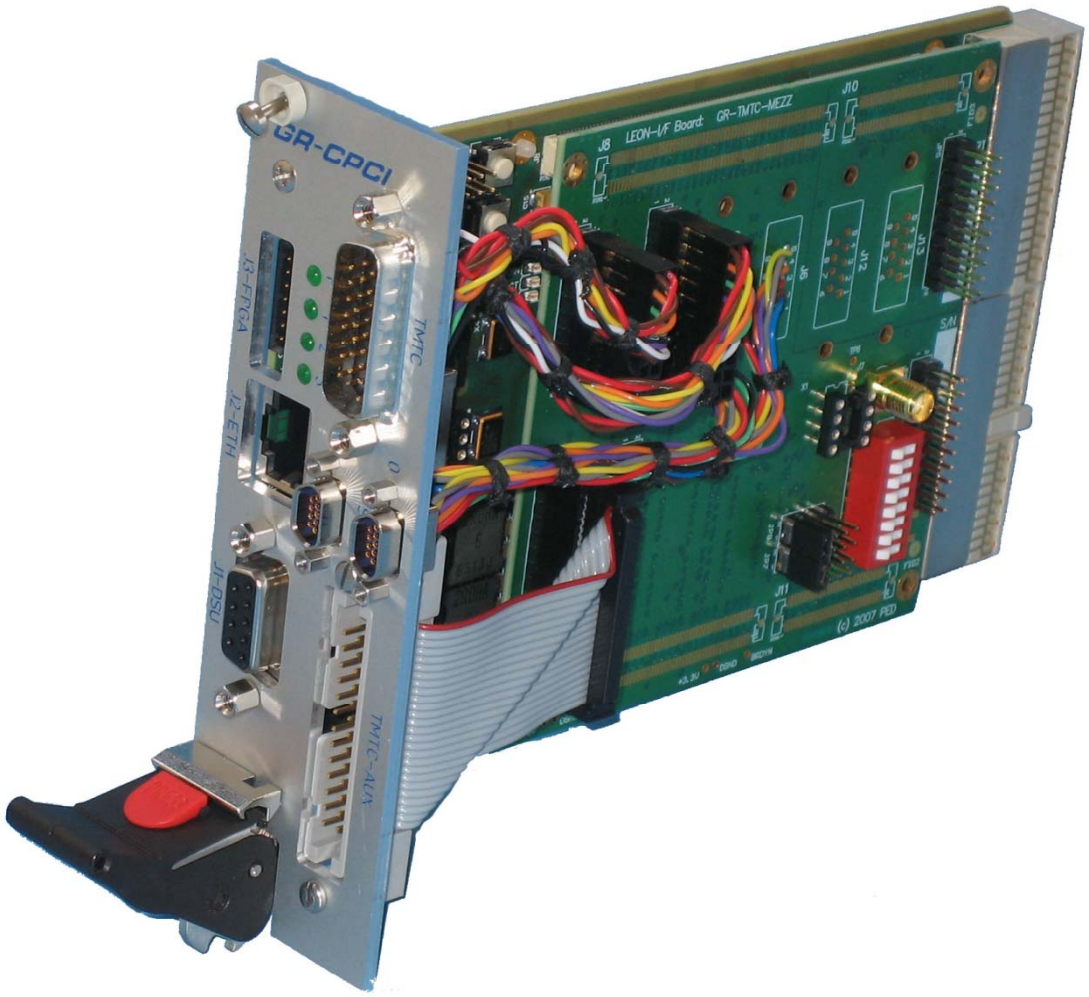


RASTA interface board:

- **Xilinx Virtex-4 FPGA**
- **cPCI connector**
- **SpaceWire with RMAP**
- **CAN 2.0B**
- **MIL-STD-1553B**
- **Optional LEON3**

AEROFLEX GAISLER

RASTA TM/TC board



RASTA TM/TC board:

- **Xilinx Virtex-4 FPGA**
- **cPCI connector**
- **SpaceWire with RMAP**
- **RS422 transceivers for TM&TC and CLCW cross-strapping**
- **LVTTL pulse commands**
- **Ethernet, UART, JTAG**
- **Optional LEON3**

RASTA SpaceWire Router boards

RASTA SPW16 board:

- Xilinx Virtex-4 FPGA
- cPCI connector
- 16x SpaceWire
- 2x AMBA with RMAP
- PCI 32-bit 33 MHz Initiator/Target
- Ethernet, UART, JTAG

RASTA SPW4 board:

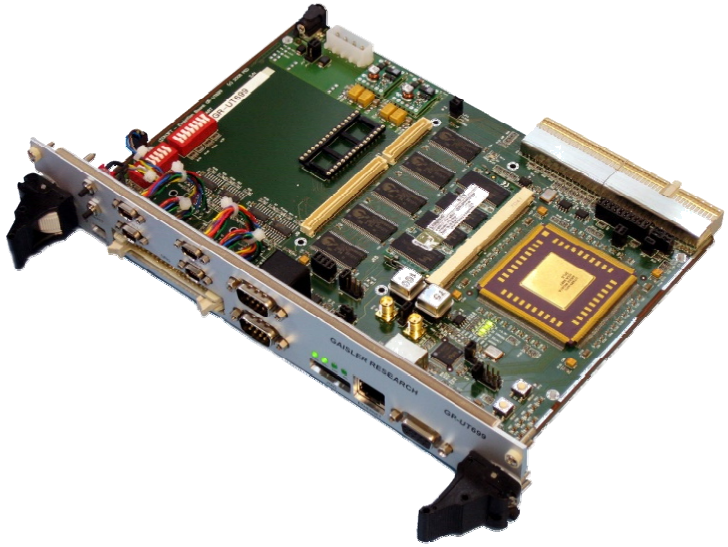
- Xilinx Virtex-4 FPGA
- cPCI connector
- 4x SpaceWire
- 2x AMBA with RMAP
- PCI 32-bit 33 MHz Initiator/Target
- Ethernet, UART, JTAG

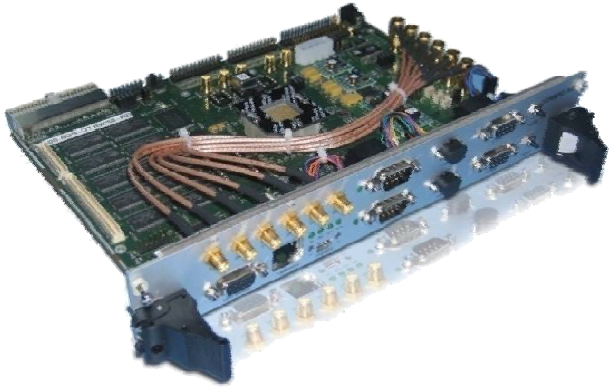
Other compatible boards

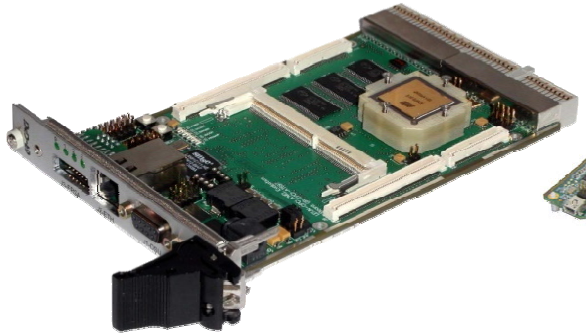
The RASTA concept is compatible, both hardware and software, with other LEON and SpaceWire based CPCI boards.

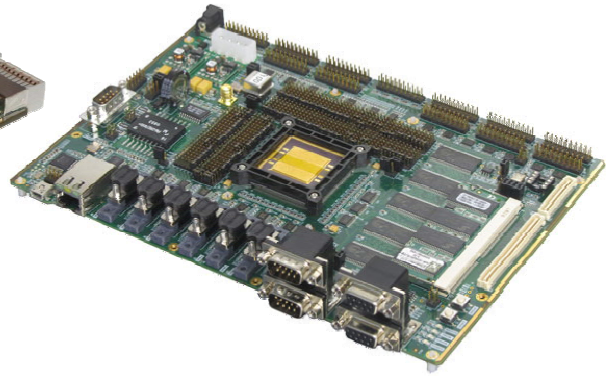
Examples of Aeroflex boards:

- **GR-CPCI-UT699**
- **GR-CPCI-AT7913 (SpW-RTC)**
- **GR-CPCI-AT697**
- **GR712RC-BOARD**

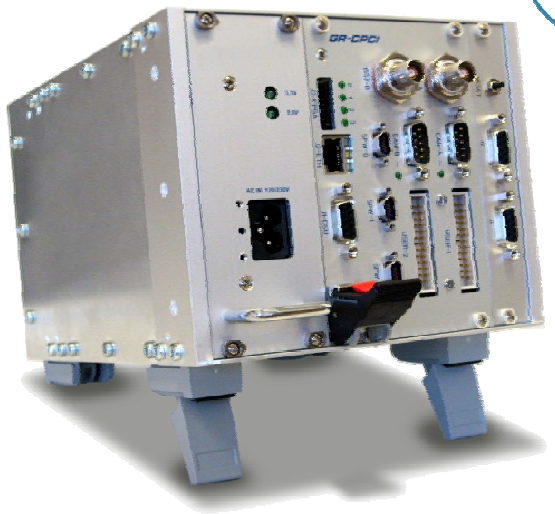








RASTA Compact PCI crates

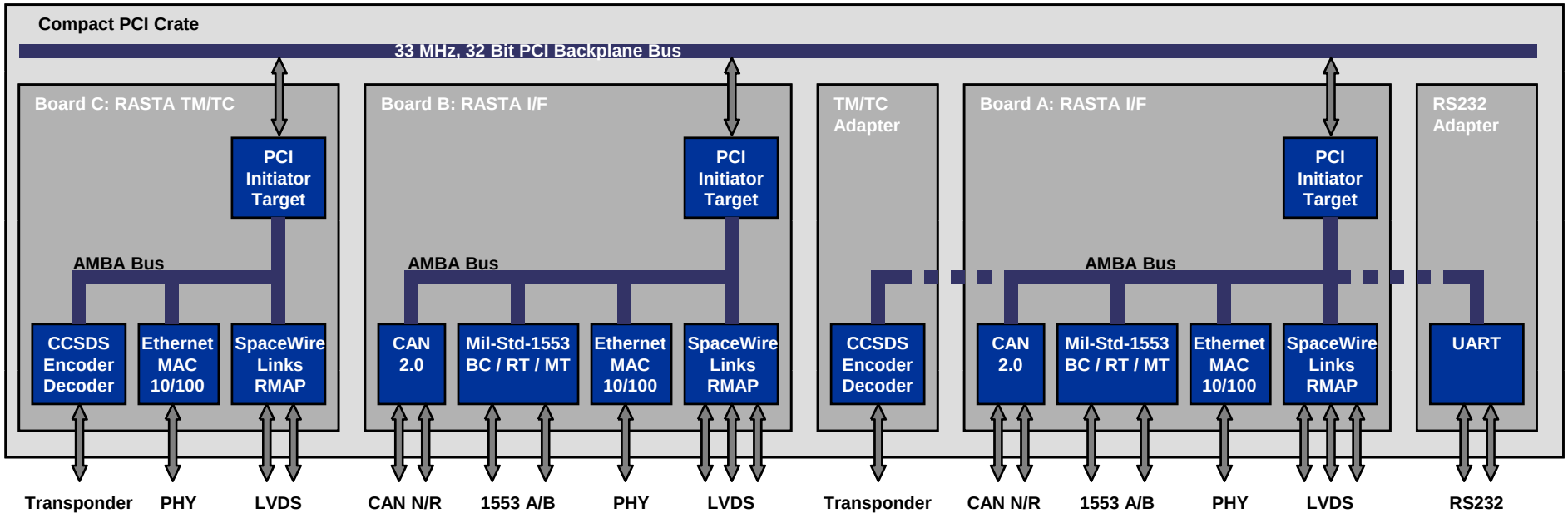


RASTA is based on standard size 3U and 6U Compact PCI crates.

(Only 3U configurations are shown on this slide.)

General CPCI crate configuration

A compact PCI crate with Xilinx based development boards can be used to emulate different designs featuring LEON3 and LEON4 processors. The architecture features communication via the backplane PCI bus, or via the SpaceWire links on the front-panels.



RASTA standard configurations

RASTA configurations comprise (multi-board):

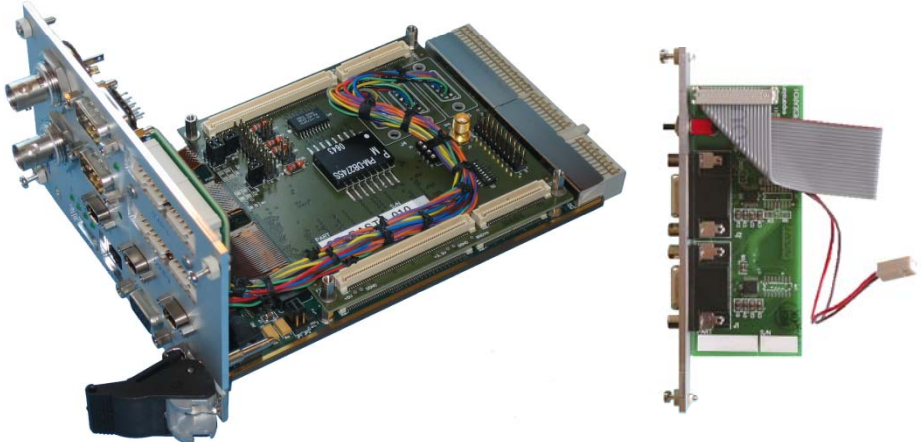
- **Processor board, either LEON3 or LEON2**
- **Interface board**
- **Telemetry and telecommand board**

RASTA integrated configurations comprise (single-board):

- **Board with either LEON3 or LEON3, with integrated interfaces and/or telemetry and telecommand support**

Example of a configuration:

- **GR-RASTA-105**
  - **GR-RASTA-I/F board**
  - **GR-CPCI-SER RS232 board**
  - **LEON3, PCI, SpaceWire, CAN, Mil-Std-1553, Ethernet, UART**



AEROFLEX GAISLER

Supported operating systems

Full RASTA support for RTEMS 4.10:

- LEON2 / LEON3/LEON3-MP / LEON4/LEON4-MP
- All standard peripherals
- All serial interfaces
- All auxiliary interfaces
- CCSDS Telemetry and Telecommand
- Multiprocessing, AMP, shared memory model

Partial RASTA support for VxWorks 6.5: WIND RIVER

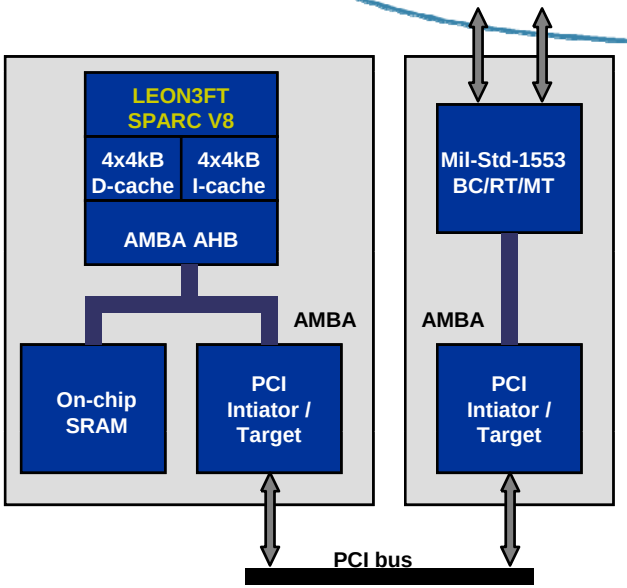
- LEON2 / LEON3
- PCI, CAN, SpaceWire, Mil-Std-1553 (BRM & RT only)
- ADC/DAC, GPIO, Timers, UART
- No multi-processor support in VxWorks 6.5

Future RASTA support for VxWorks 6.7 SMP:

- LEON3-MP / LEON4-MP

RTEMS PCI and SpaceWire support

PCI support
- Configuration space access
- Auto configuration library (PCI Plug&Play)
- Shared interrupt management
- Address translation



PCI host drivers
- GRPCI core (e.g. UT699)
- PCIF core (Actel RTAX2000S/AX2000)
- Synopsys PCI core (e.g. AT697)

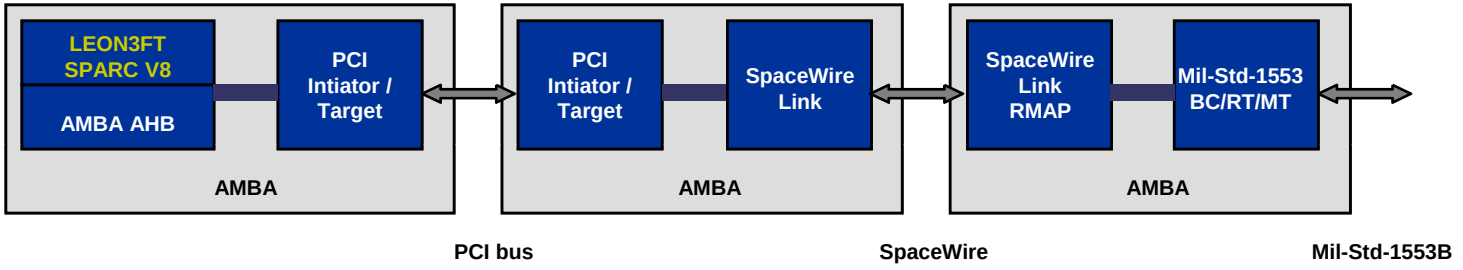
SpaceWire RMAP drivers
- GRSPW / GRSPW2 (UT699, GR712RC, LEON3FT-RTAX, LEON4)
- RMAP initiator software stack
- Auto configuration library (Plug&Play)

PCI / SpaceWire board drivers
- GR-RASTA-I/F, GR-RASTA-TM/TC, GR-RASTA-ADC/DAC
- GR701A Companion Chip, GR703 CCSDS TM/TC Chip

RTEMS Plug & Play capability

RASTA RTEMS supports multi-level plug&play discovery: AMBA bus, PCI bus, SpaceWire link

1. Initial scanning of on-chip AMBA bus is performed
2. RTEMS drivers are registered for detected IP cores
3. If a PCI interface is found, PCI bus is scanned and configured
4. If a known peripheral PCI board is found, with AMBA plug&play indication, the AMBA bus of the peripheral device is scanned
5. RTEMS drivers are registered for detected IP cores on PCI board
6. If a SpW interface is found, optional RMAP initiator stack is loaded
7. If the SpW link is active, optional scanning for remote RMAP targets is performed on the SpaceWire network
8. If a known peripheral SpW board is found, with AMBA plug&play indication, the AMBA bus of the peripheral device is scanned
9. RTEMS drivers are registered for detected IP cores on SpW board



Contact information

- **Processor and IP core information:**
  http://www.Aeroflex.com/Gaisler
- **Board and component information:**
  http://www.Aeroflex.com/Gaisler
- **Software and tools information:**
  http://www.Aeroflex.com/Gaisler
- **Contact:**
  sales@gaisler.com