Using FPGAs and a LEON3FT Processor to Build a "Flying Laptop"

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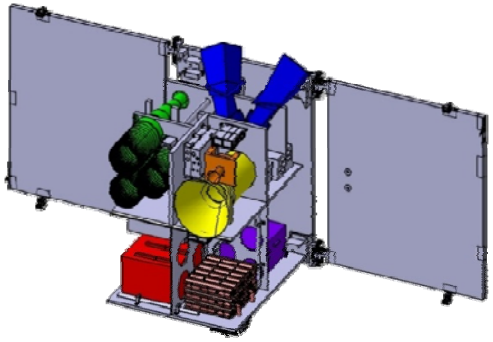
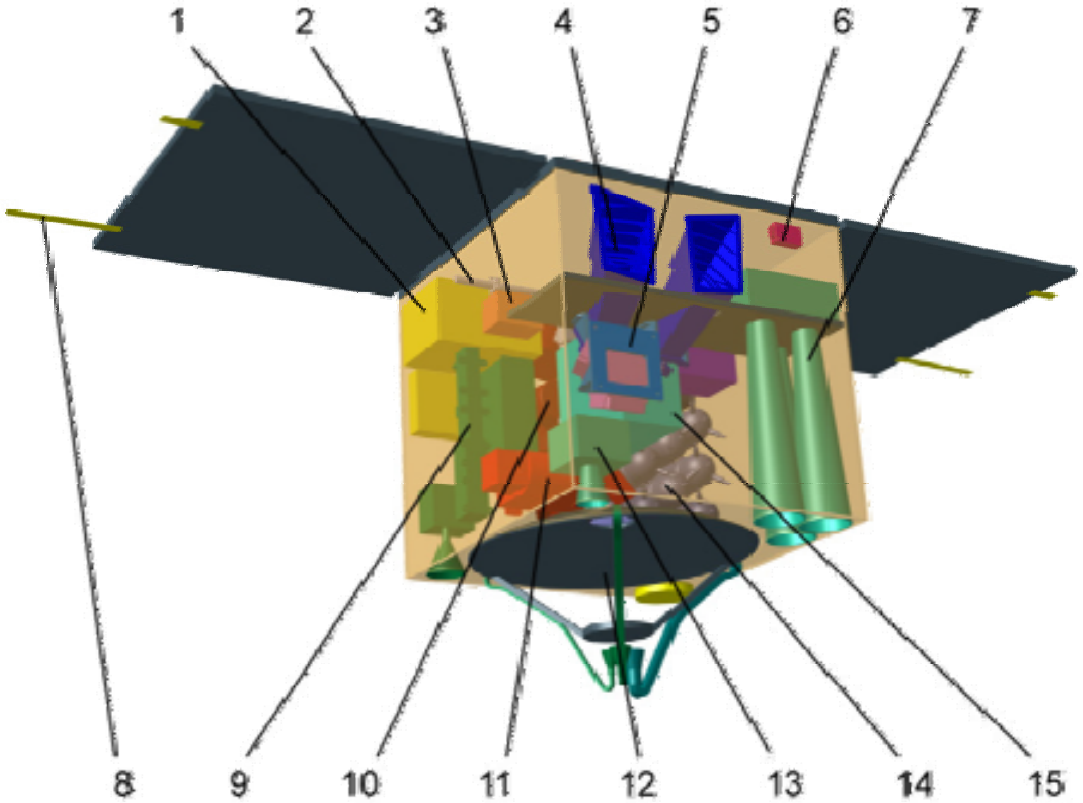
RESPACE/MAPLD 2011

The Flying-Laptop (FLP) Satellite

- Activity lead by Institute of Space Systems, University of Stuttgart (D)
- 3-axis stabilized LEO satellite
- Box size of 60cm x 70cm x 80cm
- Deployable solar panels
- Mass of 120kg
- AOCS including star trackers, wheels, GPS
- Launch envisaged 2013 on ISRO PSLV launcher
- Payloads:
  - Panoramic camera,
  - Multispectral camera,
  - Laser link terminal



The Flying-Laptop (FLP) Satellite



1 - Comm Electronics
2 - Magnetic Torquers
3 - GPS Electronics
4 - Star Trackers
5 - Rate Sensors
6 - Magnetometer
7 - VIS/NIR Camera
8 - Comm Antennas (LG)
9 - Ka-Band TWT
10 - Reaction Wheels
11 - TIR Camera
12 - Cassegrain System
13 - Panorama Camera
14 - Batteries
15 - On-Board Computer

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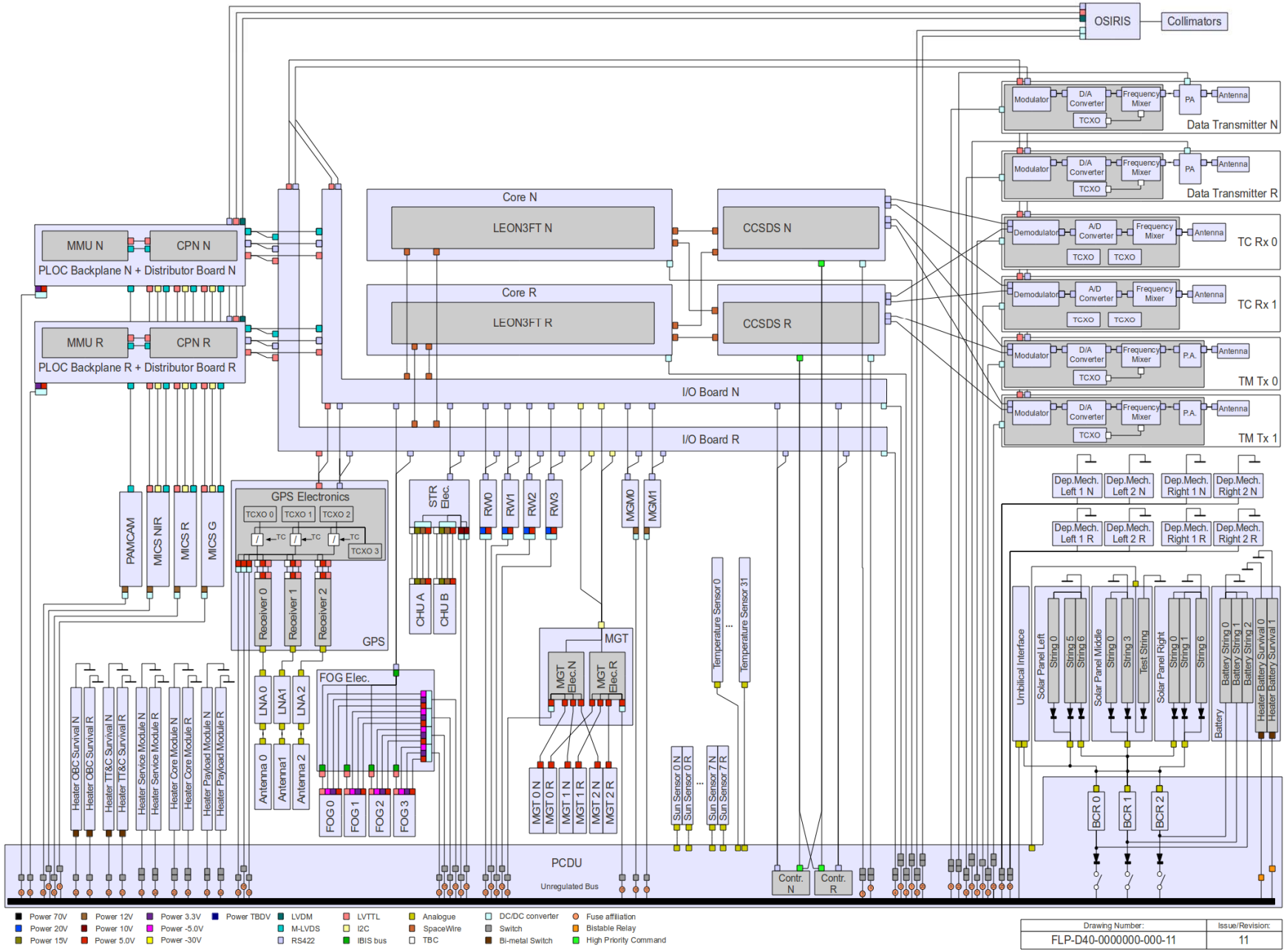
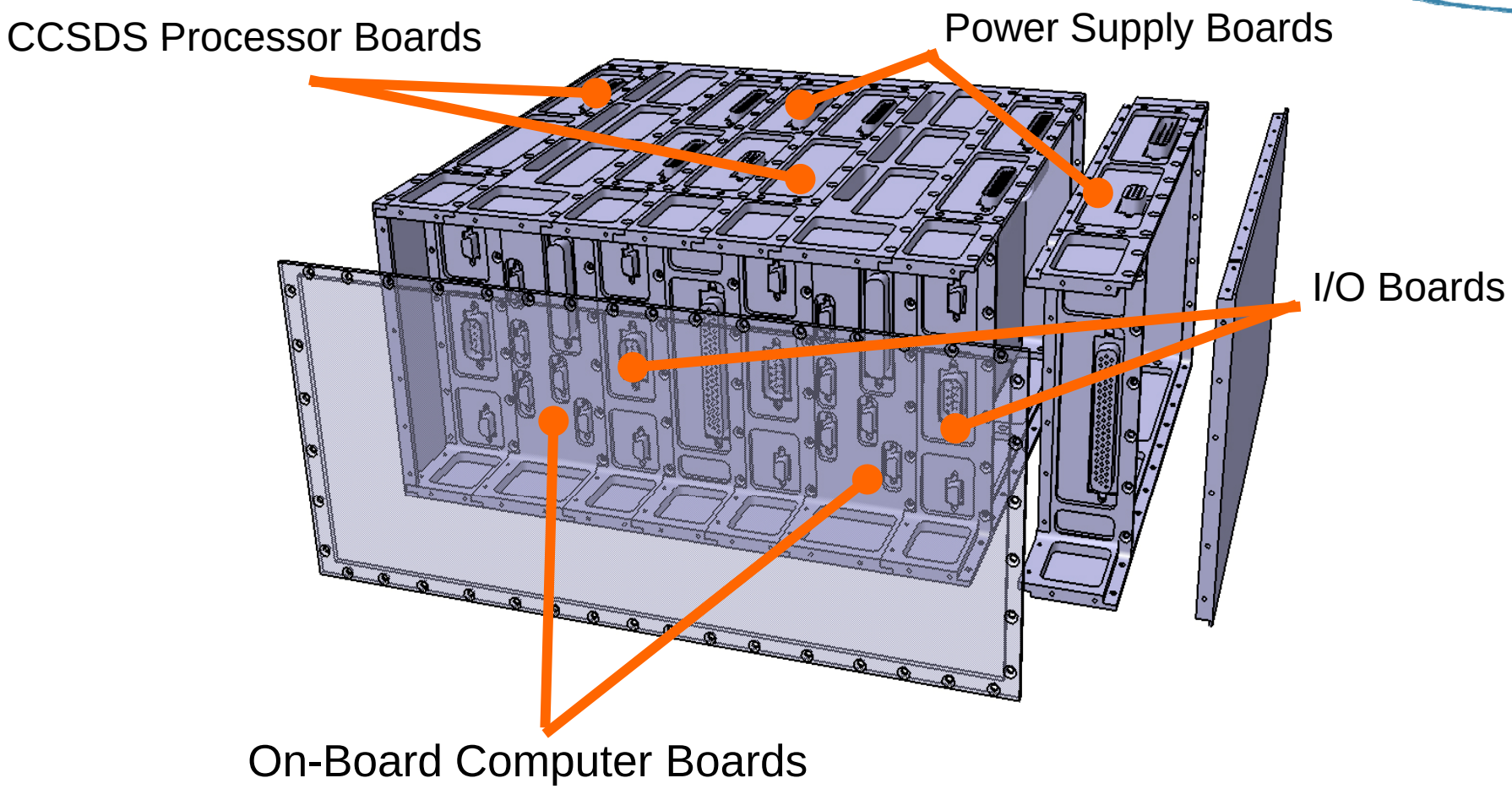
FLP Spacecraft Electrical Block Diagram



Flying-Laptop Onboard Computer



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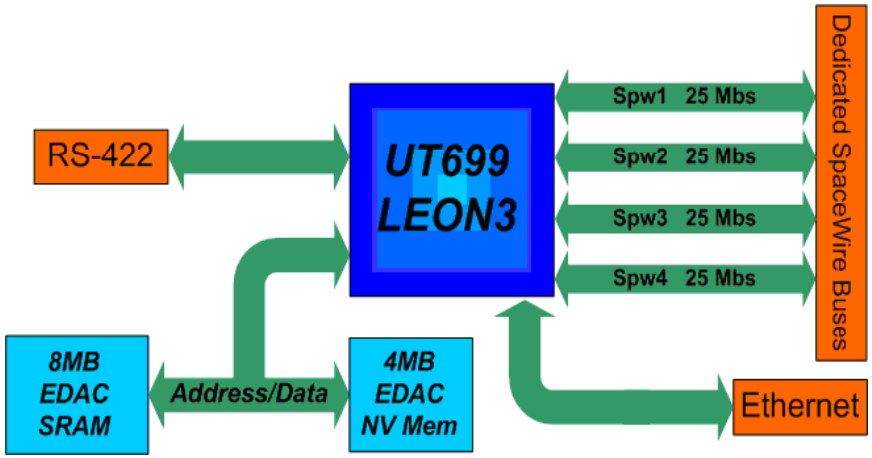
Onboard Computer Board

- **Eurocard size single board computer based on UT699 LEON3FT device, operating at 33 MHz**
- **4 MB NV RAM, 8 MB SRAM**
- **4 SpaceWire interfaces (2x CCSDS board, 2x I/O Board)**
- **1x UART (OBSW Service I/F)**
- **1x 44 Pin mixed connector with JTAG, Power Supply, etc.**

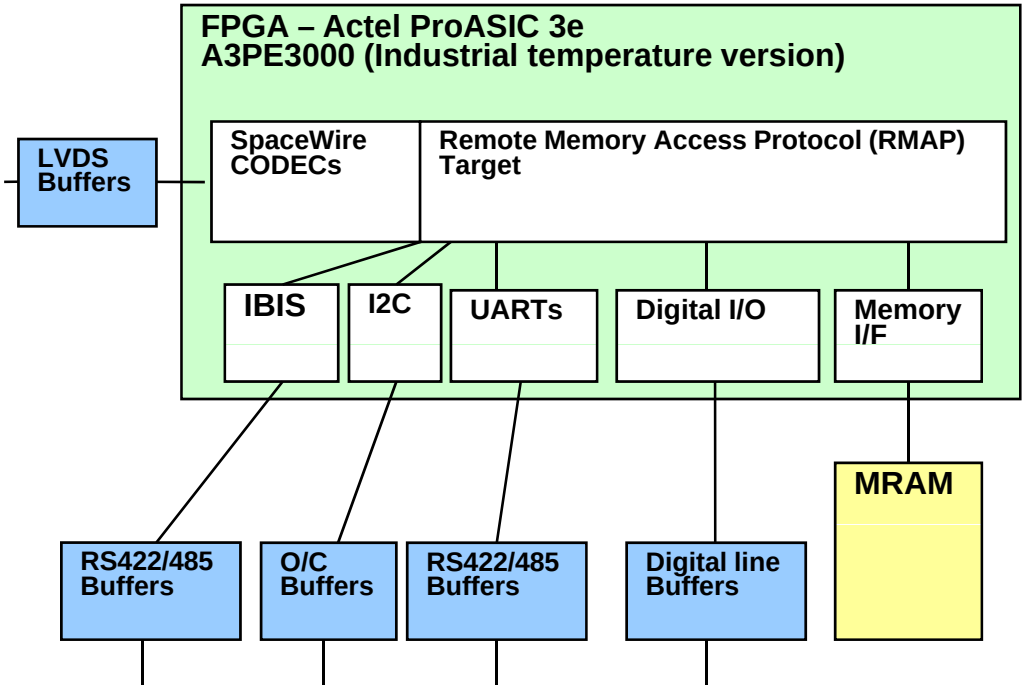


Information from DASIA 2011 presentation by Astrium

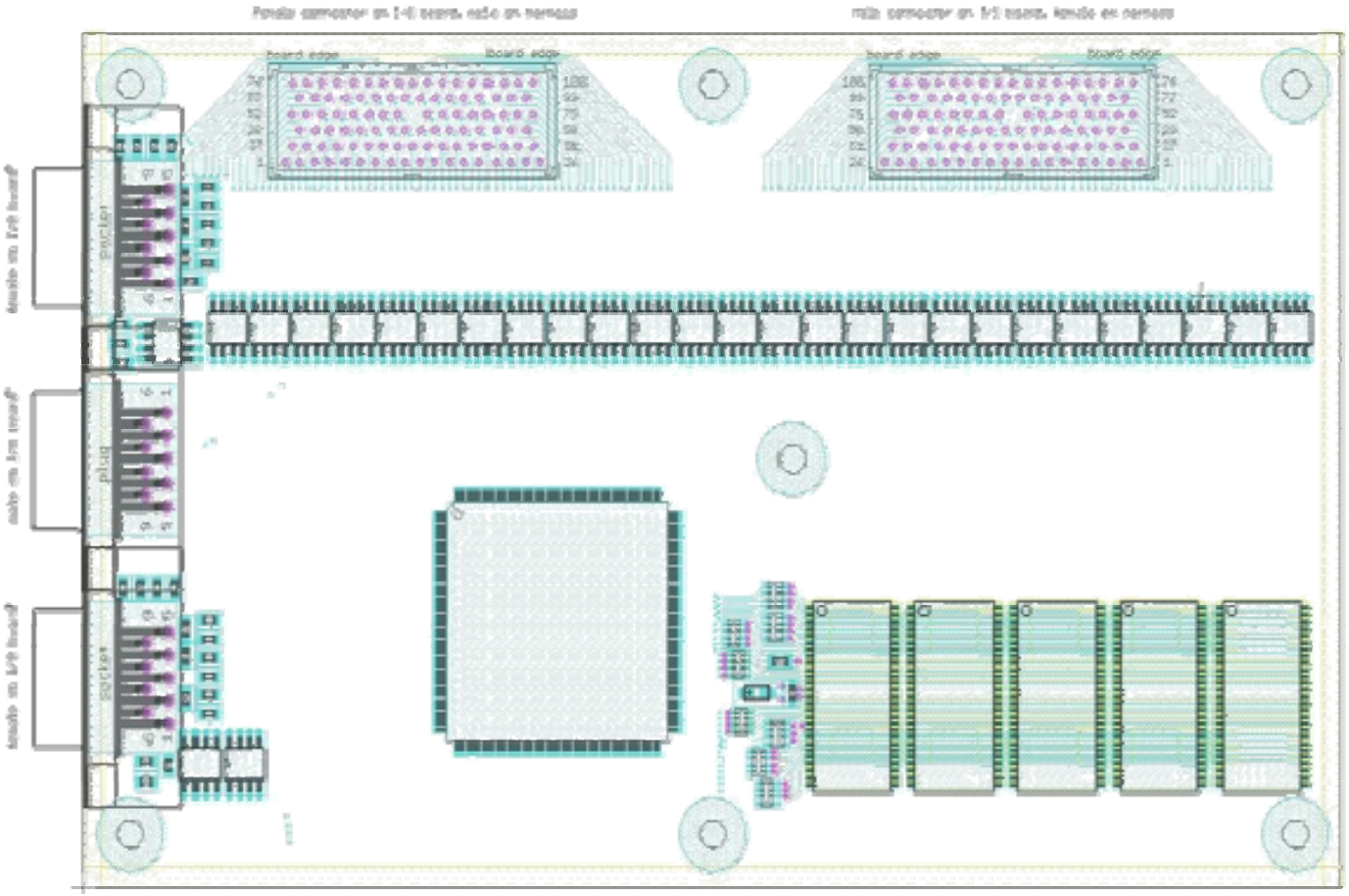
I/O Board

- I/O boards form the bridge btw OBC and S/C
- I/O-boards mimic the digital interface function of a RIU
- The I/O boards are connected to the OBC boards via a SpaceWire connection running the RMAP protocol
- The I/O board are developed by 4Links Ltd., UK.
- The I/O boards SpaceWire functionality and data routing between SpW and the low level I/O and bus interfaces is implemented in a ProAsic3 FPGA
- I/O board incorporates MRAM for S/C HK TM storage and for S/C state vector storage for reconfigurations
- Generic board design with I/Fs and SpW and central ProAsic3 FPGA and also used for CCSDS processor

I/O Board block diagram



I/O Board PCB layout (Draft)



Information from DASIA 2011 presentation by Astrium

CCSDS Processor Board

- FLP applies CCSDS/PUS standards for S/C command and control
- To implement this, the FLP is equipped with a CCSDS processor built on the same basic PCB design and ProAsic3 FPGA as the I/O Board
- CCSDS board manufactured by 4Links Ltd.
- CCSDS IP cores designed by Aeroflex Gaisler
- CCSDS processor breadboard from Aeroflex Gaisler

CCSDS SpacePackets over SpaceWire

Aeroflex Gaisler has developed a method to transfer CCSDS Space Packets over SpaceWire links based on Remote Memory Access Protocol (RMAP).

The Space Packet is transferred as part of the data field of the RMAP write command. The write access is done to memory areas in the target that are dedicated to different Packet Telemetry Virtual Channels. The success of the transfer is acknowledged by an optional RMAP reply.

The Space Packet is protected by means of the RMAP data field CRC. Additionally, the RMAP command header (containing the addressing information, e.g. for Virtual Channel routing) is protected by means of CRC.

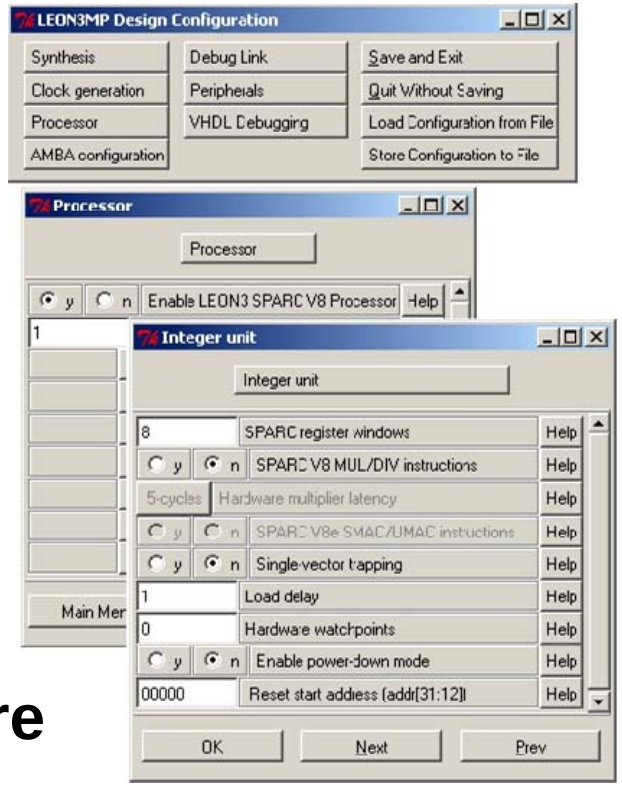
GRLIB IP core library

GRLIB is a complete design environment:

- Processors
- Peripherals
- Serial interfaces
- Parallel interfaces
- Memory controllers
- AMBA on-chip bus with Plug & Play support
- Fault tolerant & standard version

Support for tools & prototyping boards

Portability between technologies:
Actel, Aeroflex, Altera, Artisan, Atmel, DARE, eASIC/Nextreme, Eclipse, Lattice, Synopsys DesignWare Ramon Chips / RadSafe, TSMC, UMC, Virage, Xilinx, etc.



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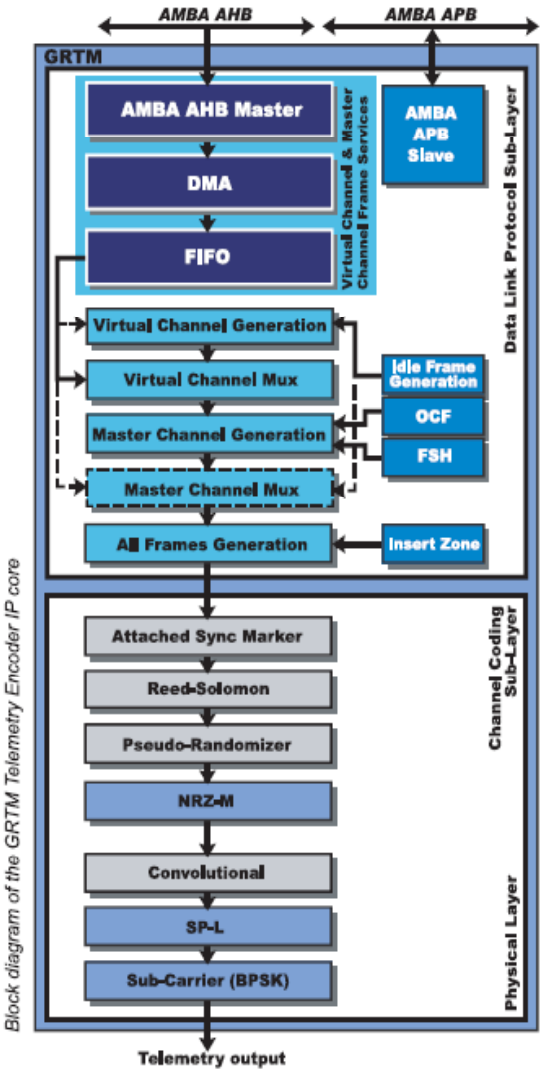
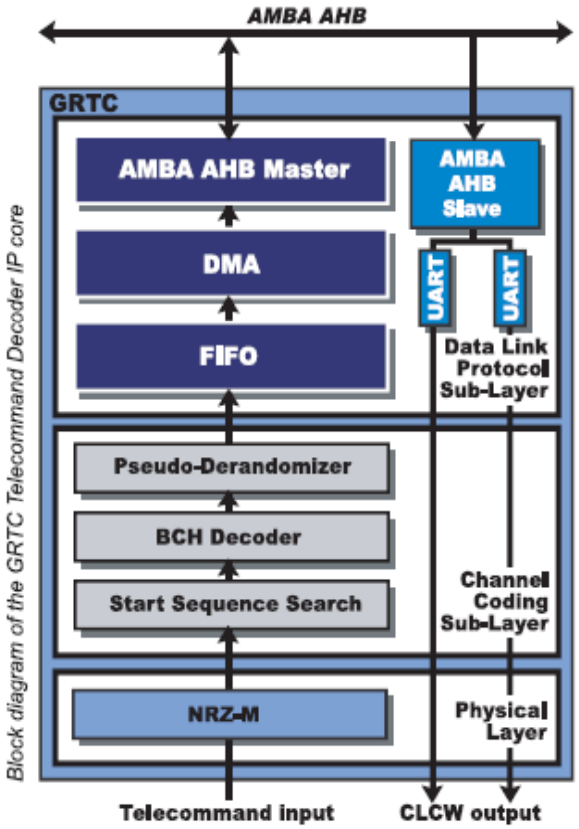
GRTM Encoder & GRTC Decoder IP cores





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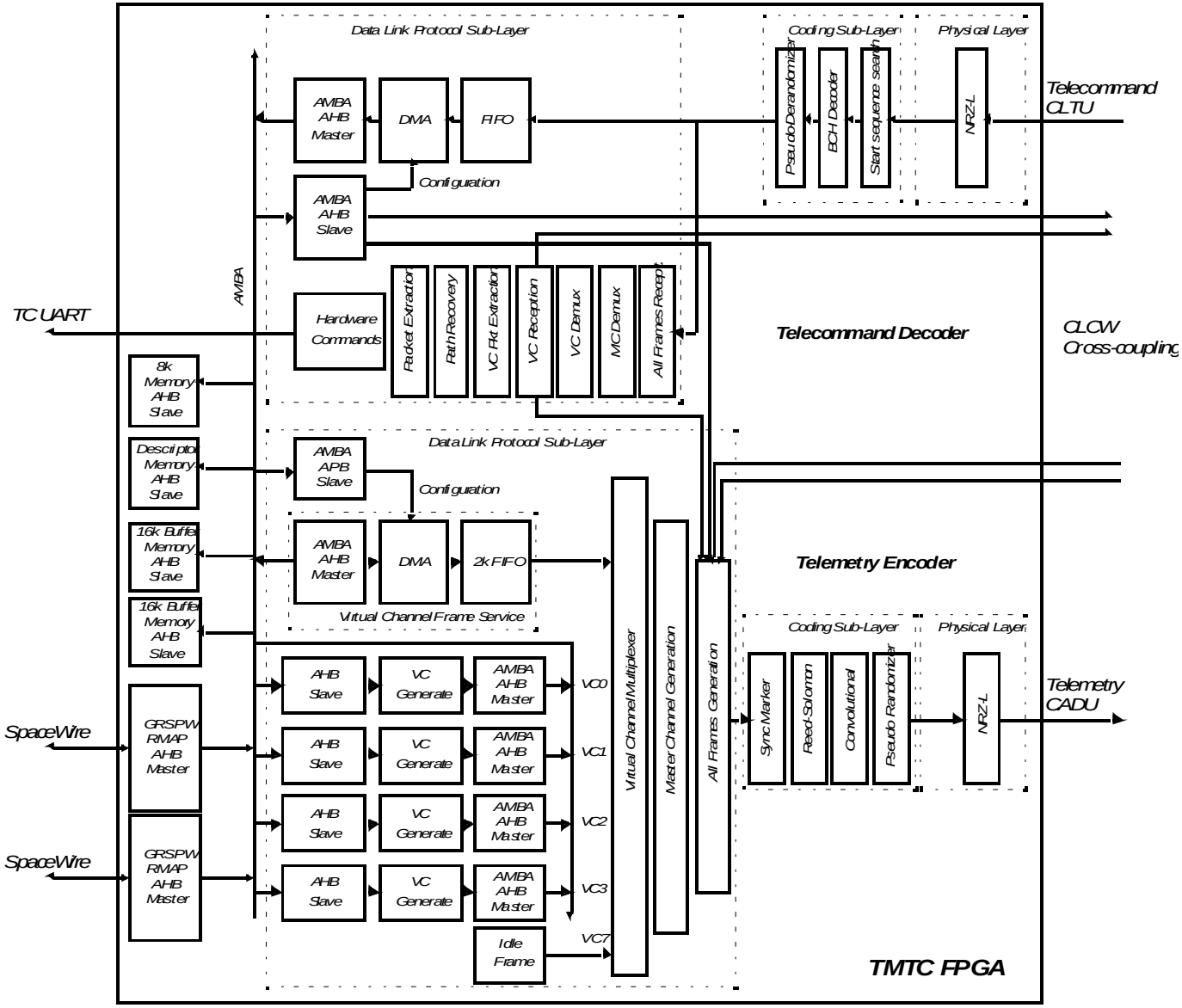
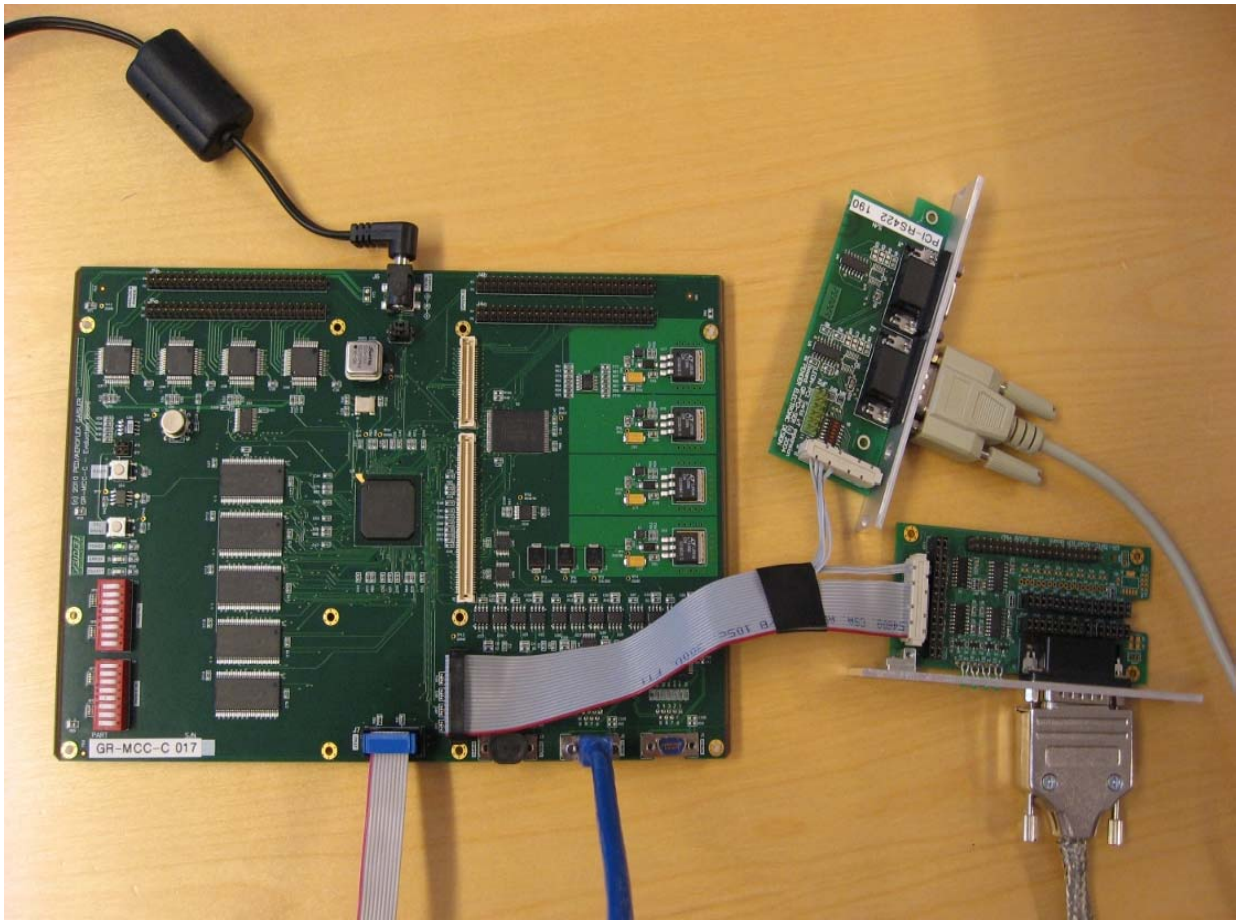
CCSDS TC Decoder / TM Encoder FPGA



CCSDS TM/TC breadboard



GR-MCC-C + GR-TMTC-ADAPTER + GR-CPCI-RS422

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Conclusions

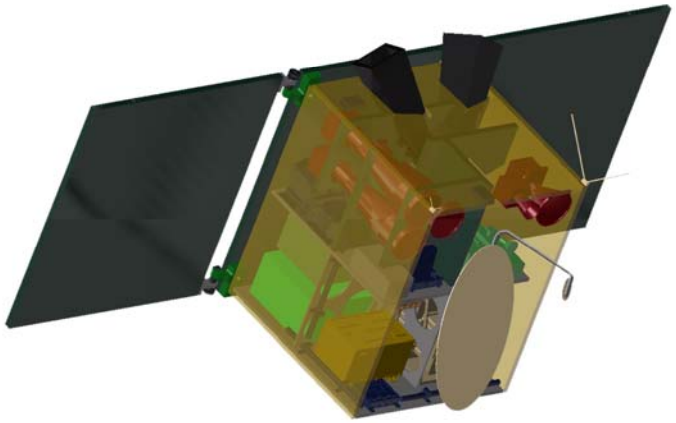
- The re-programmable ProASIC3 FPGA technology fits well in applications with low radiation requirements.
- The in-situ programmability enables the development of highly miniaturized systems which can be adapted to customers needs late in the development cycle.
- Porting a combined SpaceWire and CCSDS system to Flash-based FPGA technology went smoothly, with much of the IP core library work already done.
- Main processing power located in UT699 device, with peripheral functions such as I/O and CCSDS processing implemented in custom designed FPGAs.

Contact information

- **Processor and IP core information:**
  http://www.Aeroflex.com/Gaisler

- **Board and component information:**
  http://www.4Links.com

- **Flying Laptop information:**
  http://www.kleinsatelliten.de/index.php/en/flying-laptop.html



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