Experiments With A Multicore Onboard Architecture and Near Realtime Configurability

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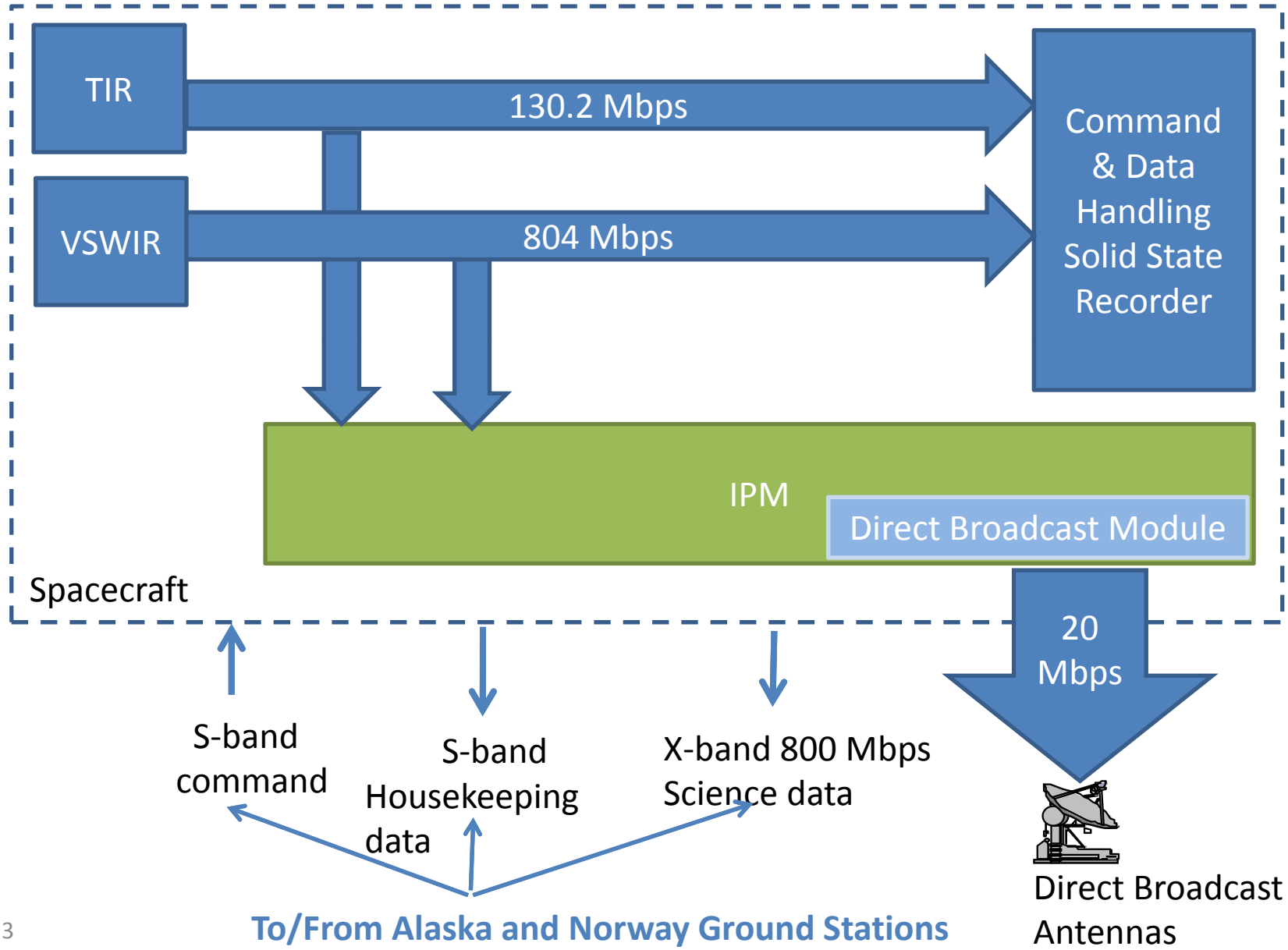
Objectives

- Dramatically improve onboard processing for high data rate NASA Decadal Survey missions, in particular, HyspIRI
- Make use of the Maestro board and augment with Field Programmable Gate Array(FPGA) technology to raise the TRL for onboard applications via the use of this multicore processor technology
  - Obtain experience on Maestro (7 x 7 tile array) with long term objective to port to Maestro-lite, a low powered version with 4 x 4 tile array
- Demonstrate the end-to-end operations concept for use of the Intelligent Payload Module (IPM) for low latency users of NASA Decadal Survey missions
  - Multi-tiered onboard data processing chain
  - Level 2 data products with atmospheric correction and geocorrection directly downloaded based on user selected subset of data and user selected location
  - Rapid delivery of data products in near realtime for quick-looks

HyspIRI Low Latency Data Flow Operations Concept



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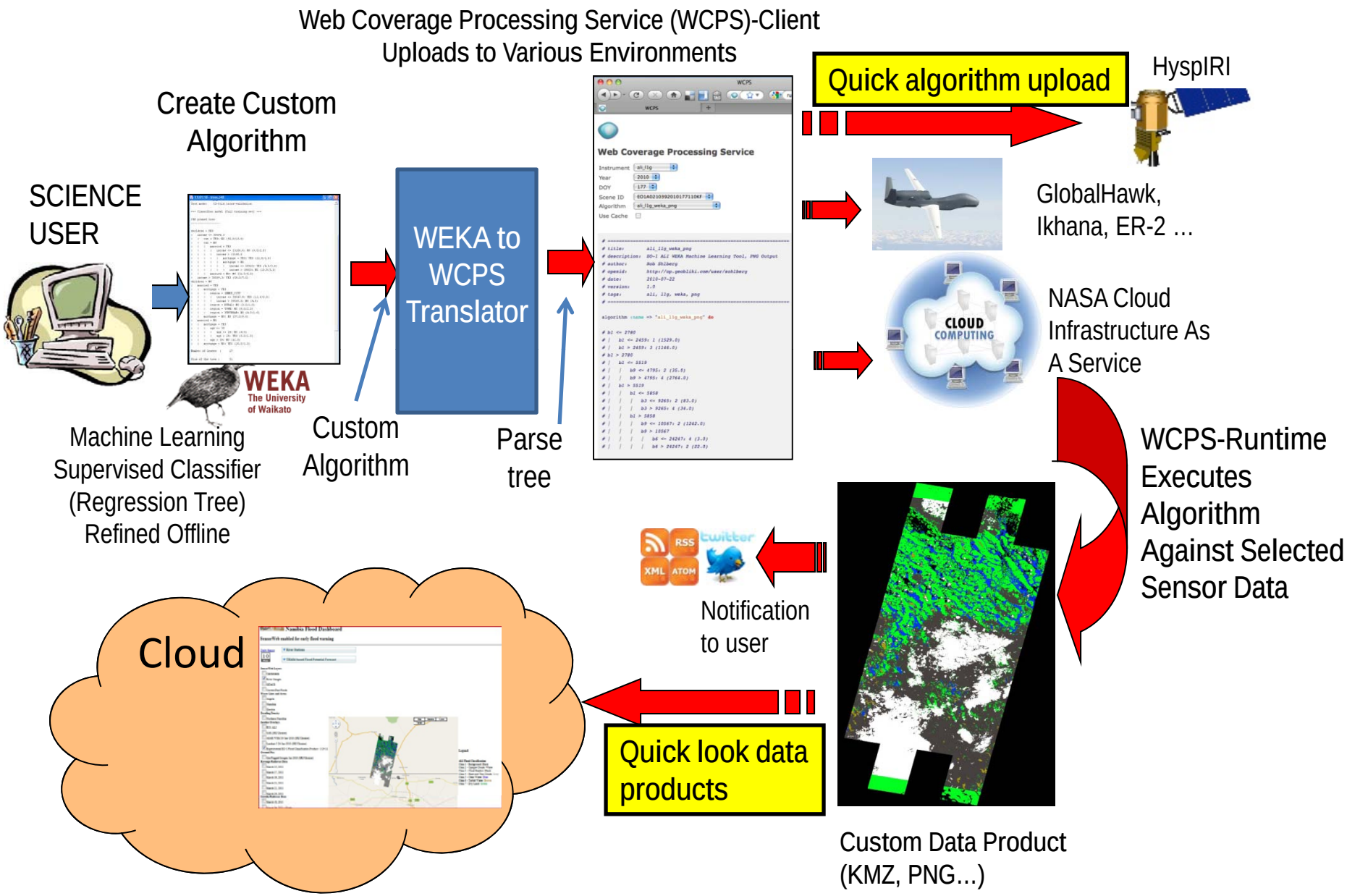
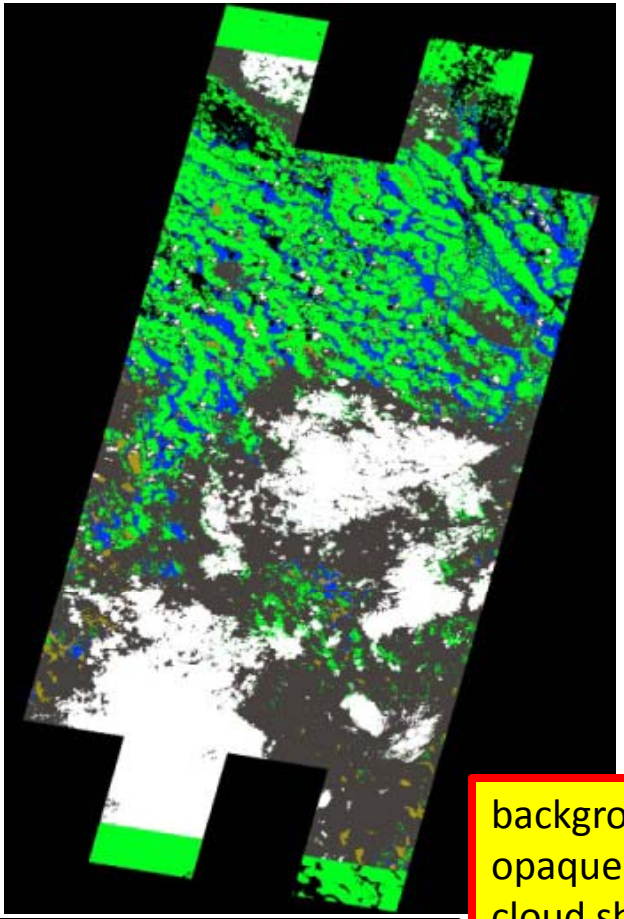
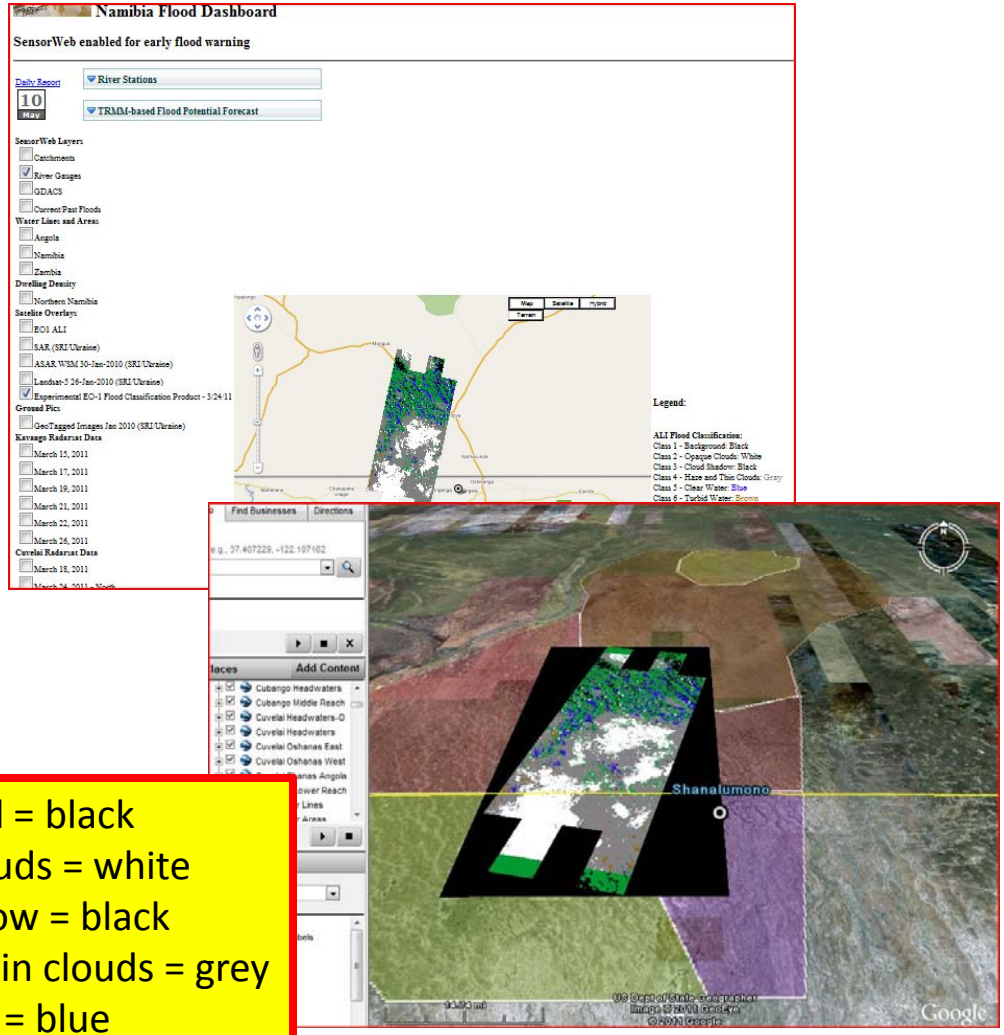
Experimental IPM Quick Load/Quick Look Ops Con



Example of IPM Flight Testbed Produce Data Product Loaded onto the Ground-based Flood Dashboard

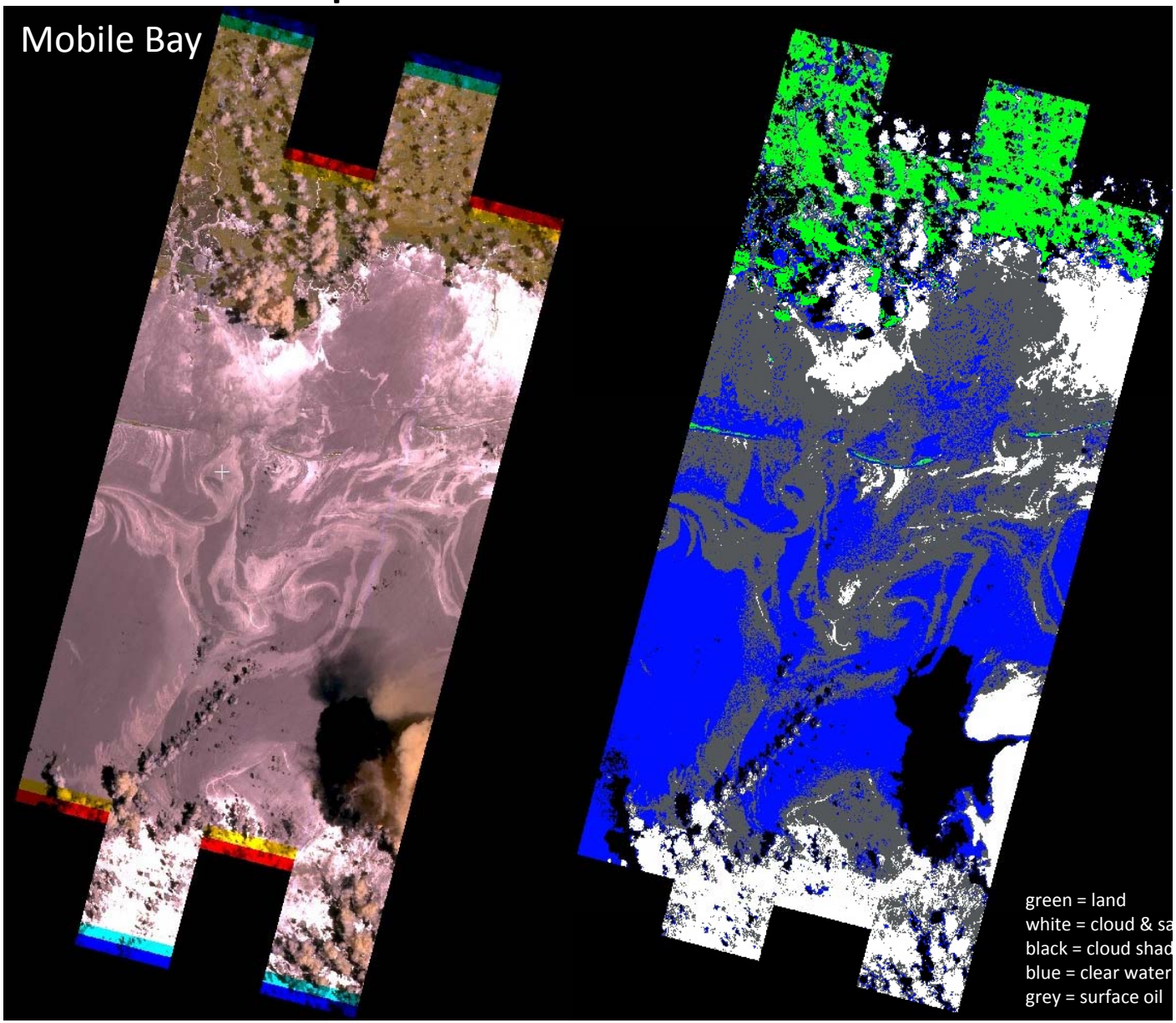




Flood Classification using WEKA tool and WCPS for Oshanas area in Namibia 3-24-11

background = black
opaque clouds = white
cloud shadow = black
haze and thin clouds = grey
clear water = blue
turbid water = brown
dry land = green

Another Example of Customized IPM Data Product



EO-1 ALI False Color Enhanced for Oil Sheen

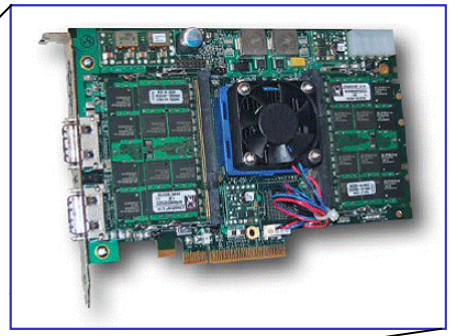
Oil Classification Output Product

Current Activities

- Build up HyspIRI IPM Testbed in the lab and boxing it up for airborne flights
  - Demonstrate Hybrid Field Programmable Gate Arrays (SpaceCube) and Tilera Multi-core Processor Architecture
    - Leveraging Advanced Hybrid On-Board Data Processor - SpaceCube 2.0 developed under ESTO AIST 2008
- Develop Advanced Software For Hyperspectral and Thermal Image Processing
  - High Data Throughput Processing Using [reconfigurable] FPGAs and MicroBlazes
  - Low-Latency Level 2 Image Processing
    - High Speed Onboard Atmospheric Correction
      - SBIR 2010, Spectral Sciences/Vightel
    - Georectification
    - Level 2 products based on user-driven custom algorithms
      - Web Coverage Processing Service (WCPS) developed under ESTO AIST 2008
  - Automatic parallelization of software using the AESOP compiler
    - NSRTF11 Fellowship Award, UMD
- Demonstrate Software Defined Radio for Ground to Space communication.
- Ground Data Processing and Long Term Storage using Cloud Computing Environment Infrastructure
  - Provided by the Open Cloud Consortium's Open Science Data Cloud

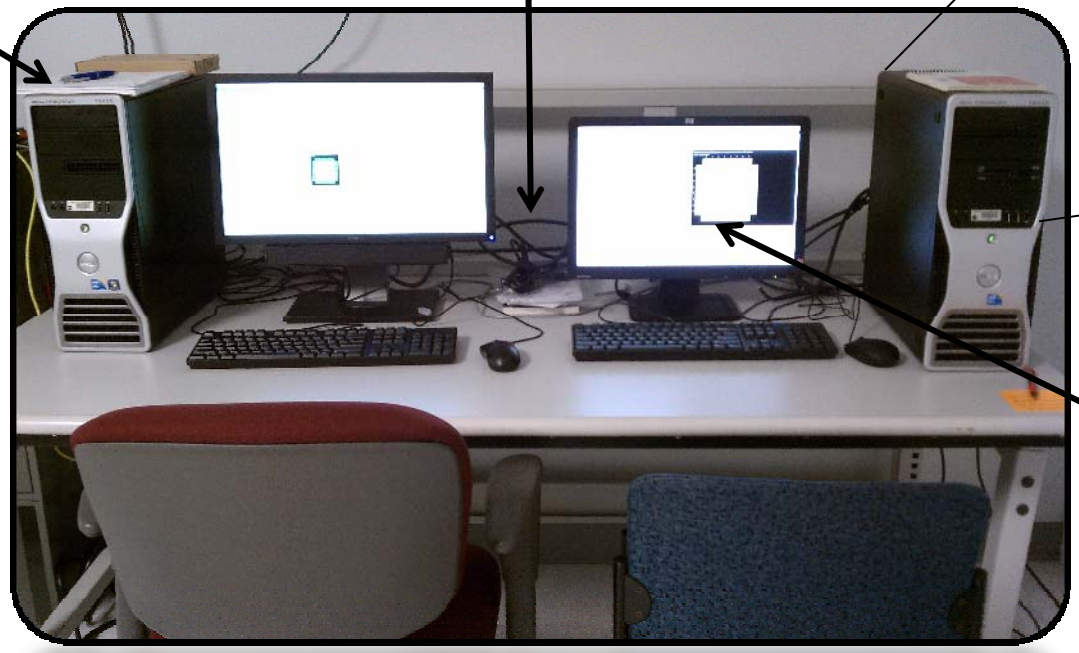
Initial IPM Testbed with Tilera Acting as Proxy for Maestro & Maestro-lite Board

TILExpress 20G



10GE Point to Point

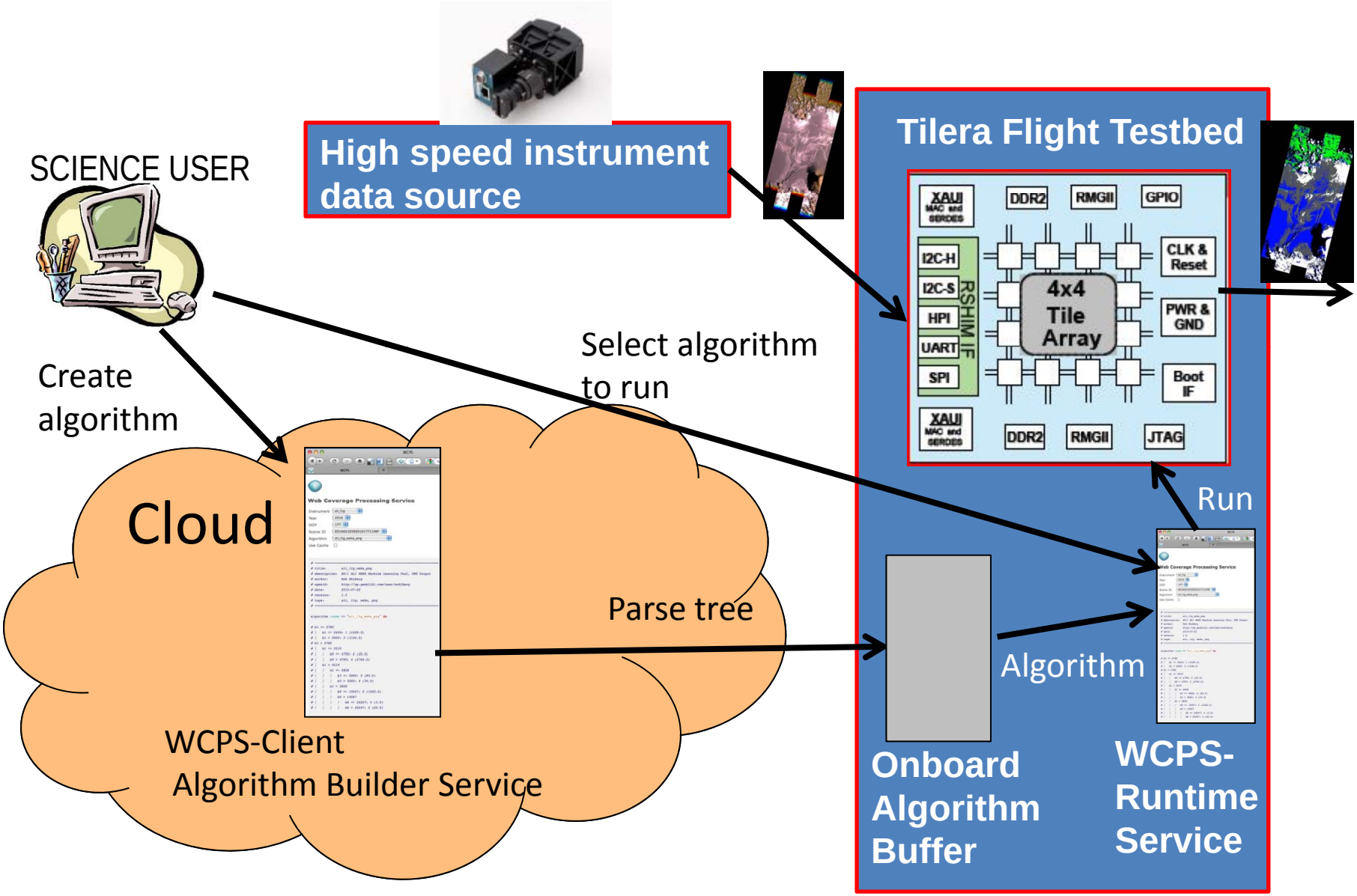
Data Simulator



Tilera Multicore Development Environment

IPM Tilera Flight Testbed Ops Con

(Tilera board is proxy for Maestro and Maestro-lite)



Initial Benchmark Tests Using Single Processor on Tilera Board and Comparing to SpaceCube (Xilinx Virtex 5 FPGA) Single Processor

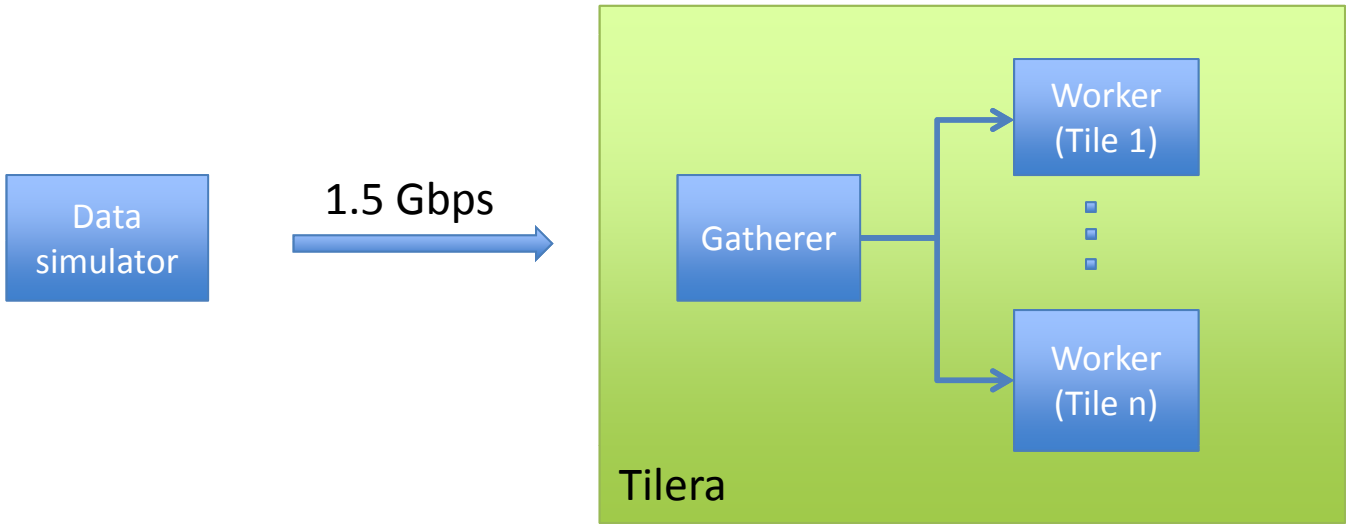
**Note that this was a preliminary learning experience and thus SpaceCube and Tilera were not optimized.

Algorithms		EO1 scene (256x1000 pixels)				HyspIRI 1/4 swath (640x565 pixels)		
		*SpaceCube Linux (ms)	*SpaceCube Standalone (ms)	**Tilera Linux single core(ms)		SpaceCube Linux (ms)	SpaceCube Standalone (ms)	**Tilera Linux single core(ms)
Cloud		1791	431	412		2170	589	558
Flood		3024	937	1072		3782	1311	1489
SWIL		7350	2872	3927		10226	4058	5555
Sulfur		116362	29515	88210		164978	42026	126592
Thermal		1103	304	736		1475	431	1034
SIWI		580	44	45		823	62	64
NDVI		630	44	45		904	62	64
NDWI		589	44	45		836	62	64

* SpaceCube – Virtex5 FPGA with a PPC design running at 400MHz
- -Version Linux - runs Linux on Xilinx board (C code compiled in Linux)
- -Version Standalone running natively on Xilinx board without Linux (C code compiled using Xilinx native cross compiler)

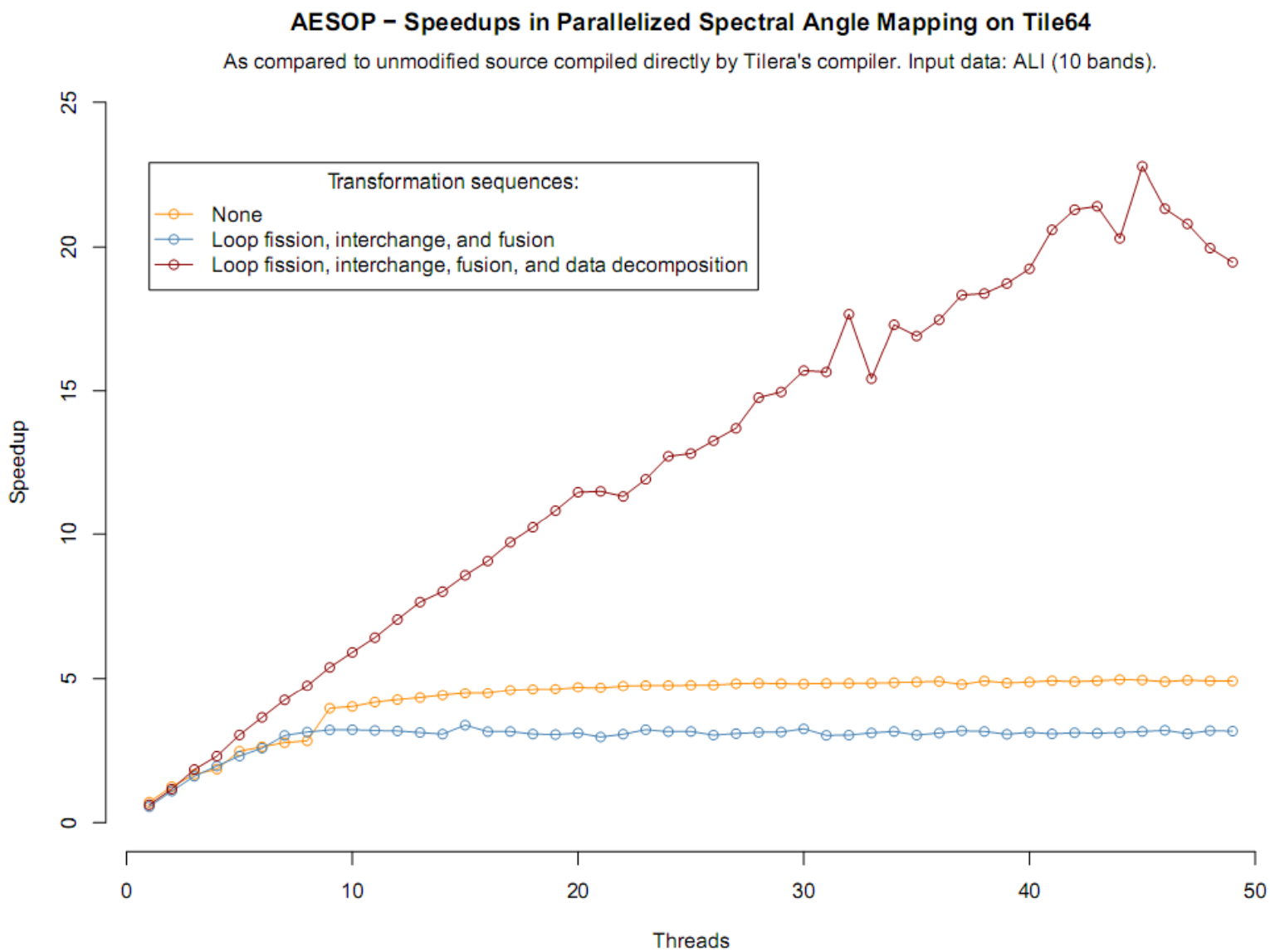
** Tilera – 700MHz Tile Processor using only one processor of the 64 available processors

Extend Tests to Make Use of Parallel Processing

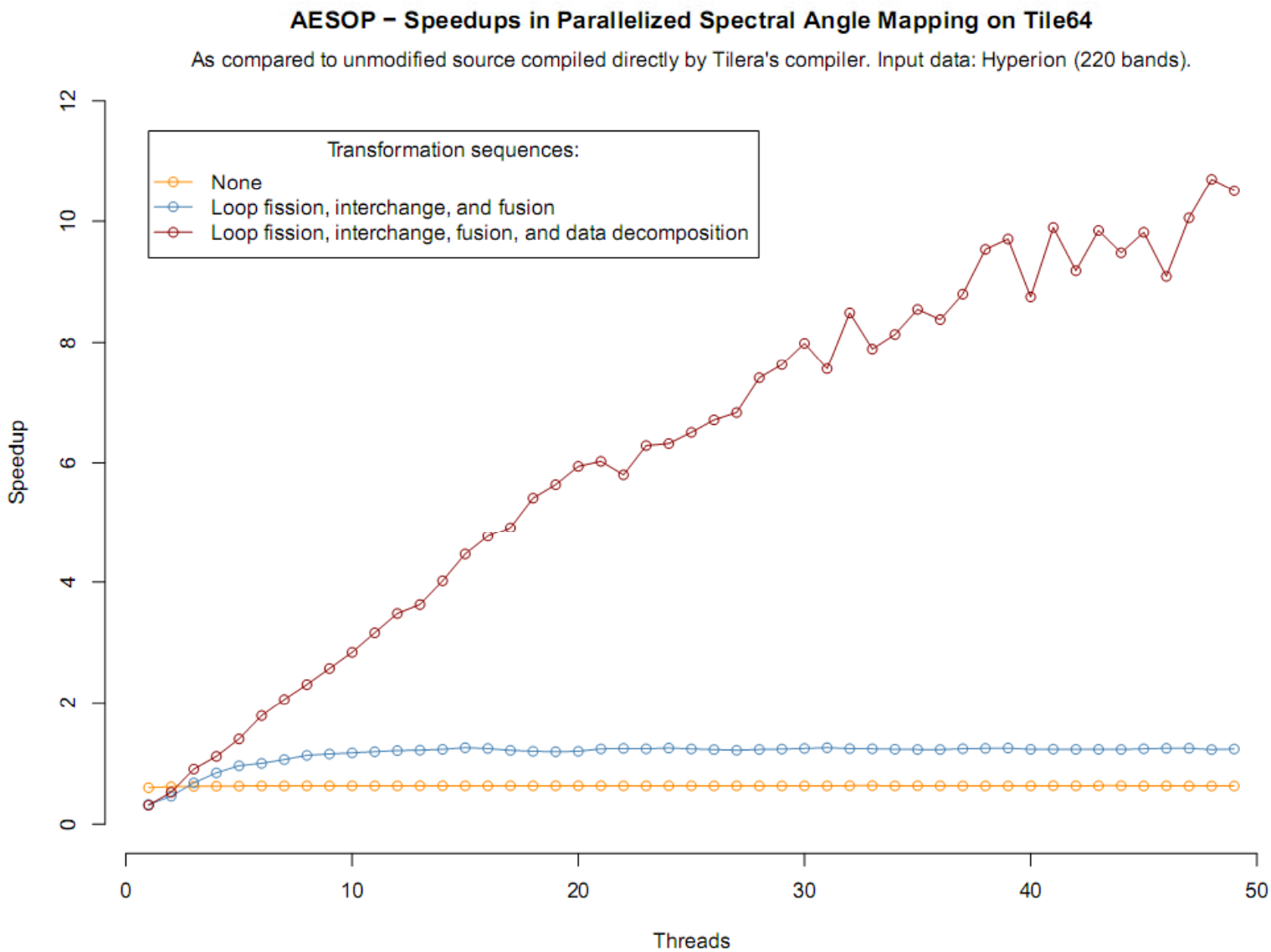


- Transmitting data over the 10GbE interface from a data simulator PC to the Tilera board.
- Distributing an algorithm to multiple tiles. Task parallelism can be achieved with speedup approaches to the number of tiles assuming:
  1) The algorithm works on each data element independently
  2) The size of the data is equal to the Tile cache size.
- Target is to add a 10X to 20X speed improvement with compiler optimization.

AESOP Parallelization Test Results (1 of 3)



AESOP Parallelization Test Results (2 of 3)



AESOP Parallelization Test Results (3 of 3)

Speedups for Spectral Angle Mapping (SAM) detecting murky water on an EO1 ALI and Hyperion scene

Loop fusion, fission, and decomposition are standard techniques, but they must be intelligently applied only when legal and when beneficial to performance.

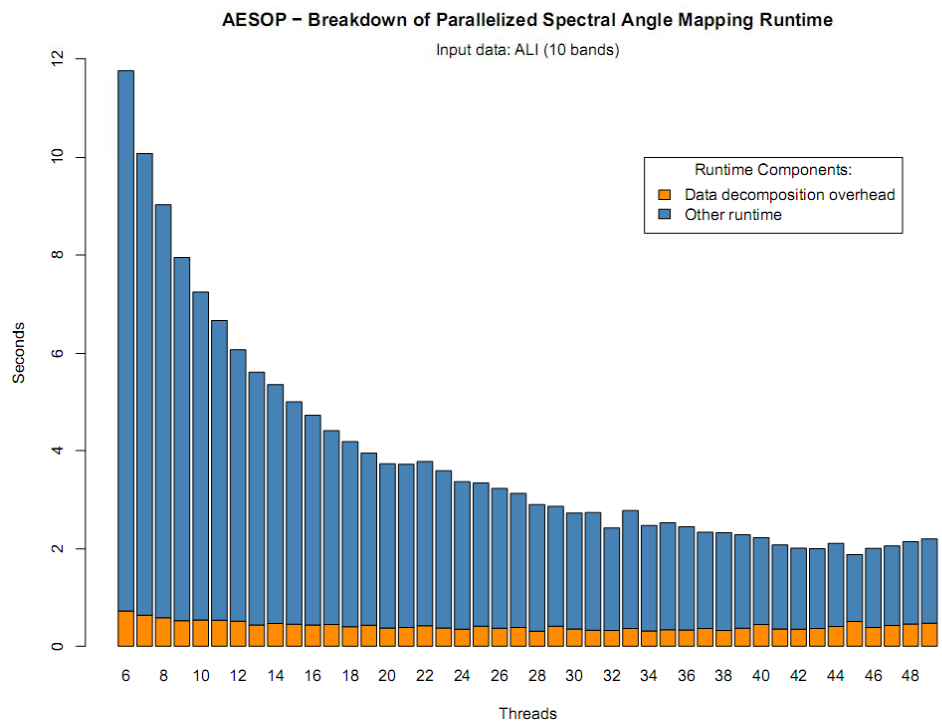
* Loop fusion: combining two loops with identical iteration space into one single loop with the same iteration space. In some cases this may improve granularity of parallelization and reduce control overhead, but in other cases it may hurt data locality.

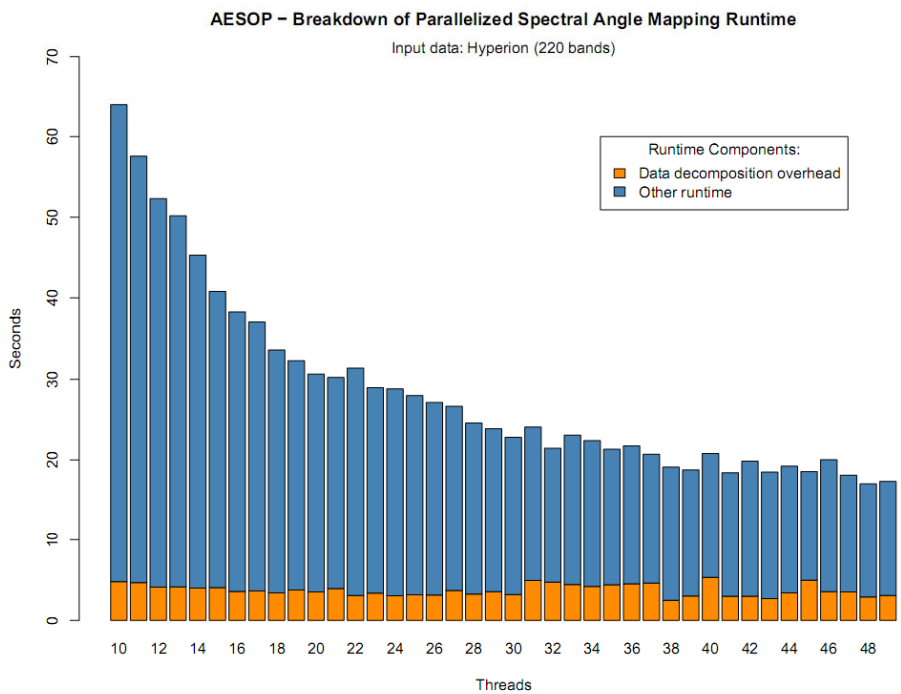
* Loop fission: splitting a single loop into a pair of loops with identical iteration space, but with the body of the original loop distributed between the pair. The effects of loop fission are opposite those of loop fusion.

* Data decomposition is also a standard technique, but it is usually reserved for distributed-memory parallelization. This strategy involves splitting large data structures into partitions which are each more local in some way to the processor which will be accessing them. Conventional SMP processors do not benefit from this, but for Tile64 this is crucial for performance due to differences in its cache subsystem.

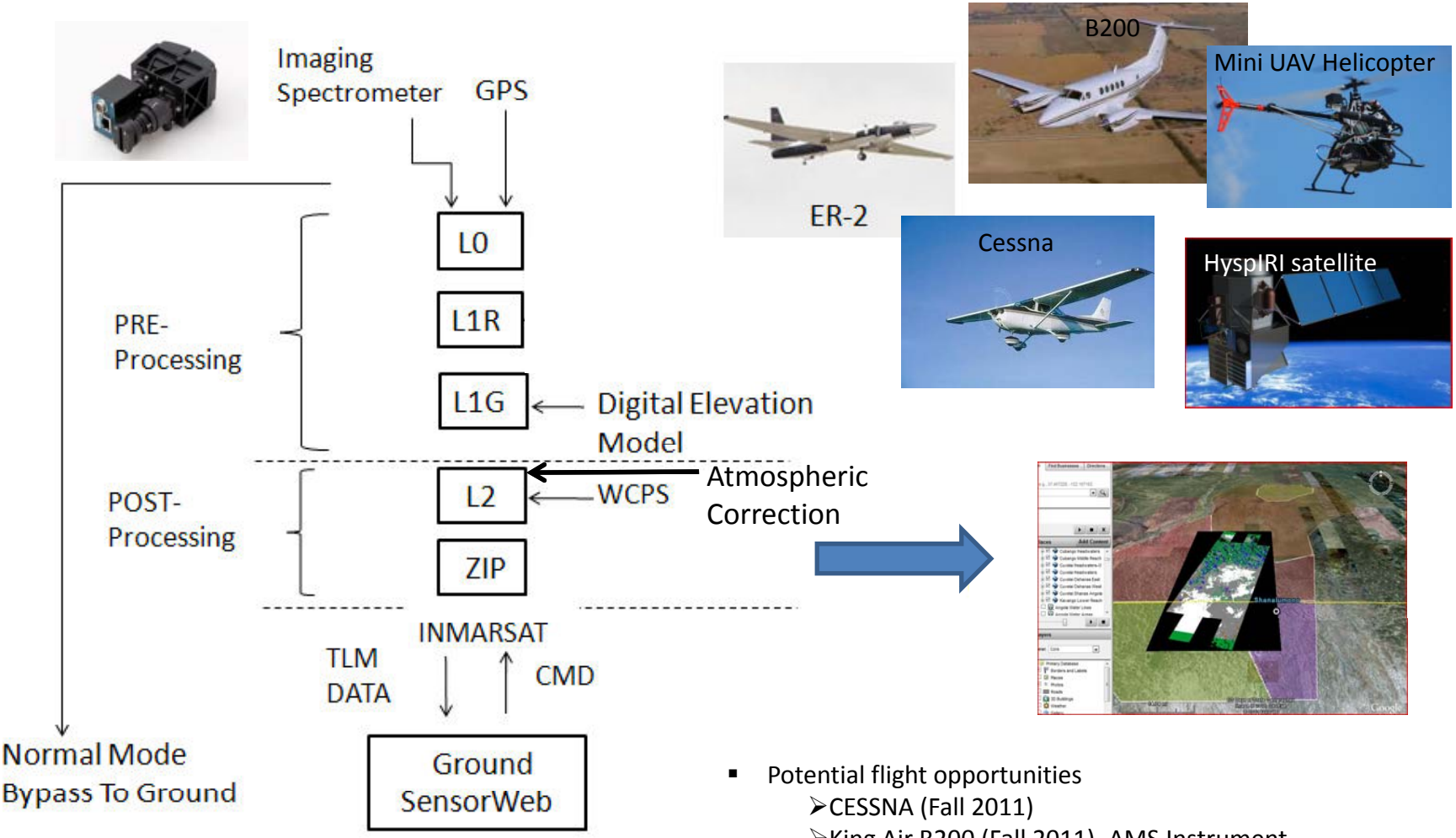
Note: that in this case AESOP runtime at 1 thread is slower than that of native compilation; speedups in this graphic are scaled down accordingly.

Breakdown of EO1 ALI and Hyperion scene processing runtime showing the amount of time spent copying shared data into locally cacheable allocations is serialized by the hardware





Presently Working on Airborne Testbed Scenario



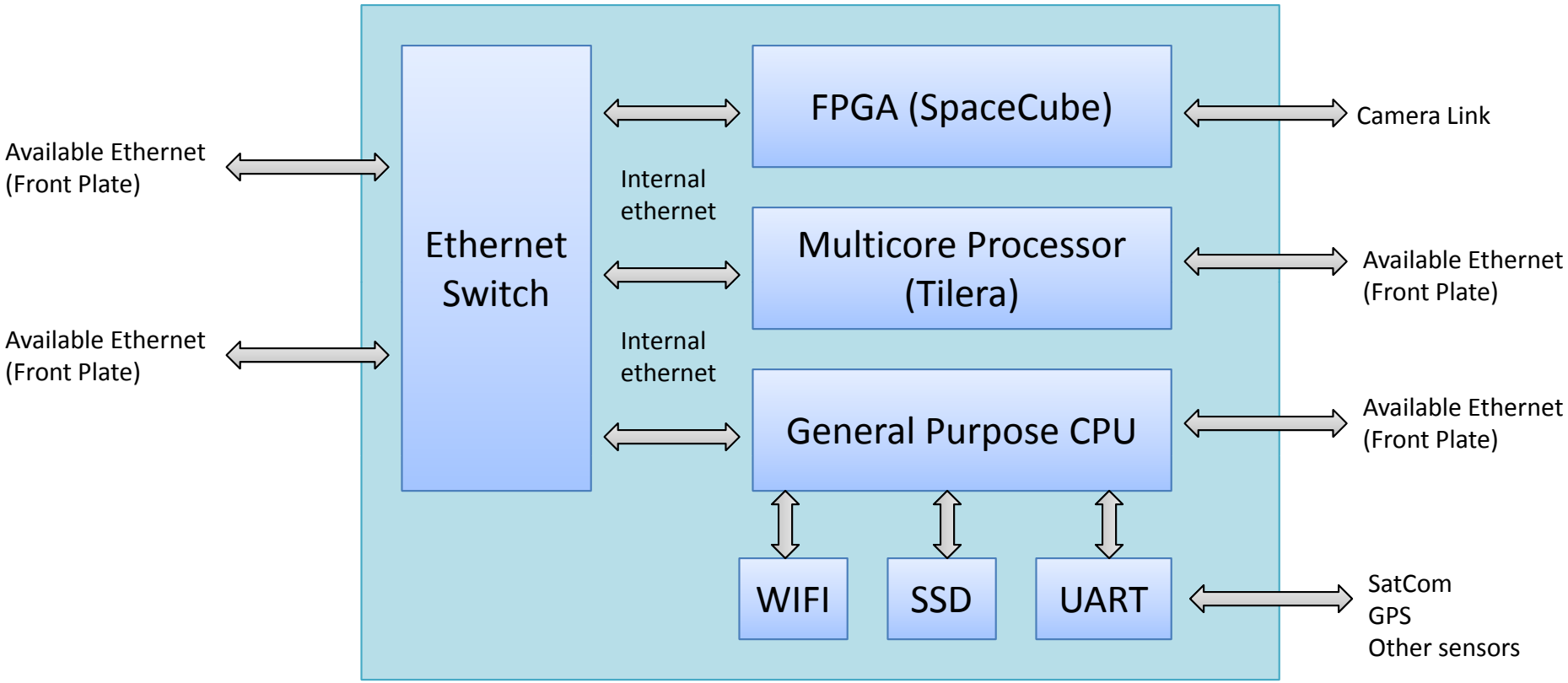
- Potential flight opportunities
  - CESSNA (Fall 2011)
  - King Air B200 (Fall 2011), AMS Instrument
  - ER2 (Fall 2012), eMAS Instrument
  - UAV Helicopter TBS

IPM Testbed Features

- Xilinx Virtex5Q FPGA for dedicated high-speed processing (band stripping, compression). **A precursor to the SpaceCube 2** which utilizes the Virtex5QV FPGA
- Tilera TILE64/TILEPro64 processor for dynamic software functions and algorithms that take advantage of symmetric multiprocessing. **A precursor to radiation hardened Maestro**
- Solid State Storage
- Camera Link (High Speed Instrument) interface
- Gigabit Ethernet interface

- Hyperspectral Instrument Demonstration
  - Brandywine Compact Hyperspectral Advanced Imager

IPM Architecture

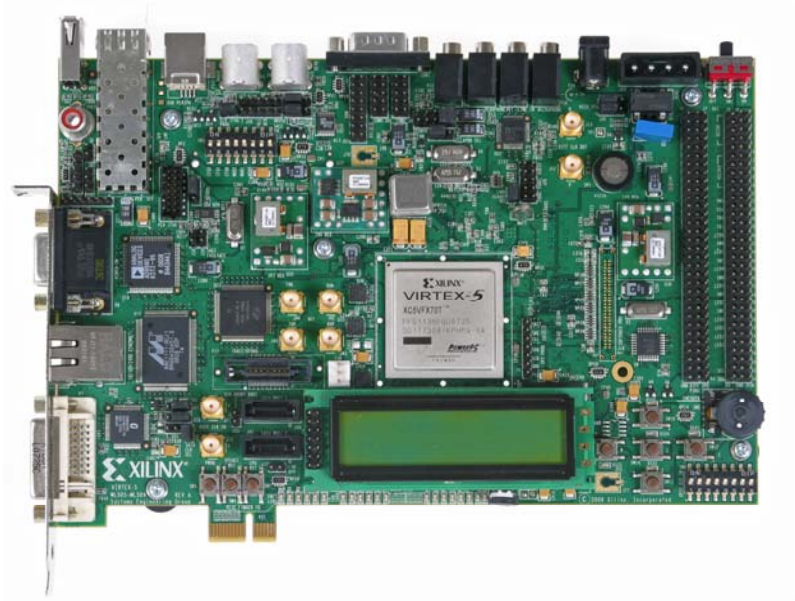


* Not the final configuration

Xilinx ML507

Key Features

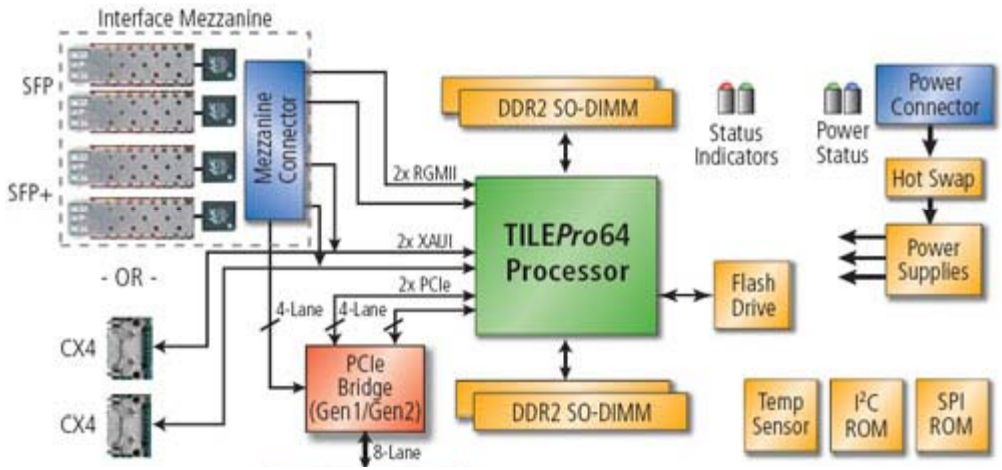
- XC5VFX70TFFG1136
- DDR2 SODIMM (256 MB)
- ZBT SRAM (1 MB)
- Linear Flash (32 MB)
- System ACE™ CF technology (CompactFlash)
- Platform Flash
- SPI Flash
- JTAG programming interface
- External clocking (2 differential pairs)
- USB (2) – host and peripheral
- PS/2 (2) – keyboard, mouse
- RJ-45 – 10/100/1000 networking
- RS-232 (Male) – serial port
- Audio In (2) – line, microphone
- Audio Out (2) – line, amp, SPDIF, piezo speaker
- Rotary encoder
- Video Input
- Video (DVI/VGA) output
- Single-ended and differential I/O expansion
- GPIO DIP switch (8), LEDs (8), and push buttons (5)
- MII, GMII, RGMII, and SGMII Ethernet PHY interfaces
- PCI Express® edge connector (x1 Endpoint)
- GTX: SFP (1000Base-X)
- GTX: SMA (RX and TX differential pairs)
- GTX: SGMII



- GTX: PCIe™
- GTX: SATA (dual host connections)
- GTX clock synthesis chips
- Header for second serial port
- Second Platform Flash PROM (32 Mb) for large device
- Mictor trace port
- BDM debug port
- Soft touch port

* Camera Link support via the expansion header

Tilera TILEncorePro-64



Specifications

General	• Form factor: Full-height, half-length, two-slot PCI Express • RoHS-6 compliant per EU 2002/95/EC • All components NEBS compliant
PCIe Interface	• Eight-lane PCIe 2.0, Gen2 compliant • Fall-back to 4, 2, or 1 lane. Fall-back to Gen1 mode • Hot plug compliant

Network Interfaces	• Multiple interface configurations:
	  • Two 10Gbps Gigabit Ethernet (25-pin CX4)
	  • Two 10Gbps SFP+ and two 1Gbps SFP (Mezzanine)
	• Can be used in co-processor mode with interfaces disabled

Memory	• Four SO-DIMM sockets for DDR2 SDRAM • PC2-6400 (DDR2-800), 1GB to 16GB total capacity • 1 GByte on-board Flash drive
Indicators	• Four on-board power supply status indicators • LEDs on rear plate for link status

Technical Features	• Supports INTx and MSI interrupts across PCI • On-board dual temperature sensor • JTAG test connector • Mezzanine expansion connector

Power	• Standard 4-pin "ATX" connector for power
	• Single 12V supply from ATX connector
	• Typical power dissipation: 50W @ 700 MHz
	• Cooling options:
	  • Active cooling fan (Standard)
	  • Passive heatsink†
	  • Required airflow: 1.1 m/s (200 lfm) @55°C

Environmental	• Operating Temperature: 0° to 55°C • Storage Temperature: -40° to 70°C • Humidity: 10% to 90% RH non-condensing
Physical Specifications	• Board Height: 11.1 cm (4.38 in) • Board Length: 16.8 cm (6.6 in) • Bracket Height: 12cm (4.72 in)

†Passive heatsink for 700MHz version only.

Netgear GS105 Gigabit Switch

Key Features

Network Management Type	Unmanaged
Jumbo Frames	Yes
Speed	10/100/1000 Mbps
MAC Address Table	4000
Buffer Memory	128K On-Chip Packet Buffering
Switch Method	Store and Forward
PoE	No
Stackable	No
SNMP	No
QoS	No
LACP	No
Layer	2
Port Mirroring	No
Module Support	No
VLAN Support	No
Power	12W, 12V, 1A
Dimensions	3.7" x 4.1" x 1.1“
Weight	0.7 lbs
Temperature	0ºC to 50ºC (32ºF to 122ºF)

Networked Attached Storage via DreamPlug

DreamPlug Key Features

- Marvell® Sheeva™ Core Embedded CPU @ 1.2 GHz
- DC Consumption: 5V/3.0A supports most demanding applications
- Boot Device: 2MB SPI NOR Flash for uboot
- Flash Memory: 2 GB on board micro-SD for kernel and root file system
- SDRAM: 512MB 16bit DDR2 @800 MHz
- 2 x Gigabit Ethernet 10/100/1000 Mbps
- 2 x USB 2.0 ports (Host)
- 1 x eSATA 2.0 port- 3Gbps SATAII
- 1 x SD Socket for user expansion/application
- WiFi: 802.11 b/g
- Bluethooth: BT2.1 + EDR
- u-boot (in internal SPI NOR Flash)
- Linux distribution: Ubuntu
- Dimension: 108mm (L) x 58mm (W) x 24 mm (H)

Acomdata 2.5" Tango USB/eSATA Hard Drive Enclosure Kit

Electrical and Weight Evaluations

Board	Voltage	Power/Current	Connector
Tilera LITEncore	12v	50W (4.2A)	4p ATX Molex
Xilinx ML507	5v	15W (3A)	4p ATX Molex
GS105 Switch	12v	12W (1A)	TBD
SSDNow V100	5v	6,4W (1.3A)	SATA Slimline
Lite5 Wifi	12v	7W (0.7A)	TBD

Component	Number	Weight(g)	Total(g)	Total(oz)	Weight%
Tilera LITEncore	1	455	455	16.05	0.38
Xilinx ML507	1	350	350	12.35	0.29
M4-ATX	1	158	158	5.57	0.13
PicoUPS-120-ATV	1	20	20	0.71	0.02
Netgear GS105	1	128	128	4.52	0.11
HD-SSD	1	80	80	2.82	0.07
5GHz Wifi	1	18	18	0.63	0.01
TOTAL			1209	42.65	1.00

* Not the final configuration

Target Making Calculated Measurements on Hybrid Maestro-lite & Virtex Board to Insert in Chart Below

Flight Processor Comparison

	MIPS	Power	MIPS/W
MIL-STD-1750A	3	15W	0.2
RAD6000	35	10-20W	2.33[1]
RAD750	300	10-20W	20[2]
SPARC V8	86	1W[3]	86[3]
LEON 3FT	60	3-5W[3]	15[3]
SpaceCube 1.0	3000	5-15W	400[4]
SpaceCube 2.0	5000	10-20W	500[5]

Notes:
1 – typical, 35 MIPS at 15 watts
2 – typical, 300 MIPS at 15 watts
3 – processor device only ... total board power TBD
4 – 3000 MIPS at 7.5 watts (measured)
5 – 5000 MIPS at 10 watts (calculated)

Chart provided by Tom Flatley- NASA/GSFC