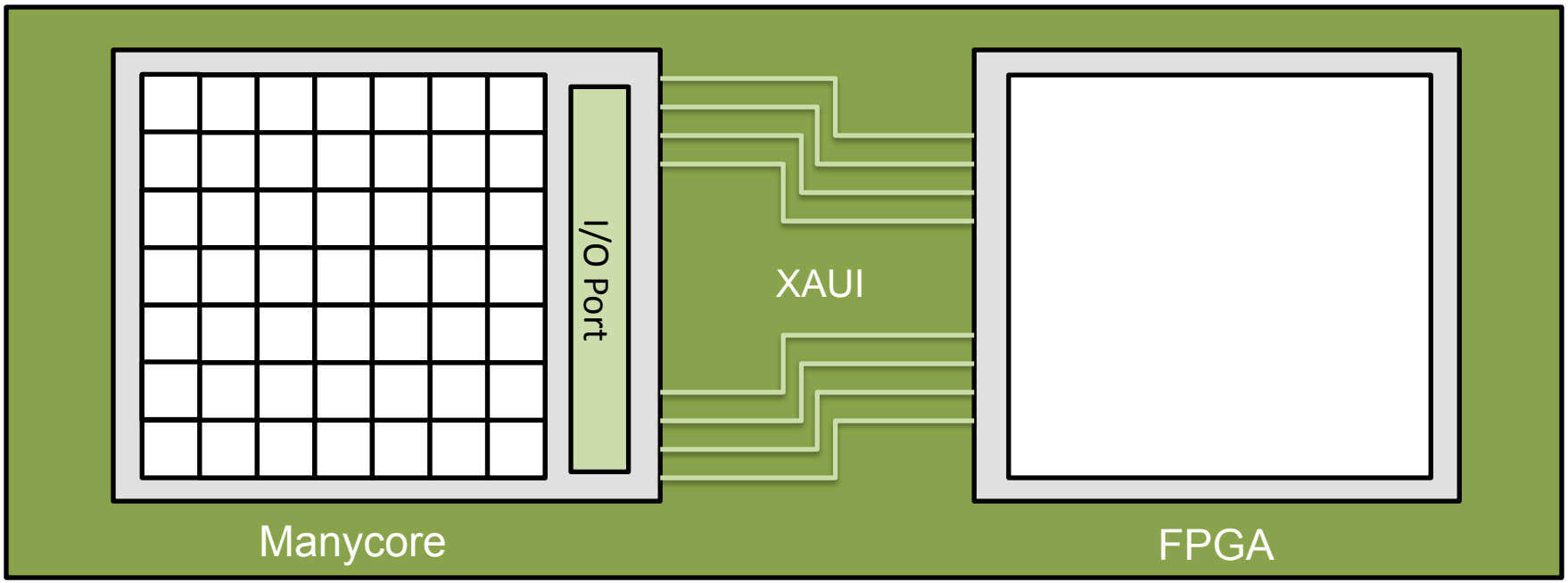
A manycore space computer with FPGA co-processing

Brandon Beresini
beresini@maxentric.com

Scott Ricketts
sricketts@maxentric.com

Michael B. Taylor
michael.b.taylor@angstromush.com

Rad-hard Unified Scalable Heterogeneous Architecture (RUSH)



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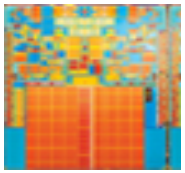
Today's talk

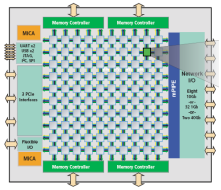
- Motivation
- RUSH Architecture
- Preliminary Results

Promising candidates for next-generation space computing



CPU

e.g. RAD750

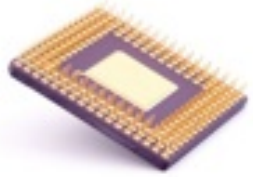


Manycore

e.g. Maestro

FPGA

e.g. Virtex 5QV



ASIC

e.g. OPERA RHBD

Higher Performance,
Better Power efficiency

Greater Programmability,
Lower NRE Costs

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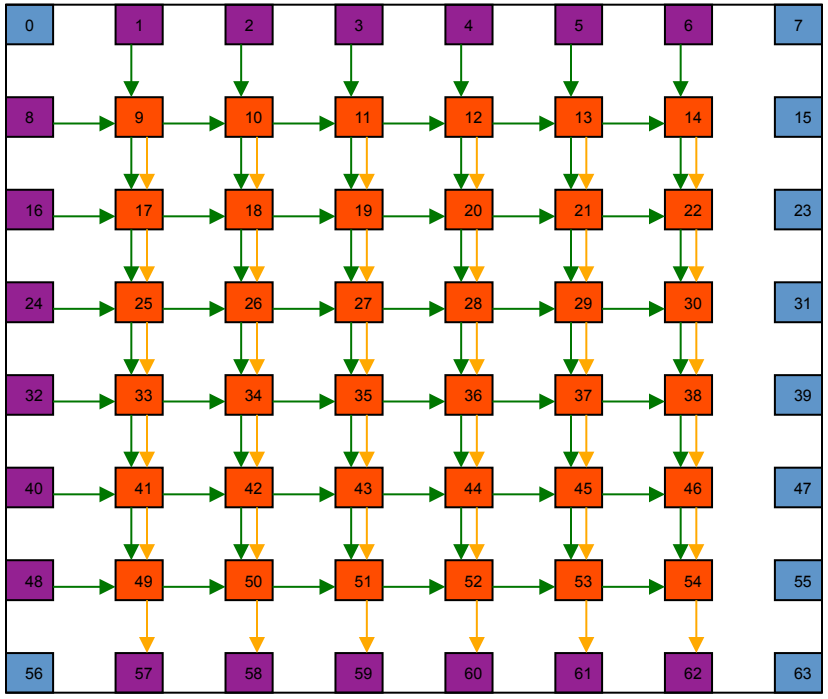
Manycore (or tiled) architectures offer programmability and scalability

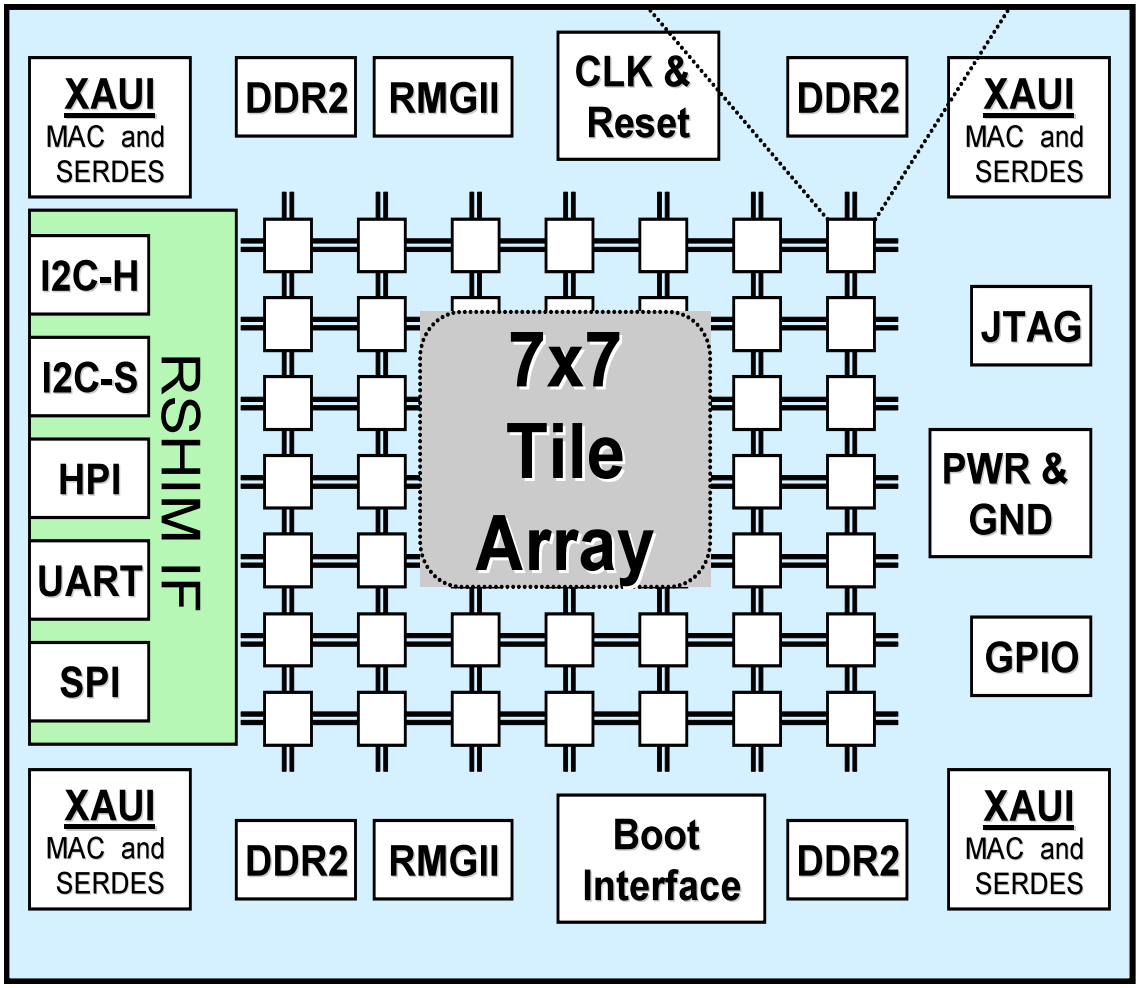
- Array of general purpose tiles
- Low latency between tiles
- Coherent shared memory
- Message passing for efficient sync



Mesh networks manage intra-chip communication

Dynamic Networks give access to all of the fundamental resources of the architecture

- Tiles
- L1, L2 Caches
- DRAM
- I/O Devices



[Malone, MAPLD 2009]

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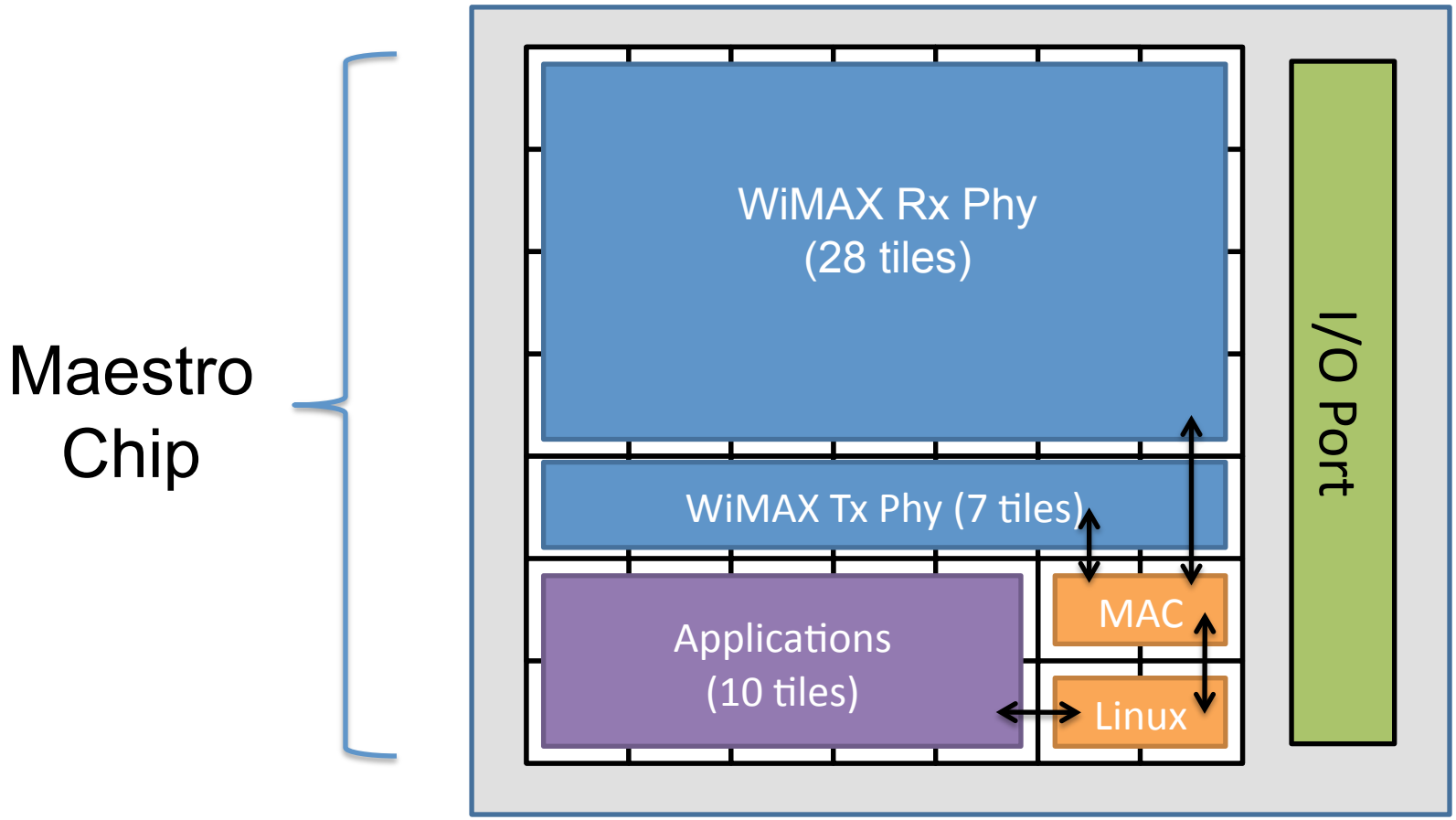
Running Example: Maxentric's Manycore Software Defined Radio



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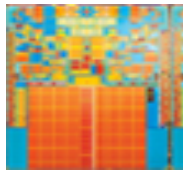
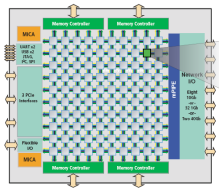
An optimal processing platform might have a mix of these:



CPU

e.g. RAD750

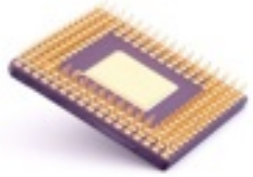


Manycore

e.g. Maestro

FPGA

e.g. Virtex 5QV



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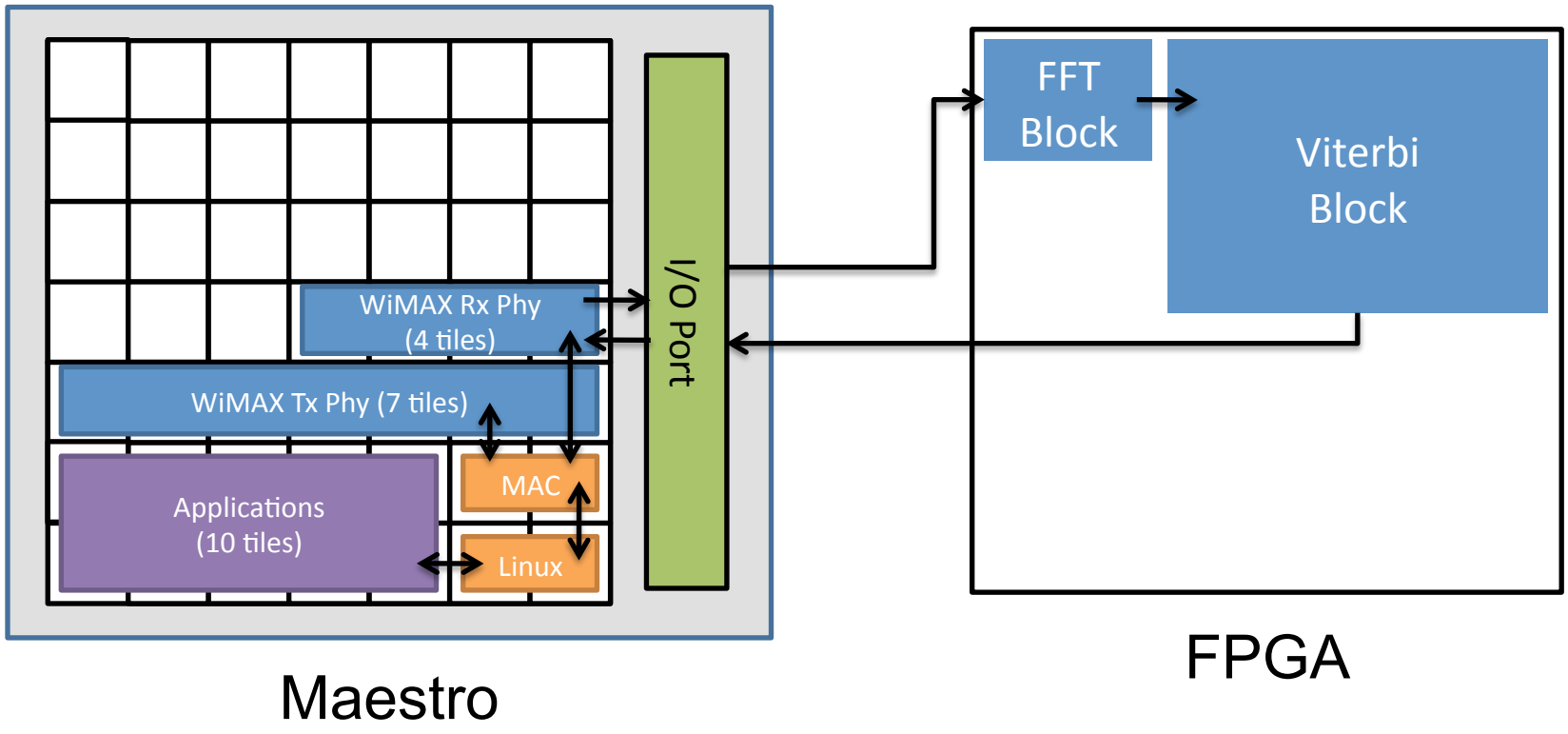
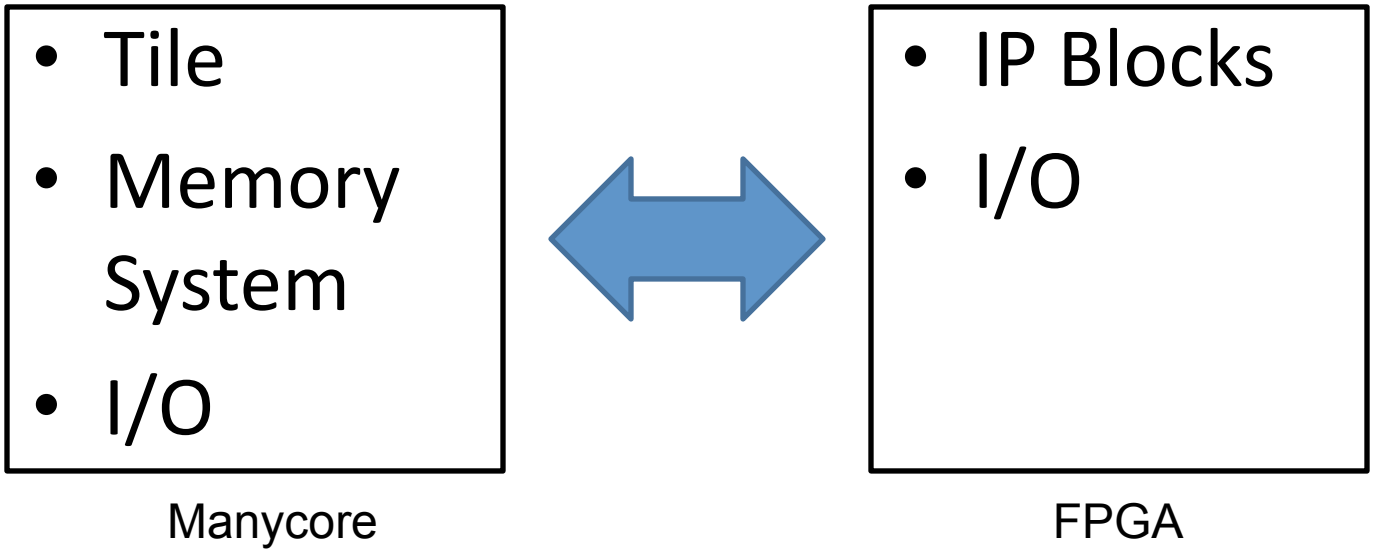
We might want to offload the Viterbi decoder to an FPGA



Integration of heterogeneous processing systems is challenging

Hardware integration	Providing access across chip boundaries to architectural resources	e.g. physical layer protocols, access to memory systems on CPUs, logic cores on FPGAs, etc
Software integration	Developing software that uses the correct semantics and interfaces for cross-chip communication	e.g. message formats, synchronization, data streaming model, etc

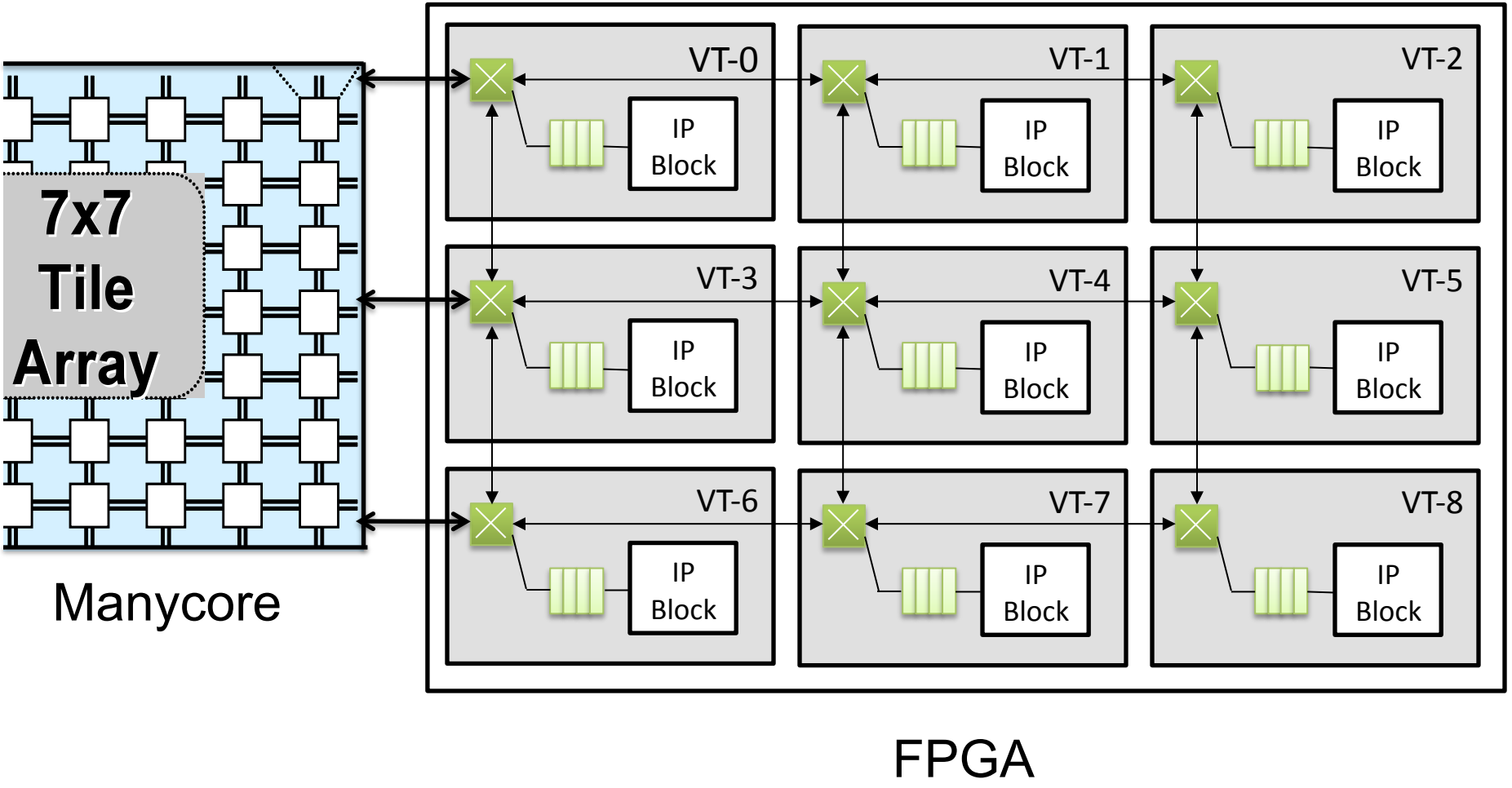
Integration requires exposing the underlying architectural resources of the two chips in the system



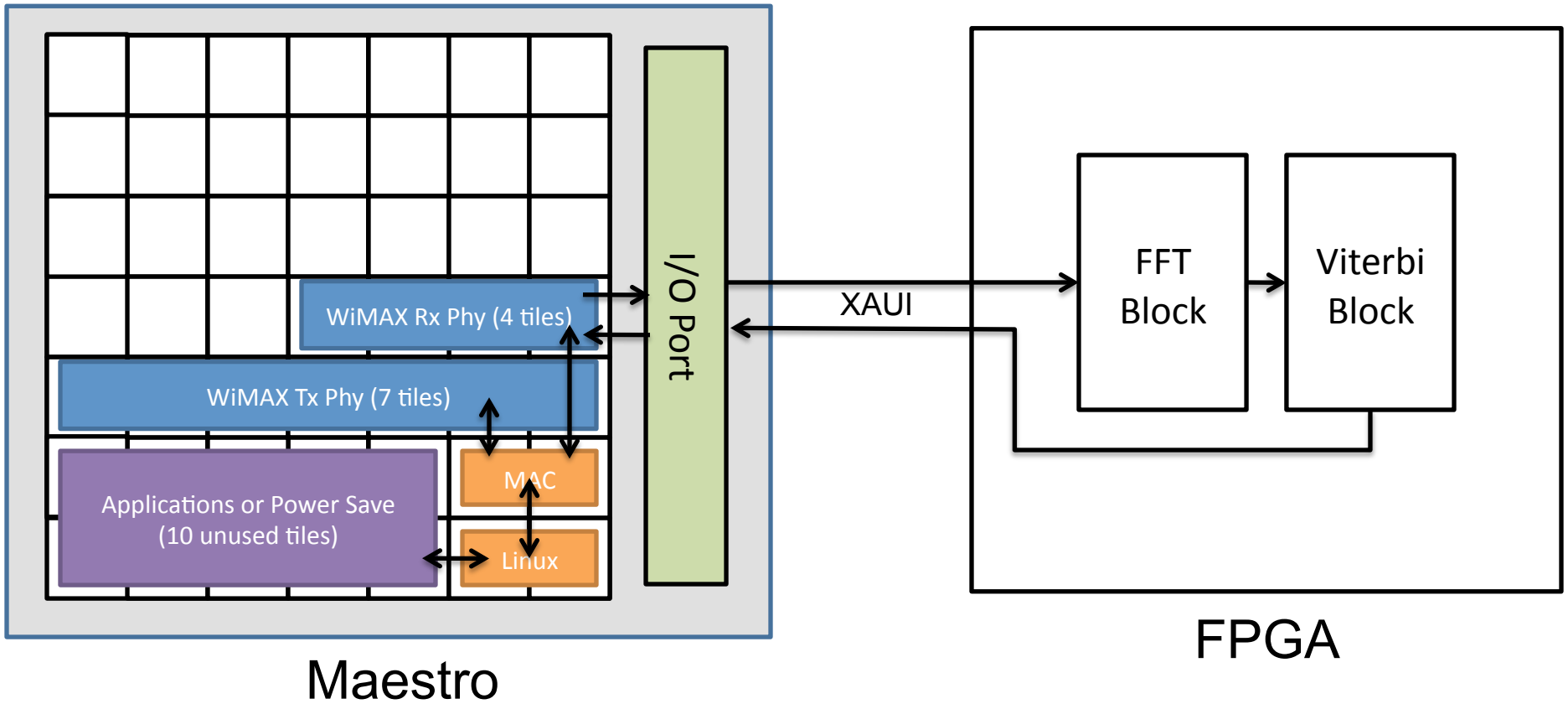
Tiled architectures like Maestro have mechanisms to handle these challenges

Hardware integration	Expose memory systems, tiles and I/O to I/O devices through packet-based mesh network
Software integration	Provide message passing, DMA, and shared memory as simple and powerful models for data movement and synchronization

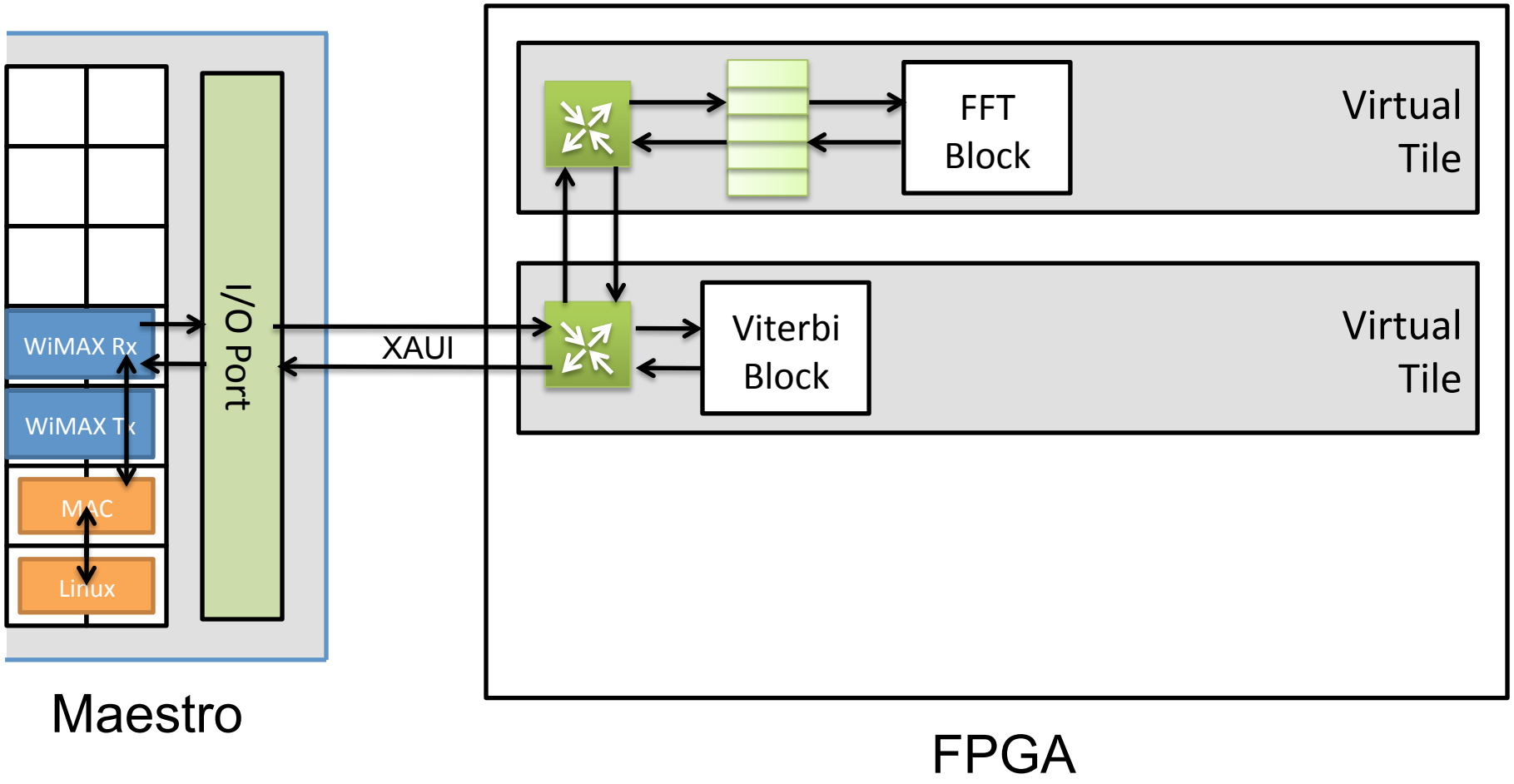
RUSH applies the tiled model across the heterogeneous system



Integrating Maestro and an FPGA (SDR Example continued)



RUSH places the FFT and Viterbi blocks into virtual tiles



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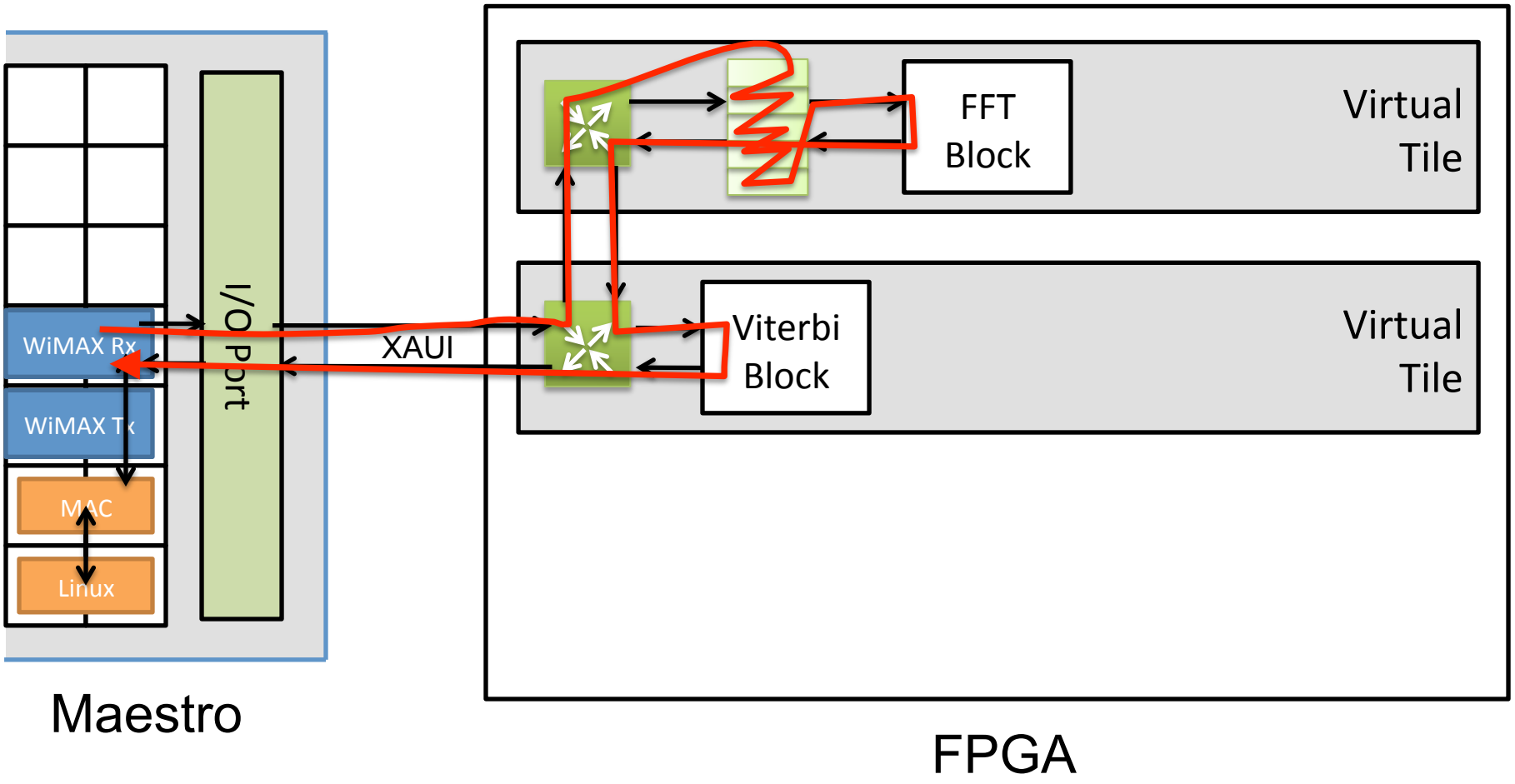
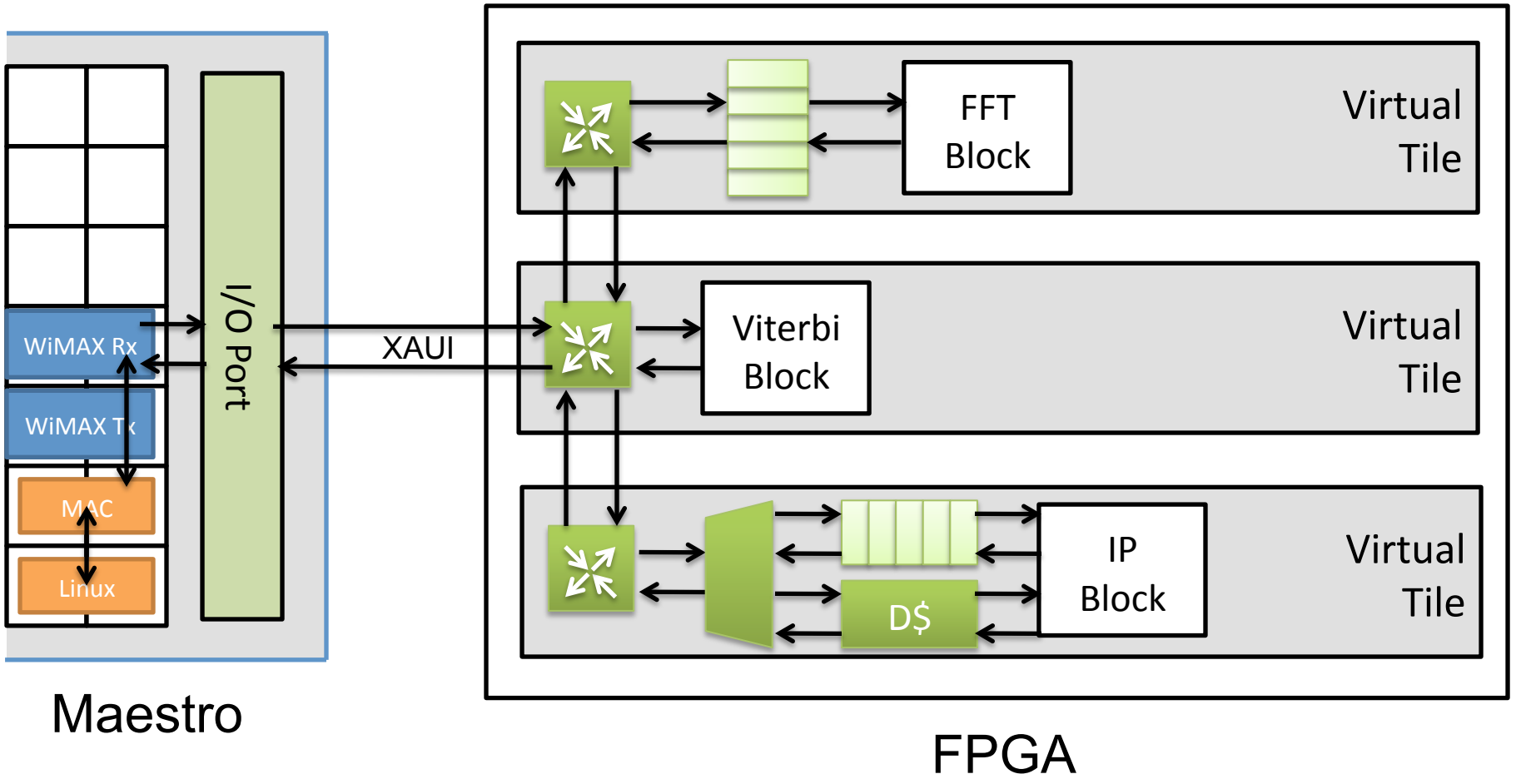
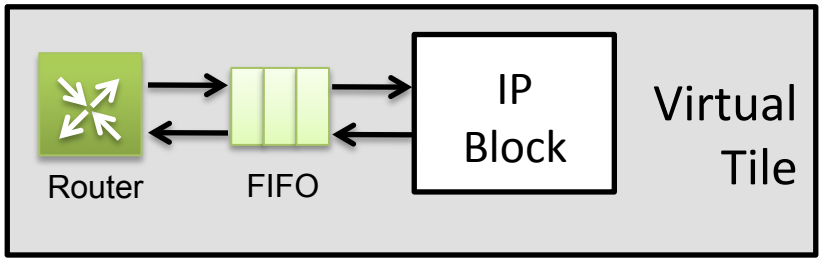


A tile can add a data cache that is coherent with the cross-chip shared memory system

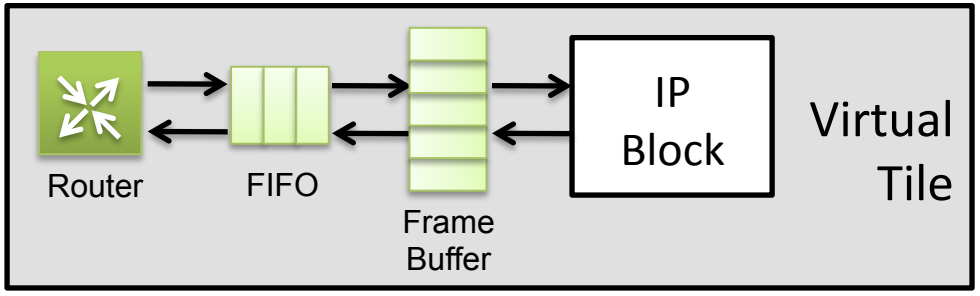


FPGA-side prebuilt blocks provide integration with RUSH communication idioms

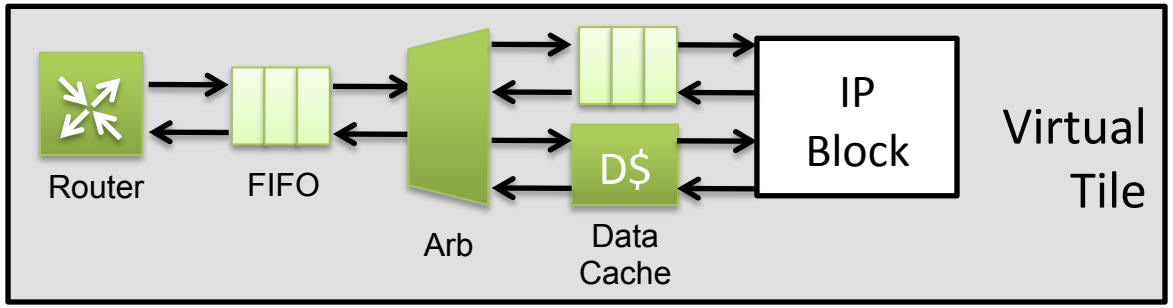
Sample-driven



Frame-driven



Random
Access



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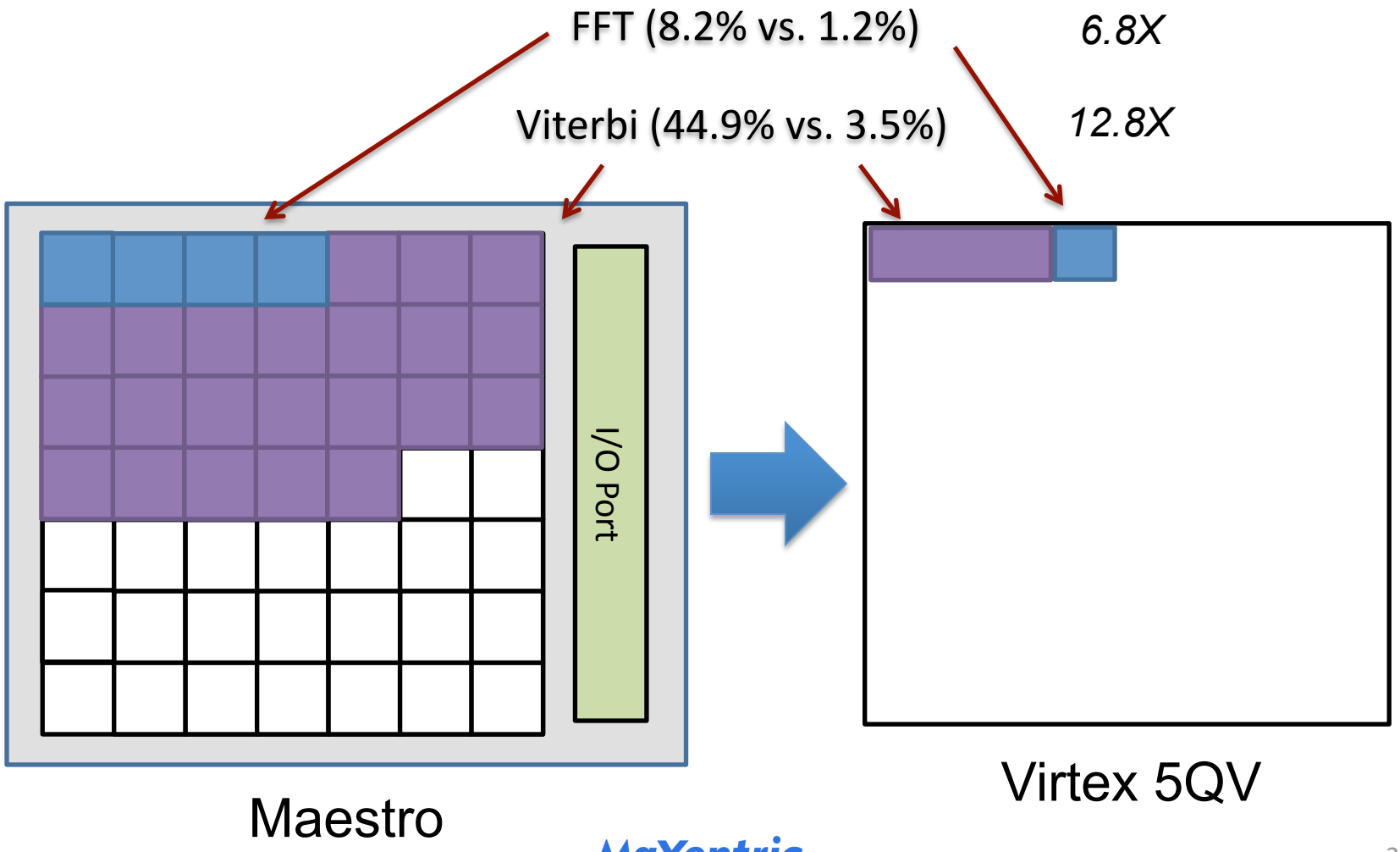
Evaluation Methodology

- Application: Software Defined WiMAX Transceiver
  - Frame size: 2048
  - 40Mbits/s QPSK at 11k frames/s
  - K=7, ½-rate encoder
- Analyzed complexity for demanding kernels
  - FFT
  - Viterbi
- Estimated resource allocation for kernels

Estimates of potential efficiency gains



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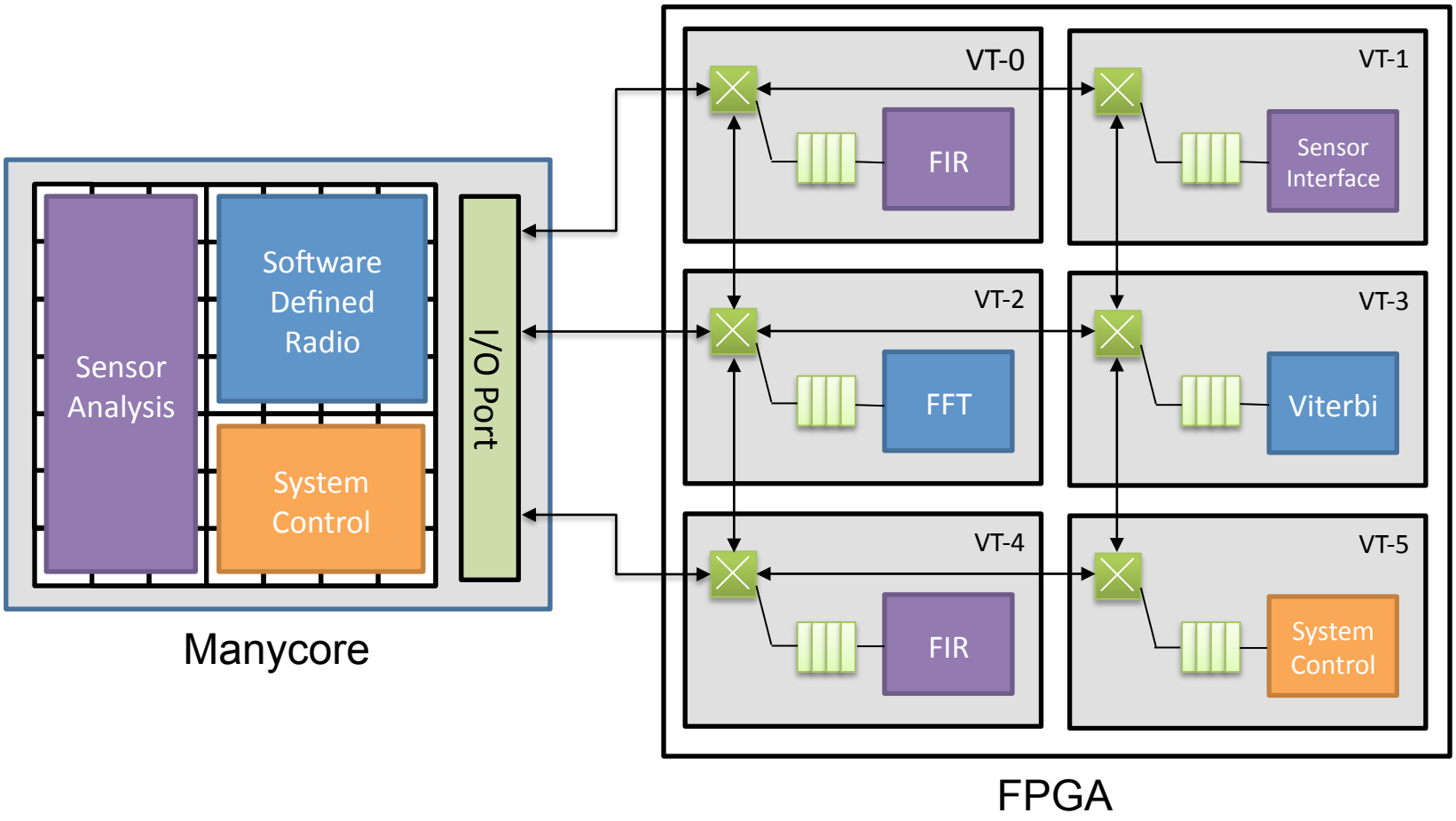
Future Work: Extending beyond kernels to systems of systems



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Conclusion

- Virtual tiles and the cross-chip mesh network apply the tiled model across the heterogeneous system
- Applying the tiled model creates a unified heterogeneous architecture
- The unified architecture enables developers create high performance and power efficient systems

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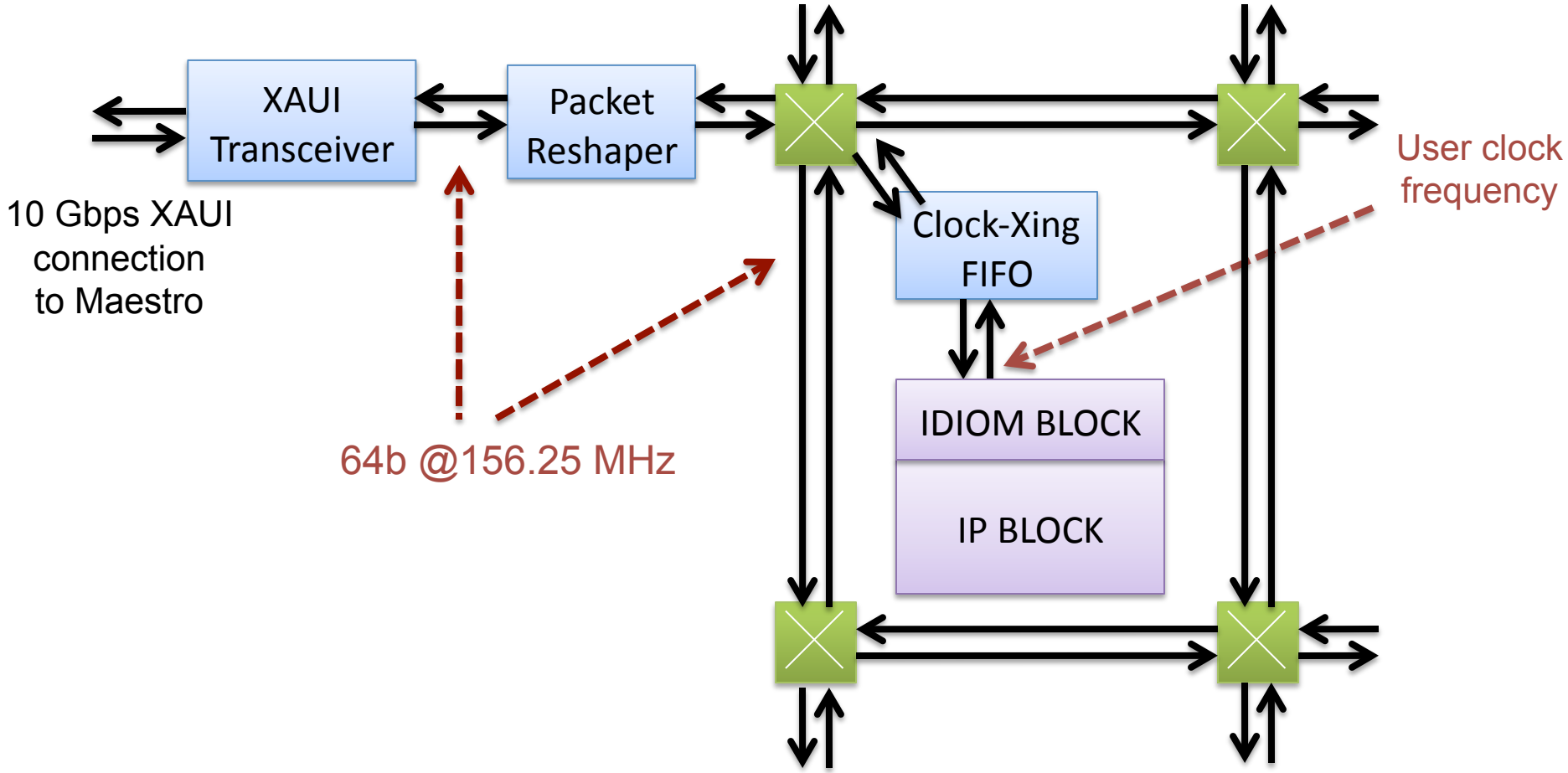
Cross-Chip Communication: FPGA Side



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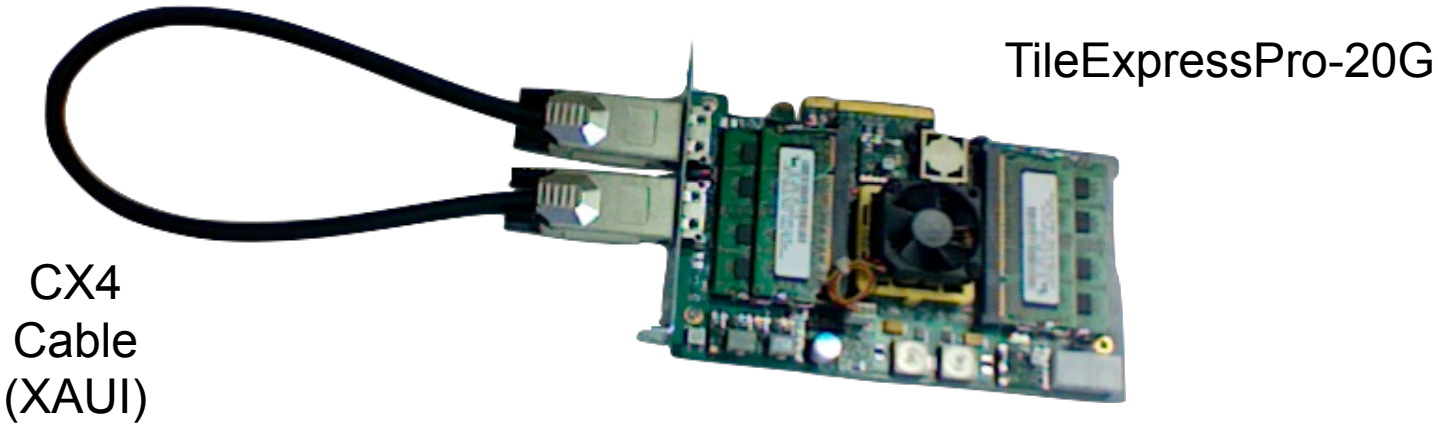
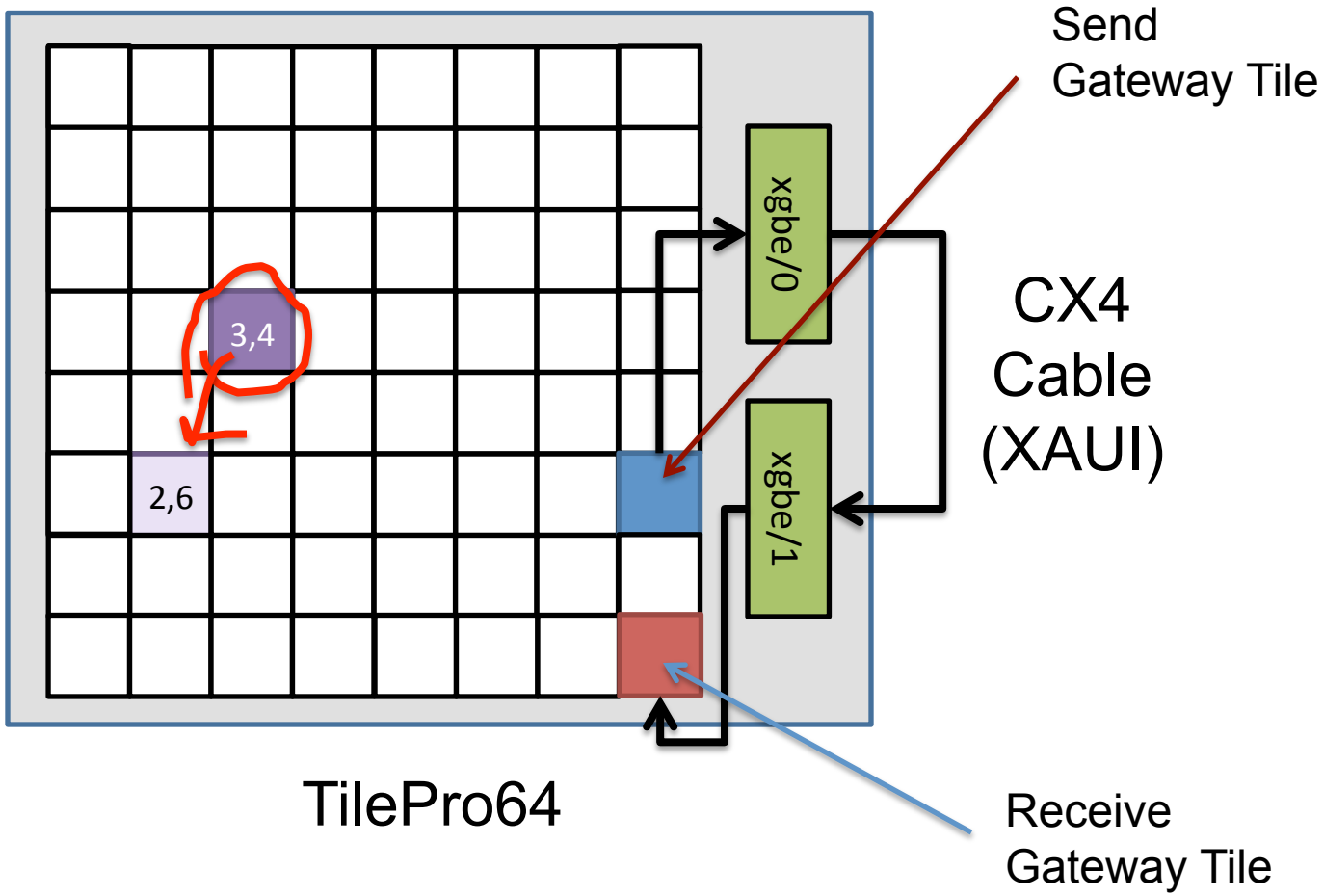
Cross-Chip Communication: Tilera Side

- Since FPGA is configurable, Tilera side is relatively more important for Phase I
- We prototyped connection with XAUI CX4 Loop-Back cable on TileExpressPro-20G
- Subsequent slides explain Tilera side comm.



Tilera Side Communication



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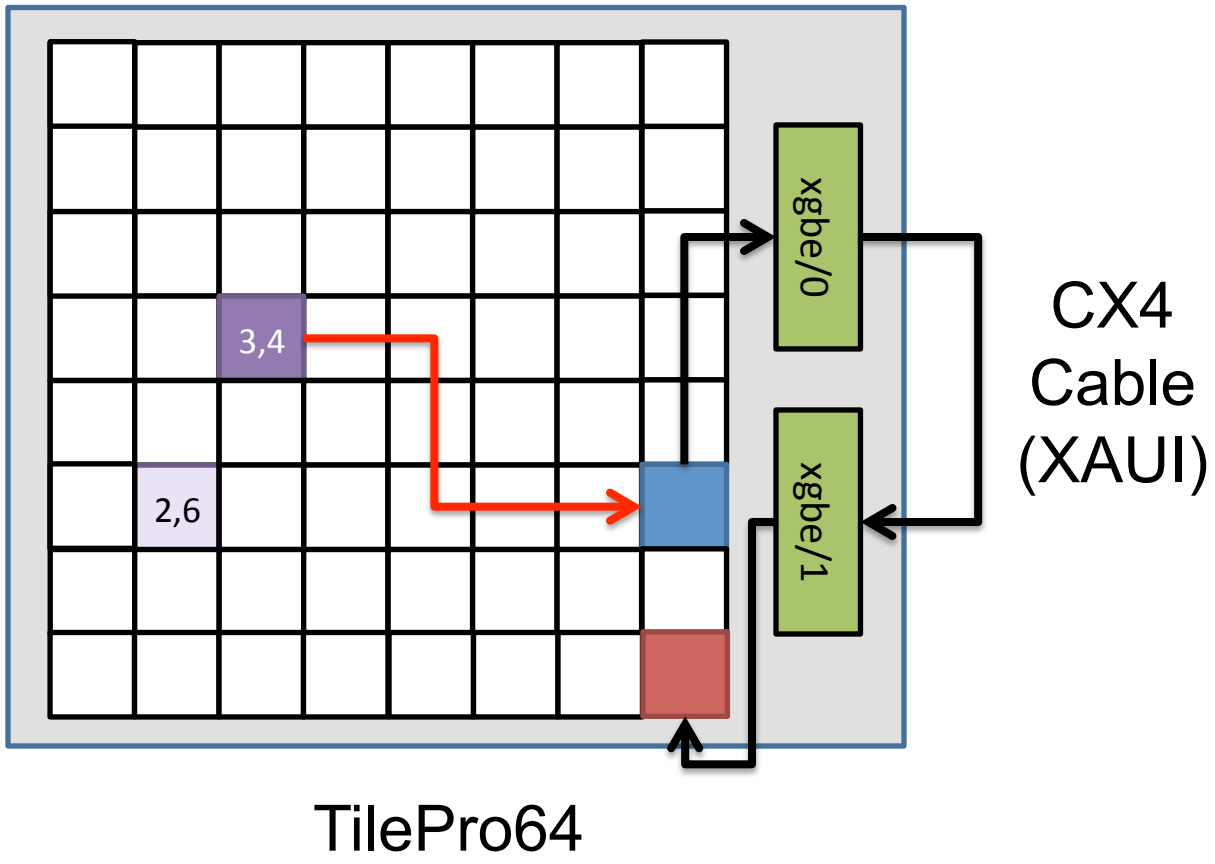
Tilera Side Communication



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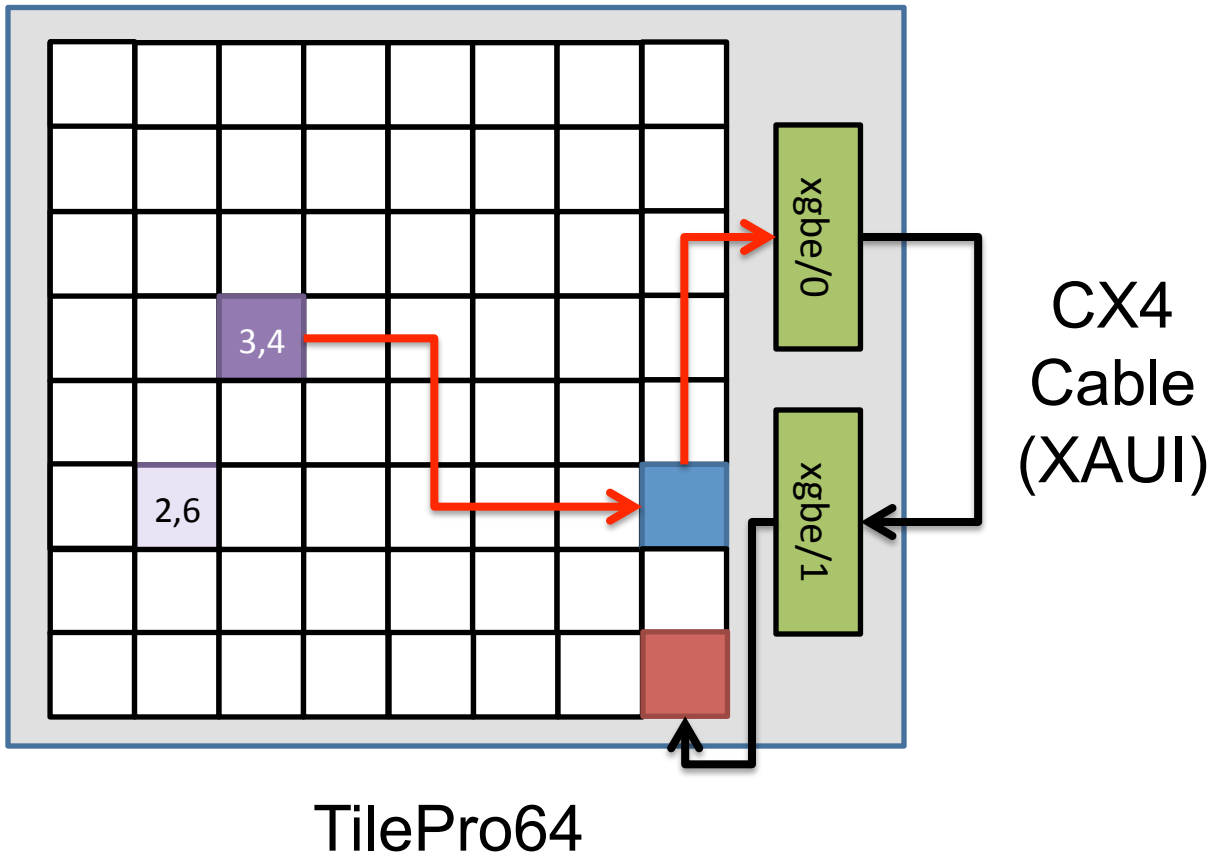
Tilera Side Communication



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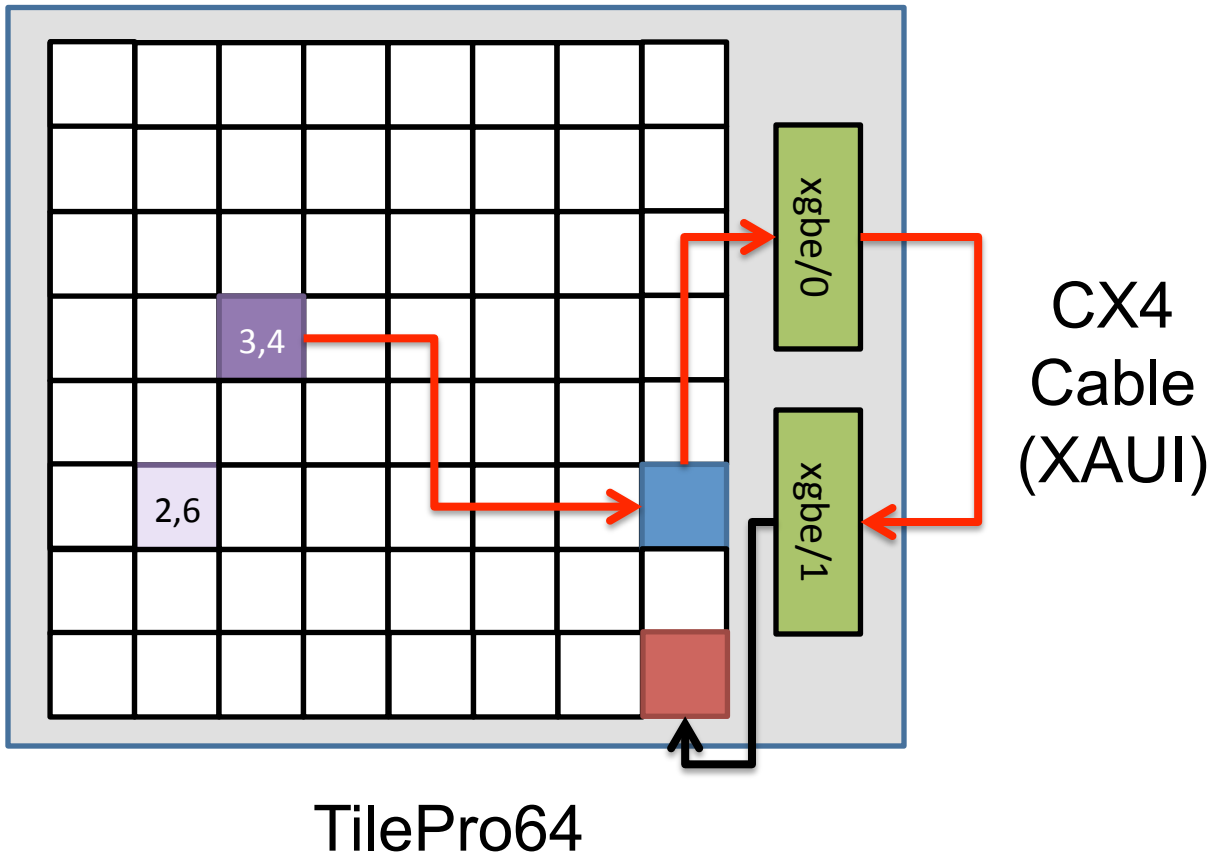
Tilera Side Communication



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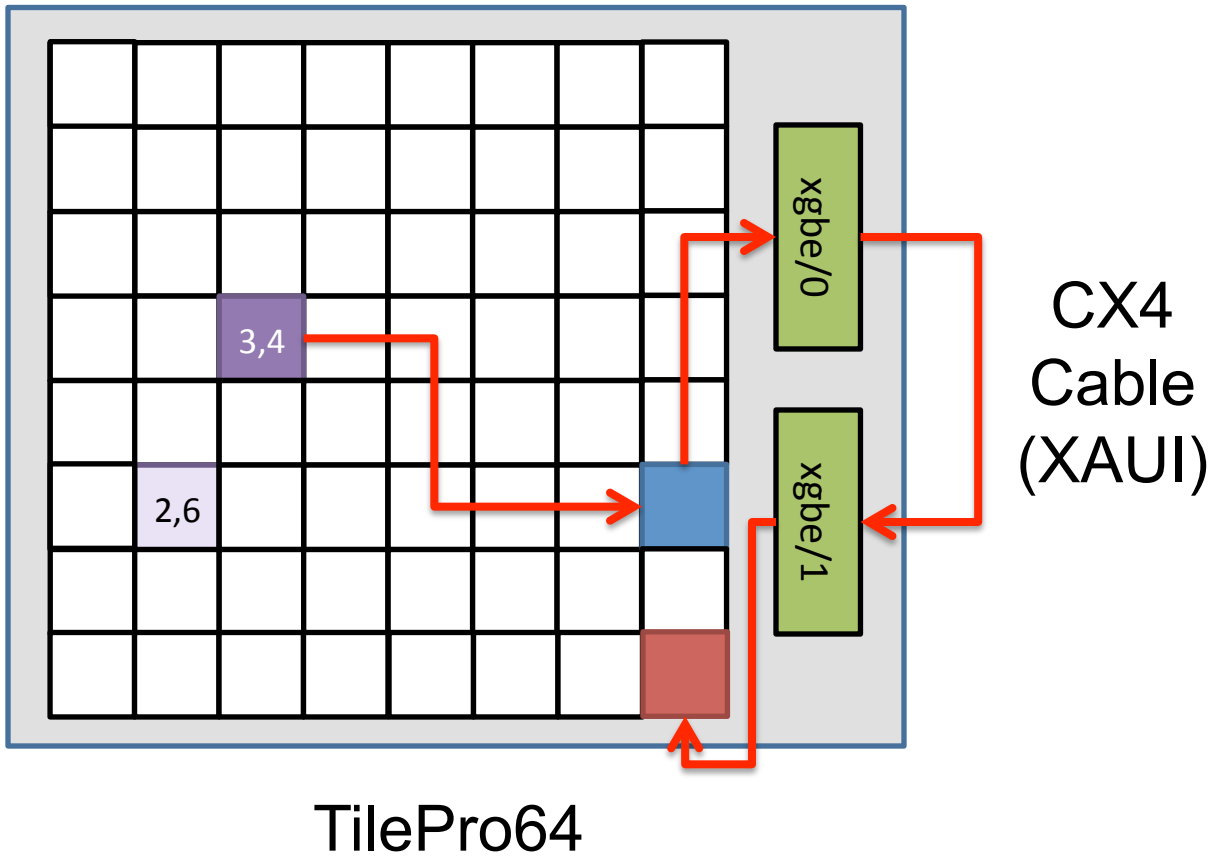
Tilera Side Communication



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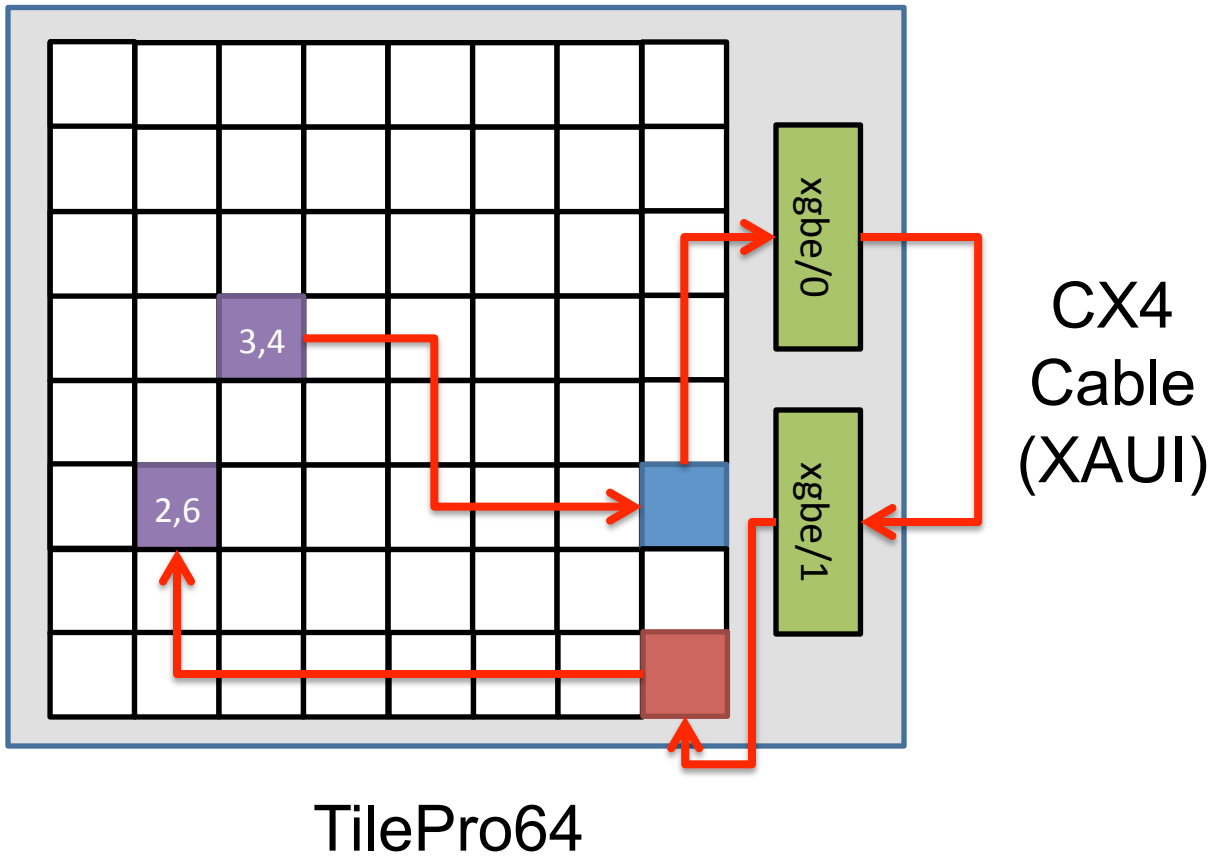
Tilera Side Communication



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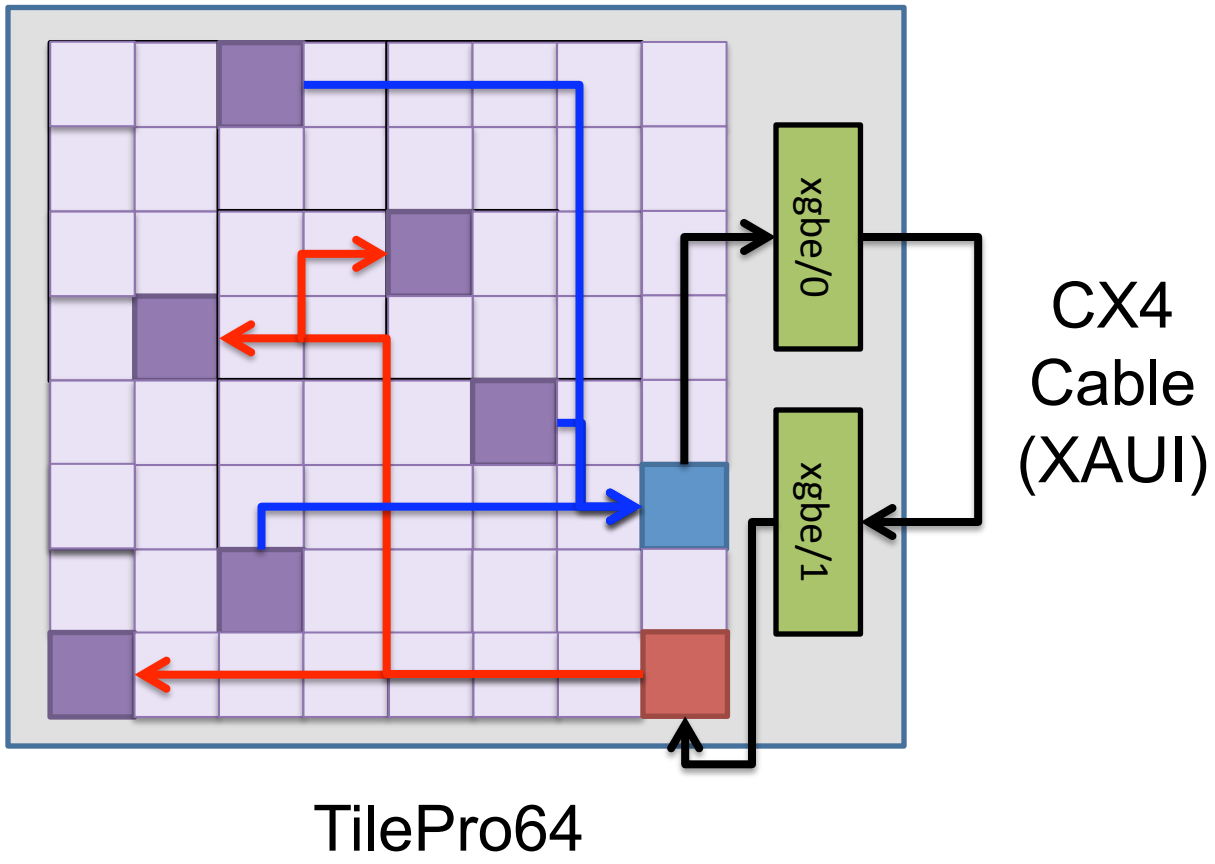
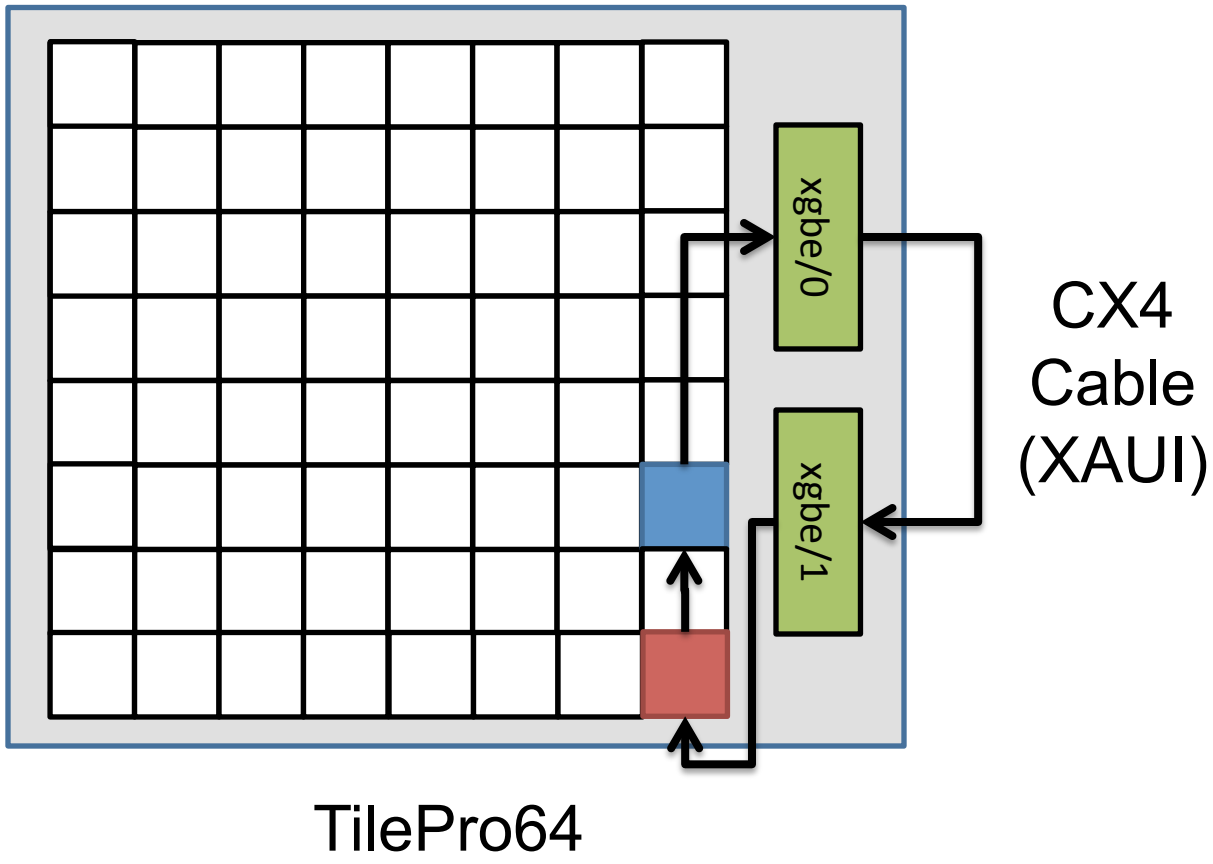
Tilera Side Communication



Round Trip XAUI latency XAUI Loopback cable



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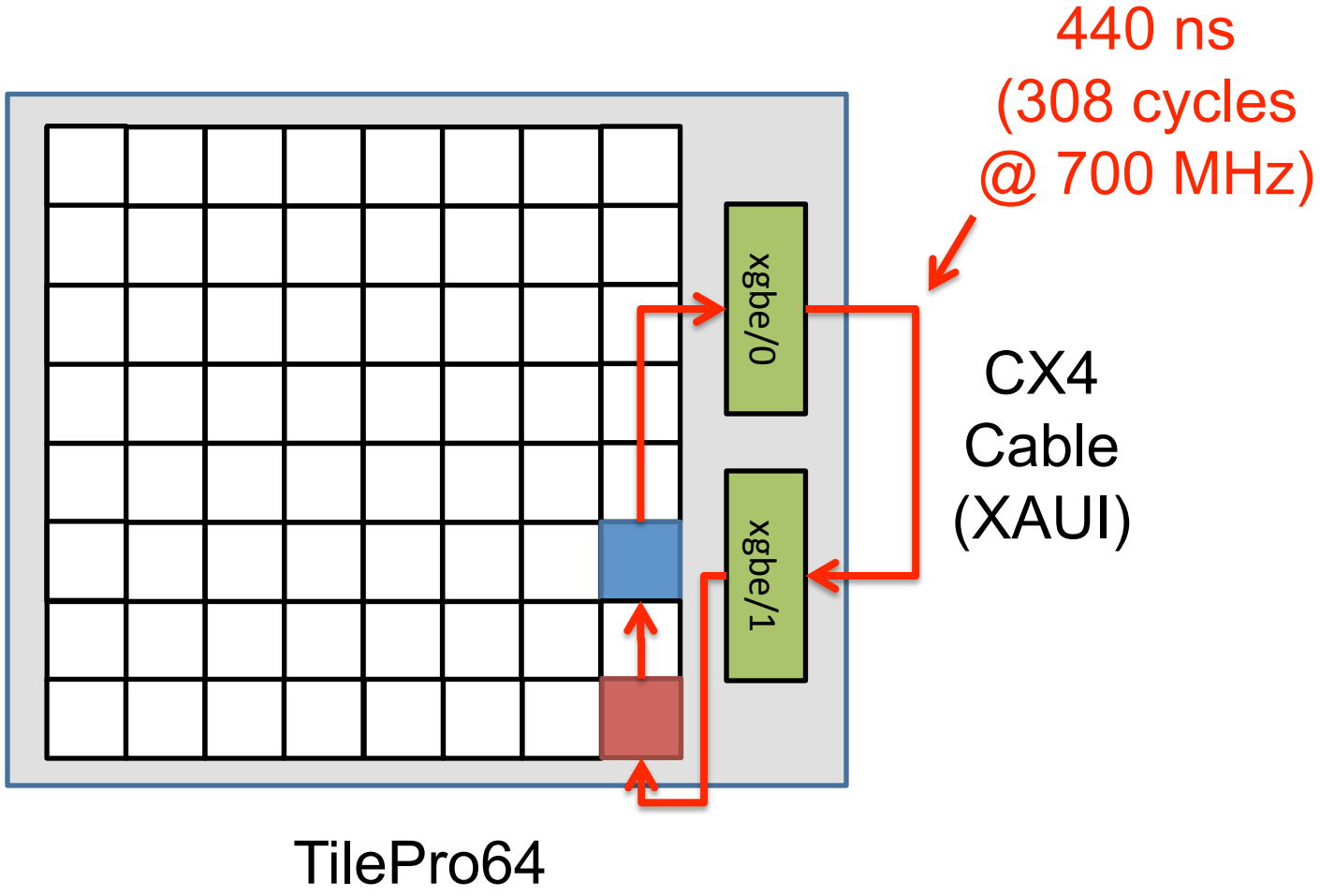
Round Trip Latency: 440 ns



Good Reason to Expect Latency will be Similar for FPGA<->Tilera

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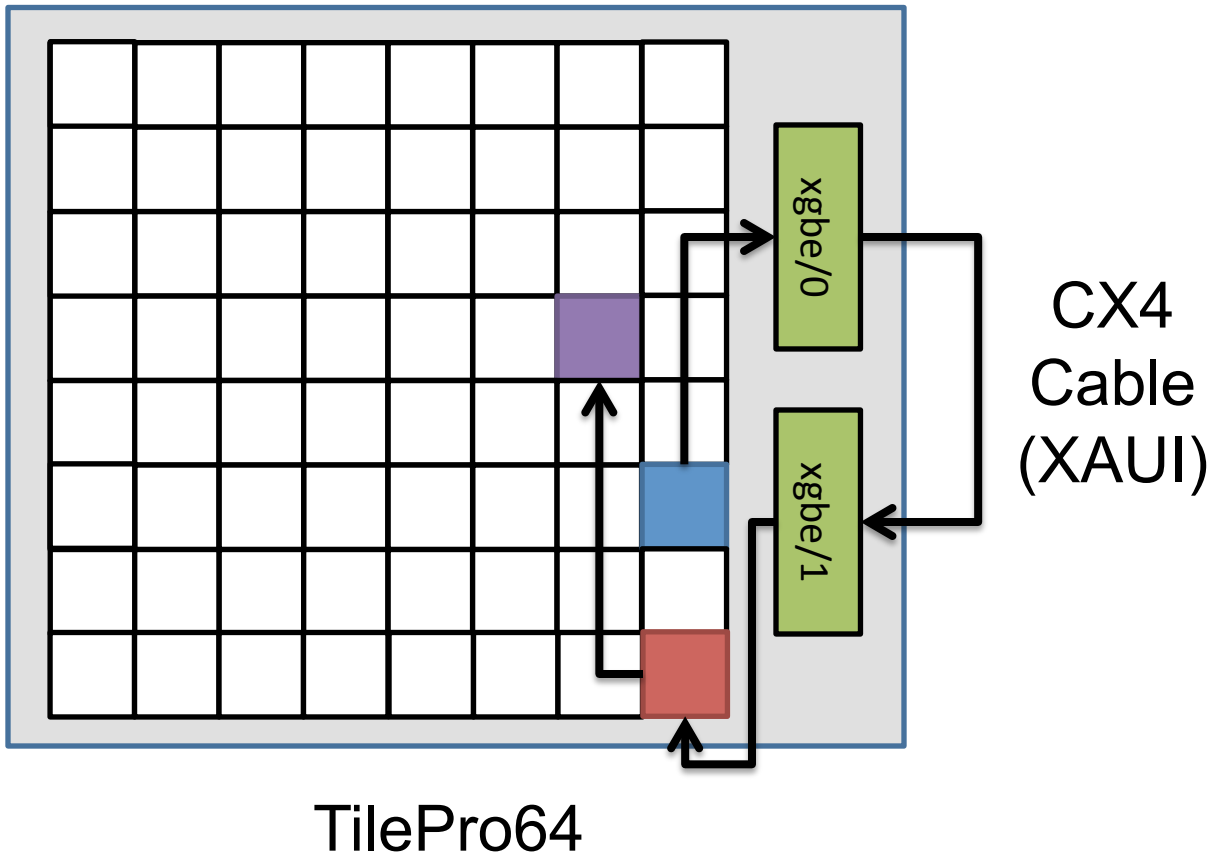
Throughput Test Setup



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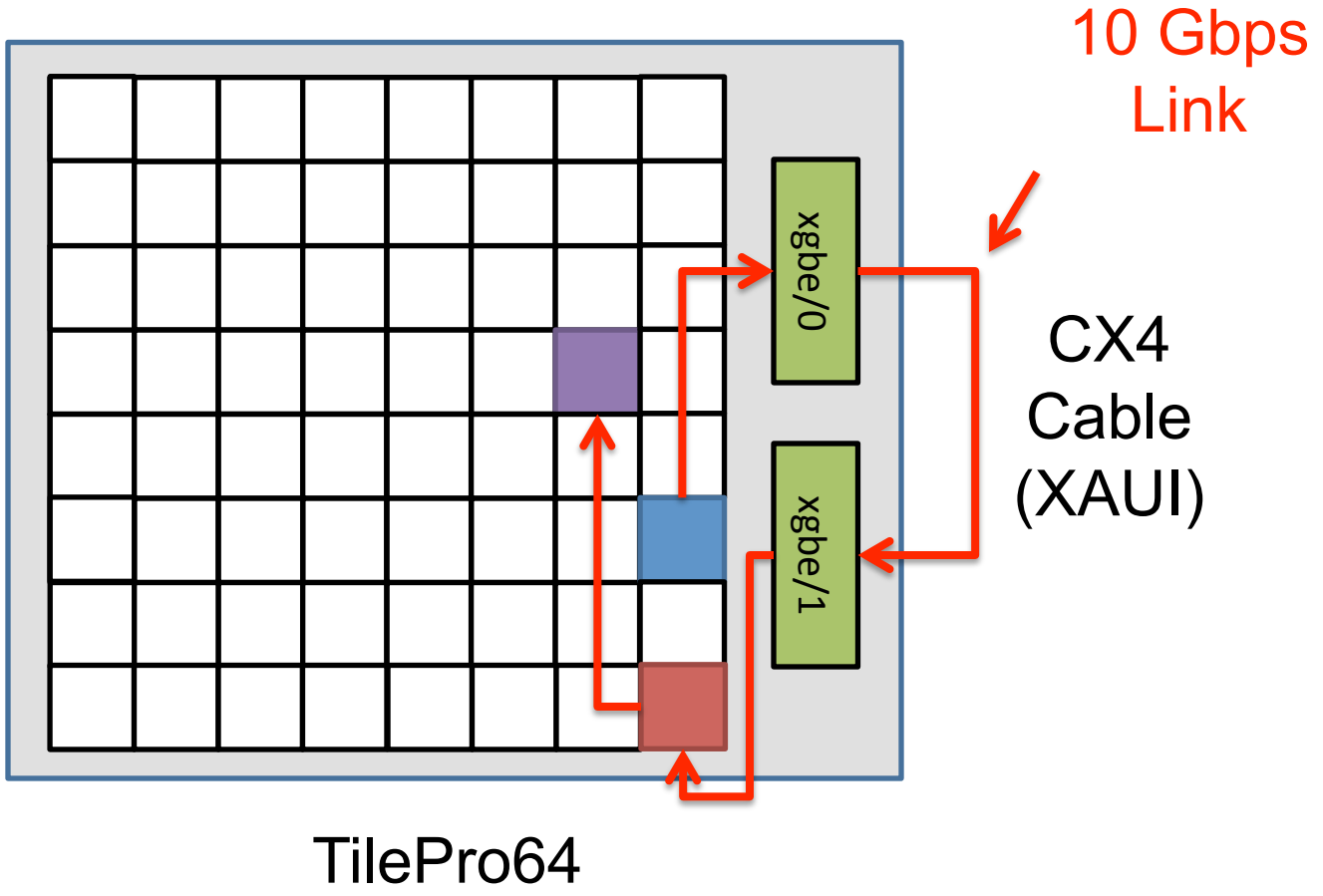
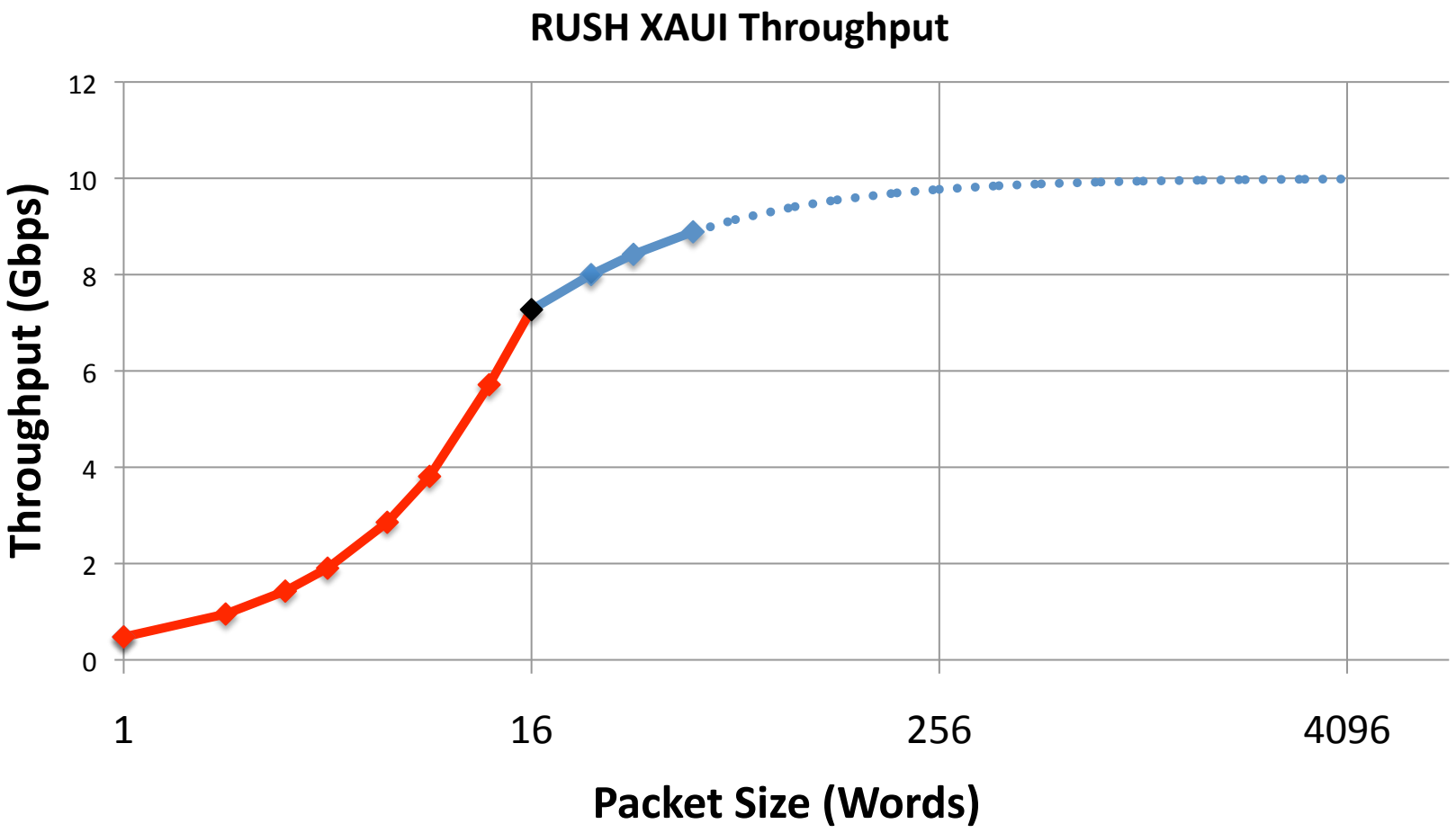
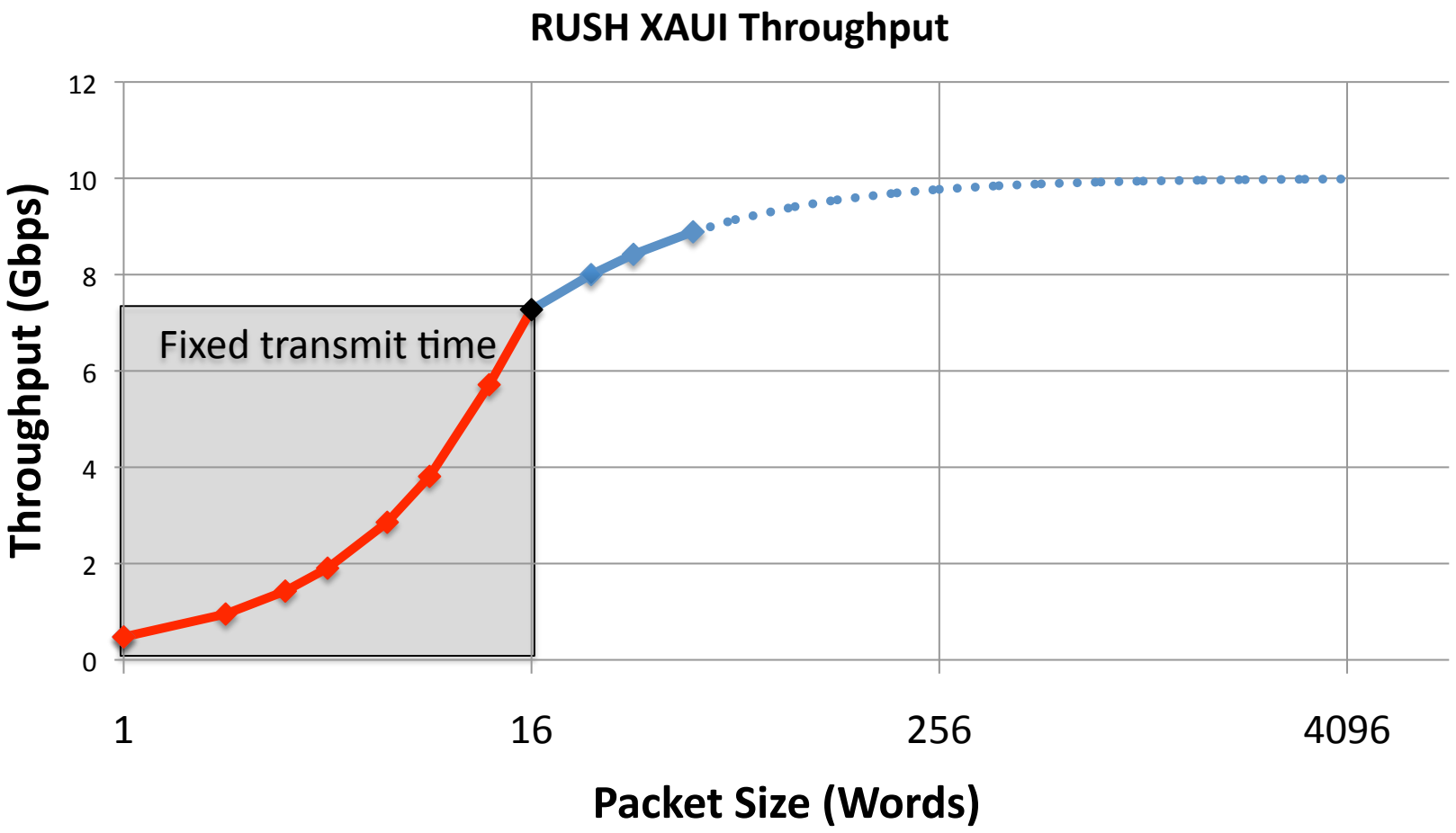


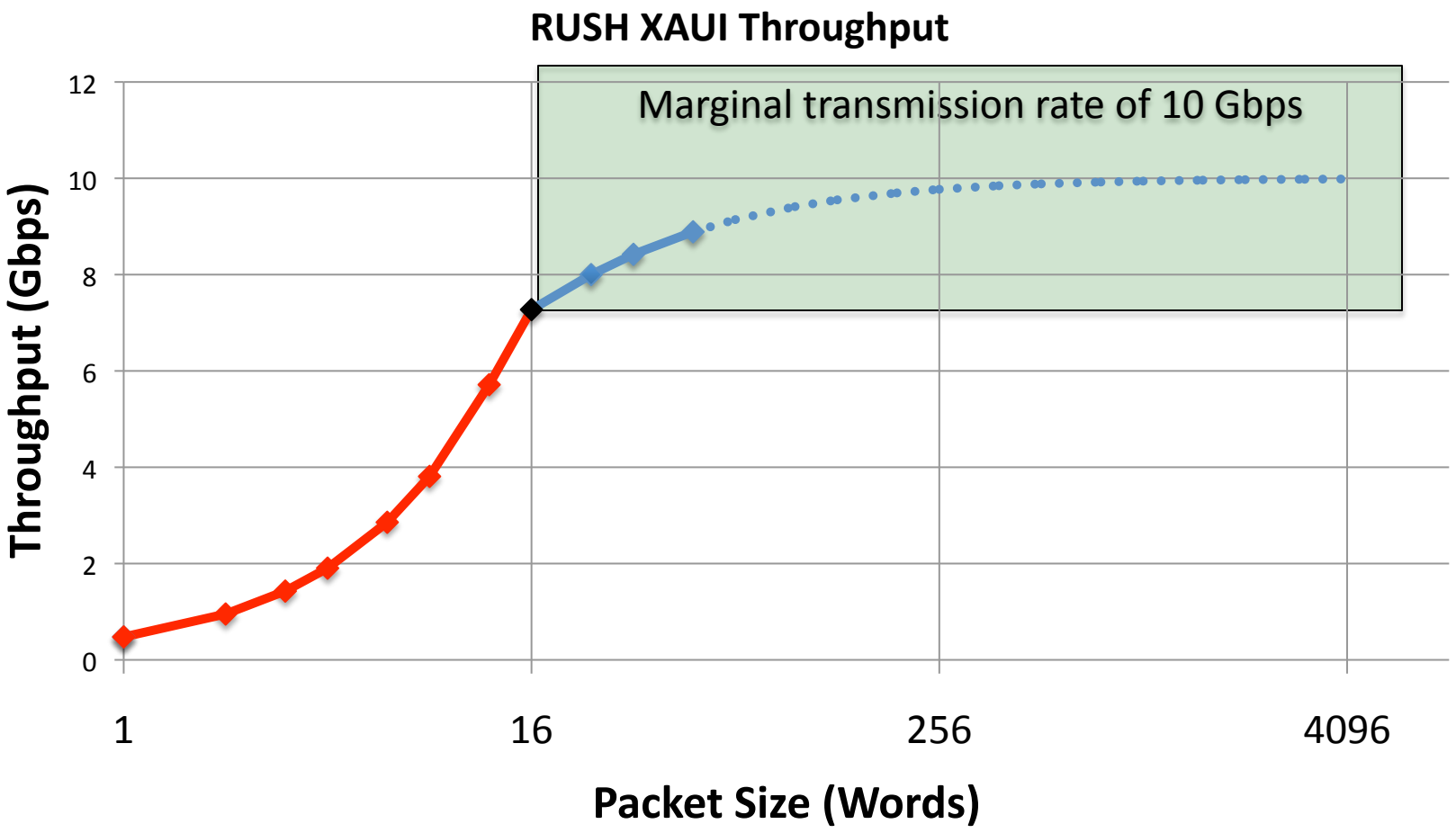
XAUI communication at 10 Gbps



Small Packets



Large Packets



XAUI communication

- Latency: 440ns (308 cycles at 700MHz)
- Throughput: Approaching 10 Gbps
  - **minimum underlying XAUI packet size**
    - **21 words; 15 words are data payload**
    - ***1 to 15 words of data are the same cost***
- Stability: 24+ hr run
  - rt latency packet latency varies by <=1 cycle
- Reliability: 24+ hr rur
  - 0 data errors