SPACE MICRO

Image Processing System for ISR Applications: IPC5000

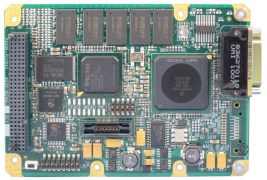
Jose Romero, Space Micro
Dave Bozek, Space Micro
David Czajkowski, Space Micro
Darrell Sellers, Space MIcro
Dave Strobel, Space Micro

New Facility and Capabilities

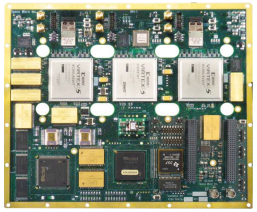
- 20,000 sq. ft
- Improved Clean Room
  - Class 10,000
- Additional Environmental Equipment
  - Thermal vacuum
  - Random vibration
  - Sine vibration
  - Shock
  - Thermal cycling
- SECRET facility
  - COMSEC handling

Radiation Hardened Products

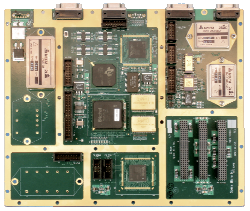
Digital Boards



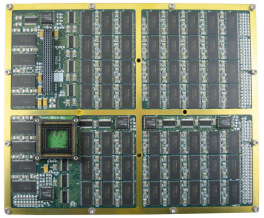
Proton400k-L™ Dual-Core Computer



Proton300k™ Reconfigurable SBC

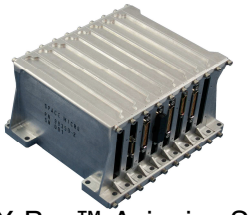


Proton200k™ Custom DSP SBC



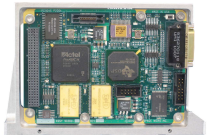
Solid State Buffer

Systems/Instruments



ProtonX-Box™ Avionics Suite

------Examples of Configured Slices --------

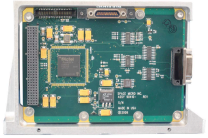


Proton200k™

FPGA/SpaceWire

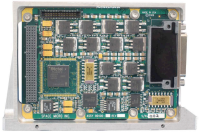
Digital I/O

Analog I/O

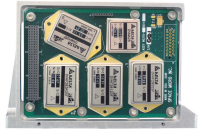


GPS (Receiver not shown)

Valve/Relay Driver

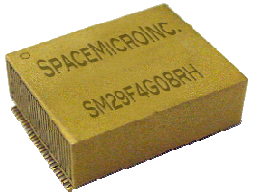


Power Switch

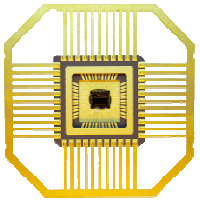


Power Supply

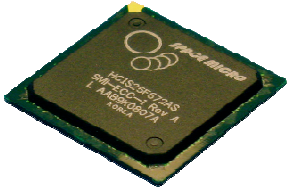
Components



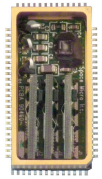
8 Gb RH NAND Flash



H-Core™ Pat. "Watchdog" IC



2.5 Gbps ECC IC

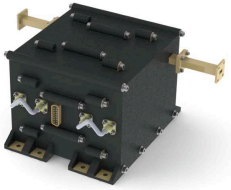


Divert Attitude Controller (DACS)

RF Microwave

uSTDN ™ Transponder

uSGLS™ Transponder



Ka-Band Transmitter

uXLPA™ Linearized SSPA

Abstract and Motivation

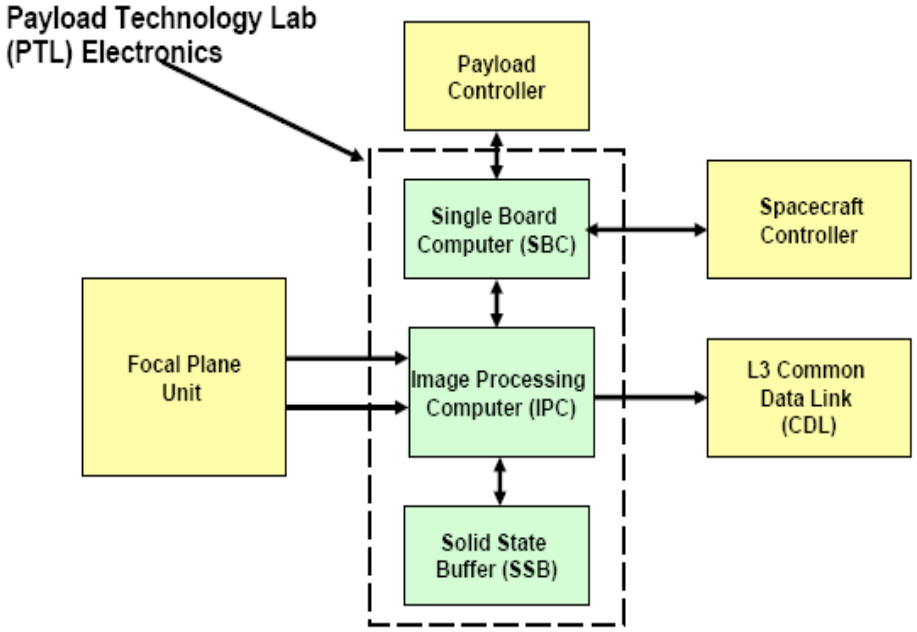
Space Micro has developed a low power, radiation hardened space image processing computer system, called the IPC 5000, which highly leverages commercial microprocessor and microelectronics technology. It is adaptable for various new ISR space emissions. The IPC 5000 combines several low power techniques currently used for PDAs and laptop computers, such as a dynamic voltage scaling, frequency scaling and software controlled hardware.

In this application, Space Micro's Proton 200K DSP card and Proton 300K reconfigurable platform are the core of the IPC5000 system and will process various detector and camera images for down linking.

Embedded in this system are Space Micro patented SEU mitigation techniques which enable its computers to exceed SEU performance of traditional rad hard computers. The performance of the 32-bit Proton 200K single board computer (SBC) is 1200MIPS at 350 MHz, with a 5W power budget for the microprocessor. SEL immunity is greater than 70 MeV/ mg/ cm2 and SUE bit error rates of less the 1E-4 unrecoverable upsets per day.

Assembly IPC5000 Integrated Assembly

- **Three Slice Assembly (IPC5000) comprised of:**
  - **Single Board Computer (SBC) (Proton 200K)**
  - **Image Processing Card (IPC)**
  - **Solid State Buffer (SSB)**



3-Slice Configuration

Solid State Buffer

Reconfigurable Processor

Single Board Computer

IPC5000 Image Processing Functions

- The IPC5000 basic functions are:
  - Conversion and ordering of up to 6 (optional formats available) imager channels. Selection of any single channel or all 6 channels
  - JPEG or JPEG2000 compression and packetization, per JPEG standard. Compression ratios from 1:1 up to 16:1
  - Additional compression through image registration and comparison of images, with total compression greatly increased
  - Image windowing
  - NUC calibration
  - Synthetic image generation for system test purposes (internal generation of a known image to SSB or CDL)
  - Option to send compressed image to SSB or CDL (directly)
  - CDL packetization and channel ordering into standard CDL format

Fusion Processor (Proton200k™) Overview

- FP consists of:
  - 320C6713 VLIW CPU
  - 128 MB local SDRAM
  - EDAC for SDRAM
  - 2 UARTs
  - 2 MB EEPROM memory
  - PCI interface to SSB
  - IPC 64 bit data interface
  - Rx 64 bit data interface
  - Spacecraft serial interface
  - 95 MHz clocks & dividers
  - Power circuits & control for IPC5000

- FP functions
  - Master IPC5000 controller
    - Imager control (on/off)
    - IPC manager
    - Image storage to SSB
    - CDL communication
  - Management of IPC
  - Management of SSB
  - Storage of telemetry
  - Reconfigurability of FP/IPC
  - Rx algorithm platform

Proton300k SEU Mitigated FPGA Platform

- Proton300k™
  - 6 to 24 M reconfigurable FPGA gates available for user programming
  - 32-bit DSP
  - 4,000 MIPS
  - SEU rate of < 1E-4 /day
  - >100 krad (Si) TID
  - No unrecoverable SEFIs
  - SEL Immunity >70 LET
  - Power: 5-7 watts + FPGA (5) power

Proton300k™

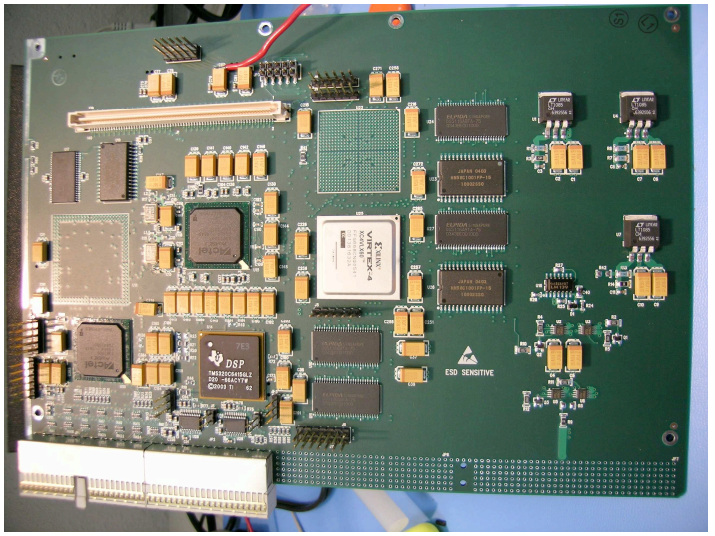


Image Processor Card Functions

- The IPC Board will contain 5 FPGAs to perform its image processing. The basic functions are:
  - Conversion and ordering of up to 14 imager channels. Selection of any single channel or all 14 channels can be made
  - JPEG compression and packetization, per JPEG standard. Compression ratios from 1:1 up to 16:1
  - NUC calibration
  - Synthetic image generation for system test purposes (internal generation of a known image to SSB or CDL)
  - Option to send compressed image to SSB or CDL (directly)
  - CDL packetization and channel ordering into standard CDL format

Image Processor Card Functions

- SSB High Speed Interface Bus is 44 MHz/64 Bits wide
- Efficiency 76% - 20 out of 84 cycles are used for house keeping.
- Sustained data rate ~ 2.14 Gbps.
- Even if all 14 channels are stored lossless the data rate will be 1.8275 Gbps

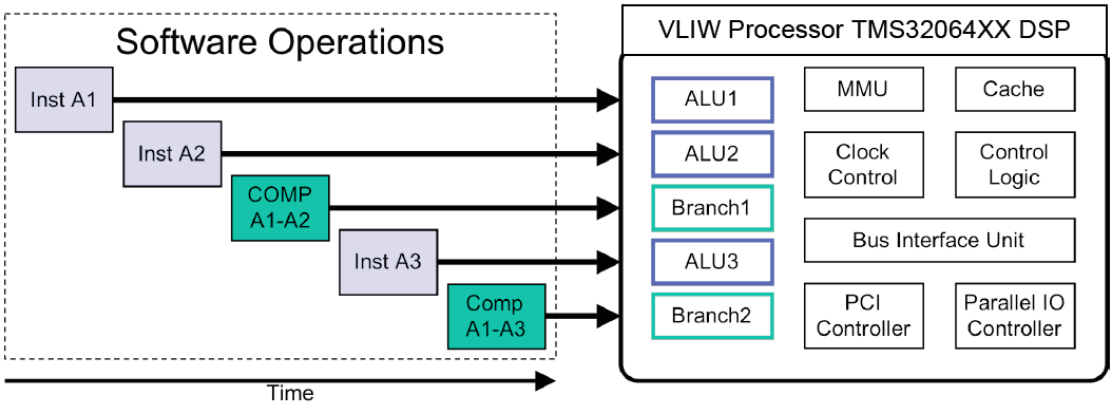
Radiation Hardness of IPC5000

- Radiation Tolerance for Proton200k
  - SEL > 70 LET (MeV-cm^2/mg)
  - SEU < 1 per 1,000 days (10^{-4}, 90% W.C. GEO, Orbit dependent)
  - TID > 100 krad (Si), Orbit dependent
  - SEFI 100% recoverable
- Radiation Tolerance for IPC5000
  - Proton200k level for Fusion Processor, except
    - Power control circuits have risk of SEGR/SEB; mitigated by dual redundancy
  - SSB is equivalent to Fusion Processor, except
    - RAM is not EDAC protected
  - IPC Board

SEU Mitigation Technology

SEU mitigation via patented TTMR™

- Detects and Corrects SEUs
- TTMR™ enables use of State-of-Art commercial Processors
- TTMR™ Combines Time with TMR (Triple-Modular-Redundancy)
  - Time: Leverages the features of Very Long Instruction Word (VLIW) processors for parallel processing of instructions
  - Spatial Triple Modular Redundancy (TMR) operations on separate ALU units within a single DSP. Comparisons will only invoke Instruction set A3 of A1≠A2
- SEU error rate equal to TMR rate
- Proton radiation tested at 51 MeV
- TTMR implementation is transparent to DSP user, Hardware or Software-wise



SEU mitigation via TTMR™

SEFI Mitigation technology

SEFI mitigation via patented H-CORE™

H-CORE™ monitors processor functionality in real time to provide fast detection and correction of any SEFIs occurrences.

- Hardware
  - Rad-Hard external Watchdog circuits sends interrupts and resets as required
- Software
  - CPU – Generates health/status signals , runs interrupt routines
  - HCORE™ IC – Monitors signals, initiates post-SEFI recovery using interrupts, and full reset as required

Current development and production status

Design: 100% complete
Fabrication: 100% complete
Integration: 100% complete
Environmental qualification: 100% complete
In Orbit on semi-classified program

IPC5000 is heritage space qualified product

Thank you for your support!

SPACE MICRO