

American Semiconductor Inc.



This work is sponsored by the
Air Force Research Laboratory (AFRL/RVSE)
TPOC: Mr. Kenneth Hebert

45nm Foundry CMOS with Mask-Lite™ Reduced Mask Costs

24 August 2011

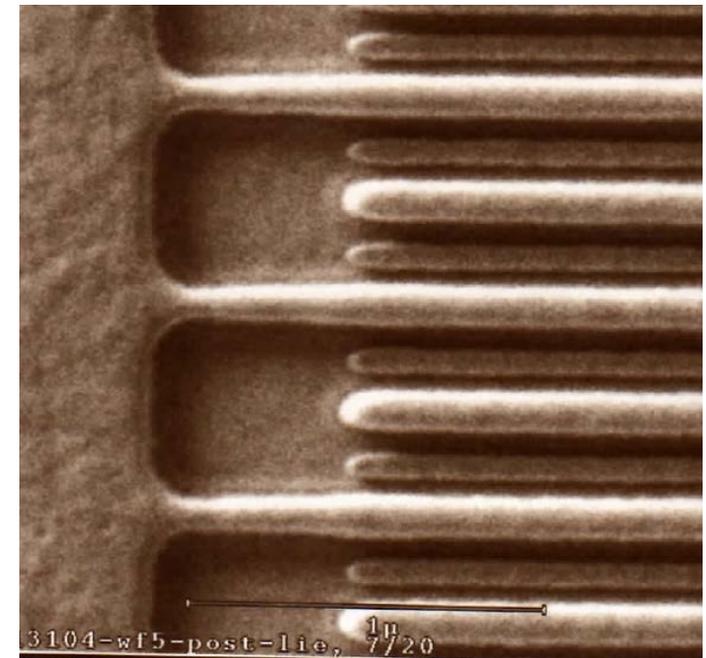
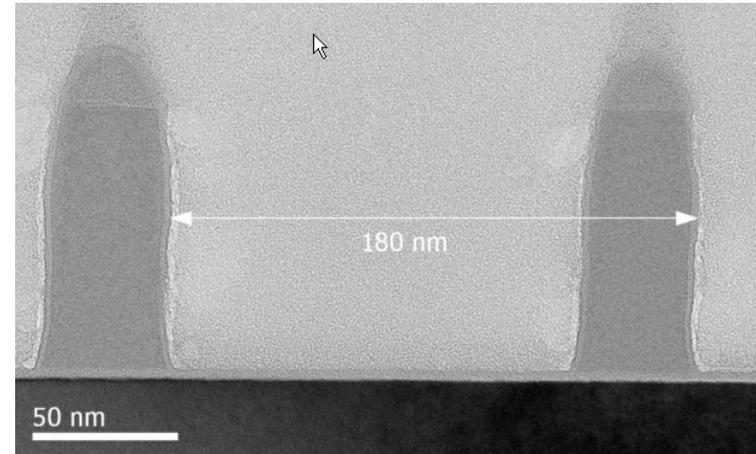


DoME

← 45nm →

Domestic Manufacturing of Electronics

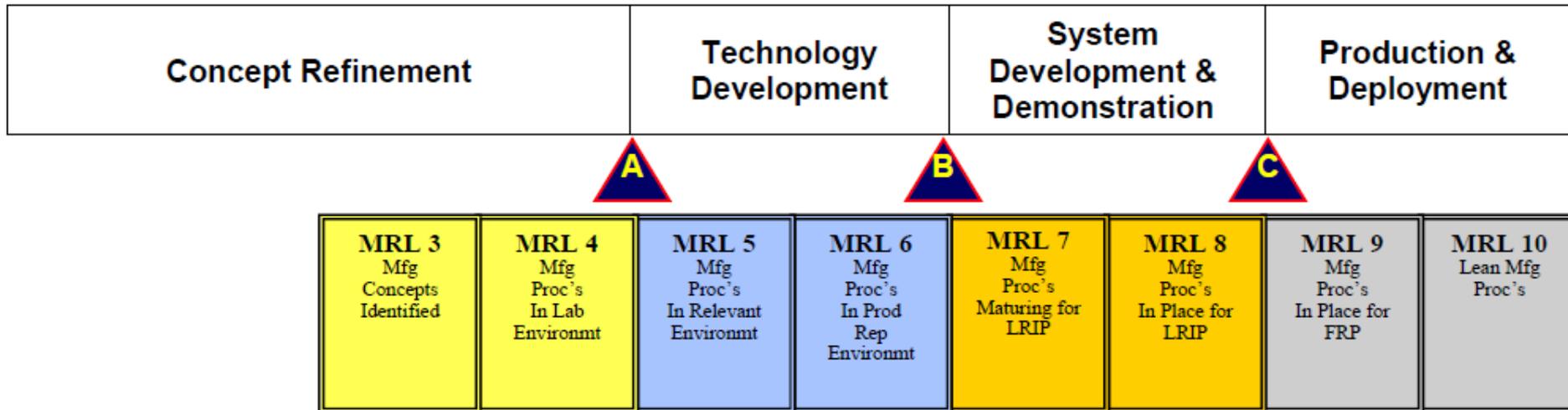
- Mask-Lite™ 1-D/Grated Layout
 - ▶ Reduced Mask Costs
- On-Shore
 - ▶ ITAR Compliant
 - ▶ TRUSTED Capable
- Economically Feasible for Low Volume
 - ▶ DoD
 - ▶ Aerospace
 - ▶ Commercial
- Supports Process Customization



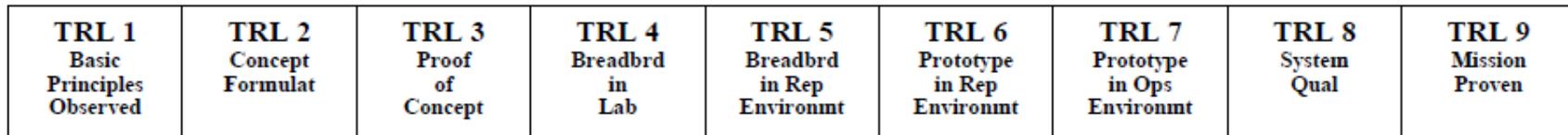
MRL = Manufacturing Readiness Level
TRL = Technology Readiness Level

DoME is a manufacturing capability development program

Relationship To System Milestones

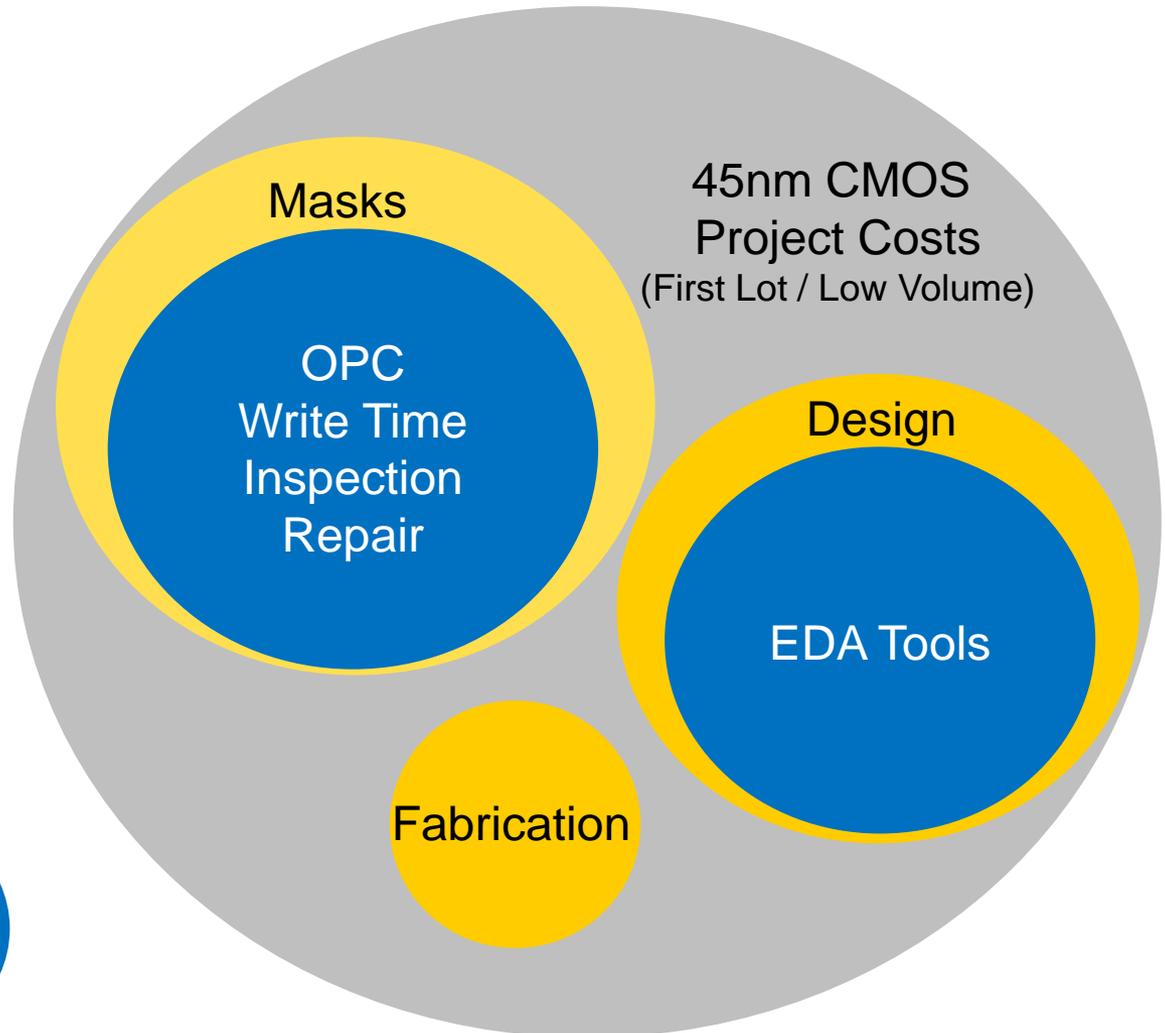


Relationship To Technology Readiness Levels



A 65-nm mask set can cost 1.8 times that of a 90-nm set, while a 45-nm mask set can cost 2.2 times that of a 65-nm set.

- EE Times 10/7/2010





1. AFRL
2. American Semiconductor
 - ▶ Process Integration: PDP, FEOL, Cu BEOL, Design...
 - ▶ Device Engineering/Modeling – Bill Richards 
 - ▶ Radiation Hardening – Randall Milanowski
 - ▶ ITAR, Trusted in Progress. (Design, Fab and Test)

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3. SVTC
 - ▶ Fab1 advanced tool set: XT1250 193nm, .85NA
 - ▶ Fab2 Cu & 45nm baseline (Sematech ATDF, 2007)



4. Tela-Inc
 - ▶ Grated Design & 45nm Commercial Experience
 - ▶ 1D Cell Library



5. Silvaco
 - ▶ Design Tools
 - ▶ PDK and Spice Modeling Support

CMOS and Custom Semiconductor Foundry

- ★ Corporate Headquarters – Boise, ID
 - ▶ Engineering – Design, Process, Modeling
 - ▶ Operations/Fab Management
 - ▶ Test & Characterization Cleanroom
 - ▶ Sales, Marketing, Administration
- Manufacturing – San Jose, CA; Austin, TX (SVTC)
 - ▶ Fab/Process Engineering
- Manufacturing – Specialty Process Modules

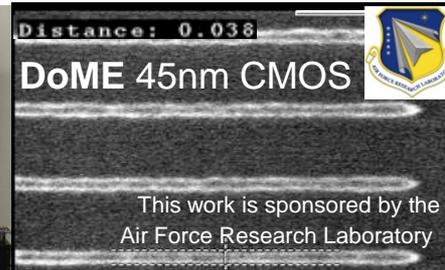
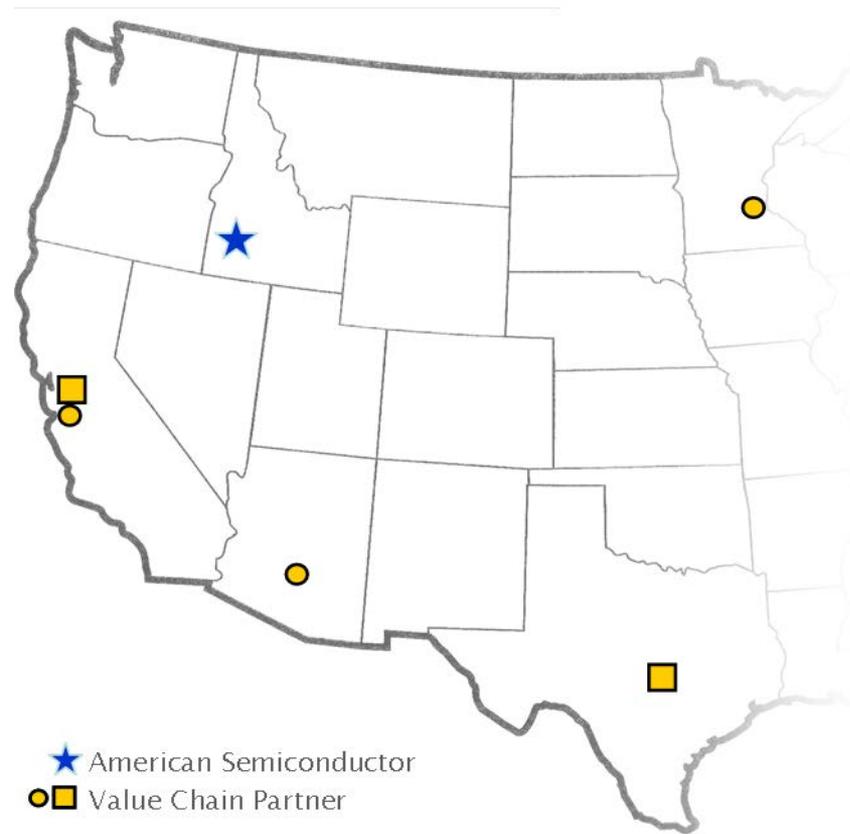
Privately Held

Founded November, 2001

Product Lines

- ▶ Foundry– Your Silicon Made. Simple.
- ▶ FleX™ - Silicon on Polymer
- ▶ Design Services – Turnkey Design Solutions

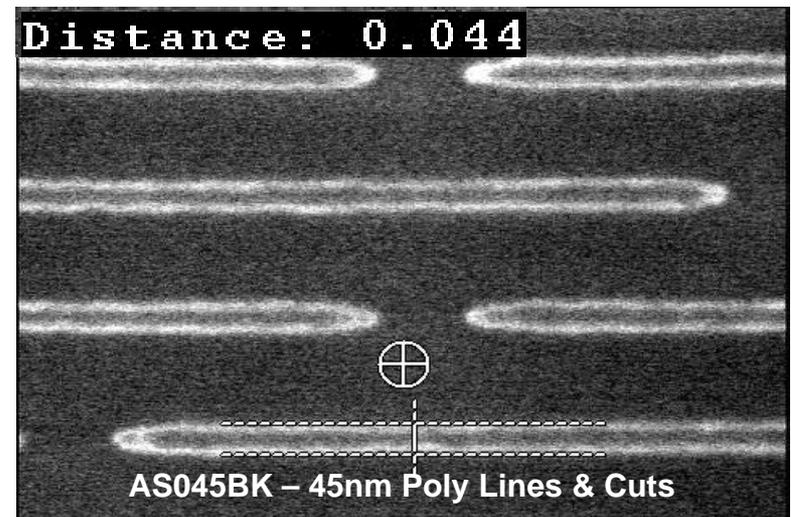
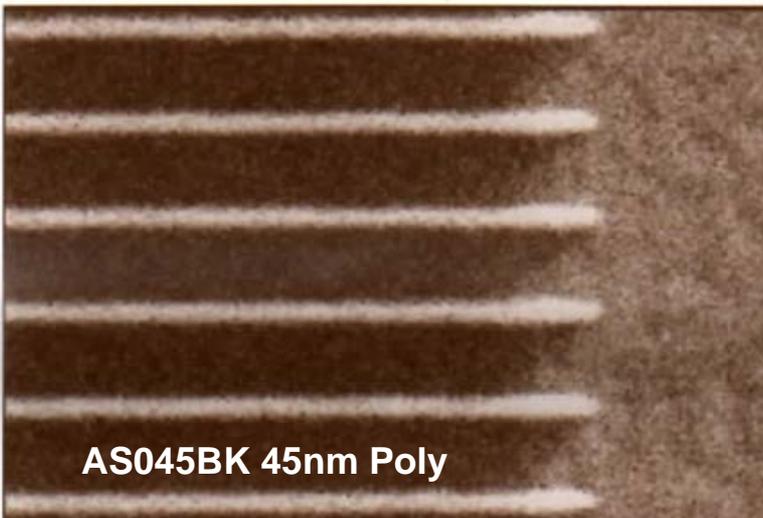
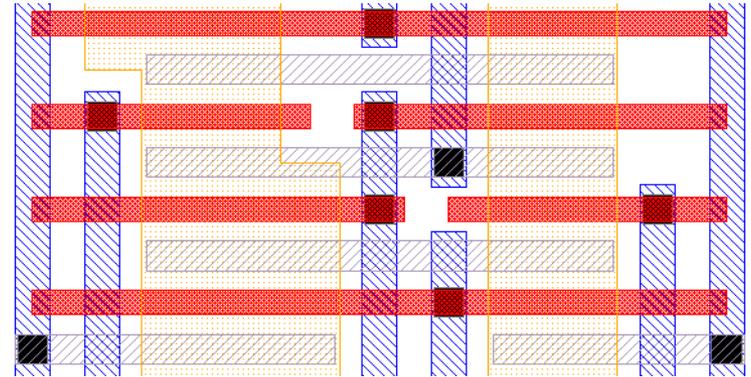
ITAR Compliant; Trusted Certification in Progress



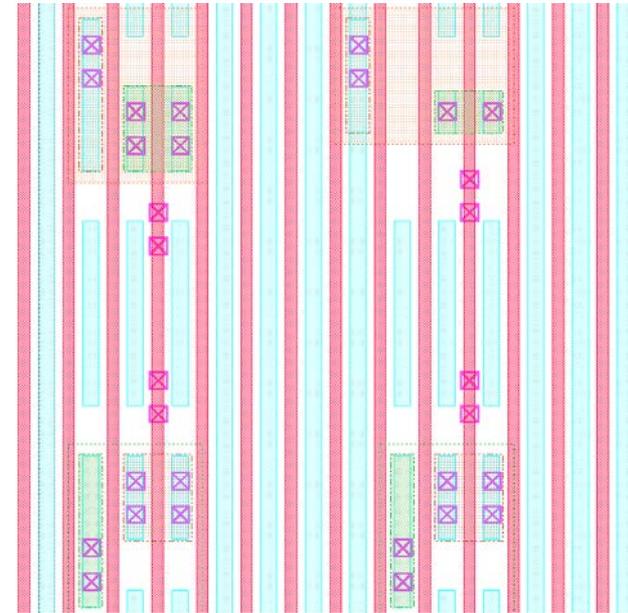
Advanced 45nm CMOS Mask-Lite technology that reduces mask costs up to 90%, making leading edge foundry technology economical for low volume requirements and applications.

Concept

- 1-D straight line geometries
- Non immersion + lower cost reticles



- 1D – geometry
 - ▶ Fixed pitch, straight line vs Traditional 2-D with corners
- Enhances Equipment Capability
 - ▶ 193nm/.85NA 65nm stepper feasible for 45nm and beyond
- Reduced Mask costs
 - ▶ Reduces or eliminates OPC requirements
 - ▶ Reduces mask write time, inspection, and repair
 - ▶ Dry lithography rather than immersion technology
 - ▶ Potential mask reuse from product to product or metal layers (example M1 and M3 masks can be same with different cut masks)
 - ▶ E-beam lithography feasibility (Mask elimination)
- Smaller Die
 - ▶ Tighter rules allow closer geometries at a feature node or...
 - ▶ Same rules with better control for better yield, better timing, better power



- Mask-Lite delivers 77% savings in total MPW wafer lot costs
- Mask costs drive industry multi-project wafer (MPW) lot pricing
- 1-D Mask-Lite technology eliminates major mask cost drivers
 - ▶ Eliminates optical proximity correction (OPC)
 - ▶ Reduces mask write times, inspection costs, and yield loss

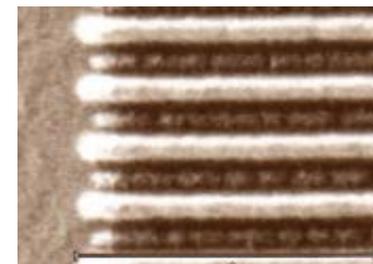
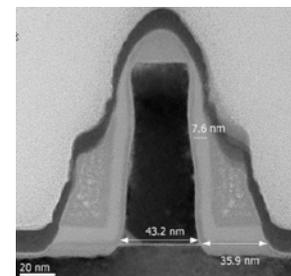
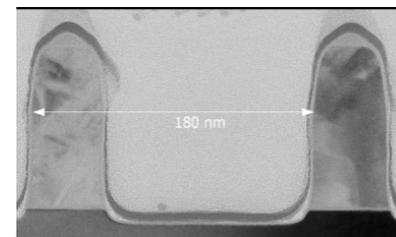
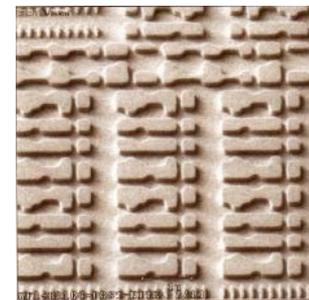
	Traditional 45nm		Mask-Lite™ 45nm	
Active	100%		10%	
Poly	100%		10%	
Local Interconnect	100%		10%	
M1-7	7 x	100%	7 x	10%
Wells, Vt, Strains	10 x	10%	10 x	10%
NSD, PSD	2 x	20%	2 x	10%
Pad Metal/Opening	2 x	10%	2 x	10%
Contacts	2 x	100%	2 x	10%
Vias (6 layers)	6 x	100%	6 x	10%
Cuts (4 layers)	N/A		4 x	10%
TOTAL	100%		16%	
MULTI-LAYER RETICLE SET	N/A		9%	

Fast follower strategy leverages industry development of 45nm tools, technology, and know-how to minimize R&D and production costs

	DoME	IBM	Intel
Process	ASI AS045BK	IBM Trusted Cu-45HP	Intel 45nm CMOS
Availability	Pure-play Foundry	IDM/Foundry	IDM
Mask Cost (tooling)	Low (Mask-Lite™)	Very High	Very High
Material	Bulk	SOI	Bulk
Gate (feature/pitch)	45nm/180nm	45nm/190nm	35nm/160nm
M1 (feature/pitch)	70nm/140nm	TBD	80nm/160nm
Local Interconnect	Yes	No	Yes
Ion N/PMOS $\mu\text{A}/\mu\text{m}$	800/600	1000/800	1360/1070
Gate/GOX EOT	Poly/SiON – HKMG	Poly/SiON	High-k/Met. (HKMG)
Strain	Yes	Yes	Yes
Lithography	193nm/.85NA	193nm/1.35NA	193nm/.93NA
1D Grated	Yes	In R&D only	Yes
BEOL	Cu, low-K, 9 layer	Cu, low-K, 11 layer	Cu, low-k, 9 layer

- DoME is Structured to be Successful
 - ▶ Fast follower strategy implements best known practices for 45nm CMOS (proven commercial technologies, equipment, processes, and knowledge)
 - ▶ Pure play foundry uses existing fabrication facilities and equipment (enables low costs for development, prototyping, and low volume production)
- Early Success
 - ▶ Functional 45nm CMOS transistors
 - ▶ Mask-Lite wafers demonstrated geometries beyond program requirements (showed feasibility to 32nm)
 - ▶ 45nm features at target pitch generated using Mask-Lite low cost reticles

	<u>Process Step</u>	<u>Requirement</u>	<u>Status</u>
1	Epi Thickness	Radiation tolerance	Integration complete
2	Shallow Trench Isolation (STI)	Uniformity and Pitch	Integration complete
3	Poly Sizing	Uniformity and Pitch	Integration complete
4	Spacer	Thickness and Uniformity	Integration complete
5	High Voltage Gate Oxide	Thickness and Etchback	Integration complete
6	Local Interconnect	Pattern & Continuity	Integration complete
7	Gate Dielectric: SION HKMG	Cox & Leakage	Integration complete In progress
8	Strain	PMOS Performance	In progress
9	Copper	Via/Interconnect Size	In progress



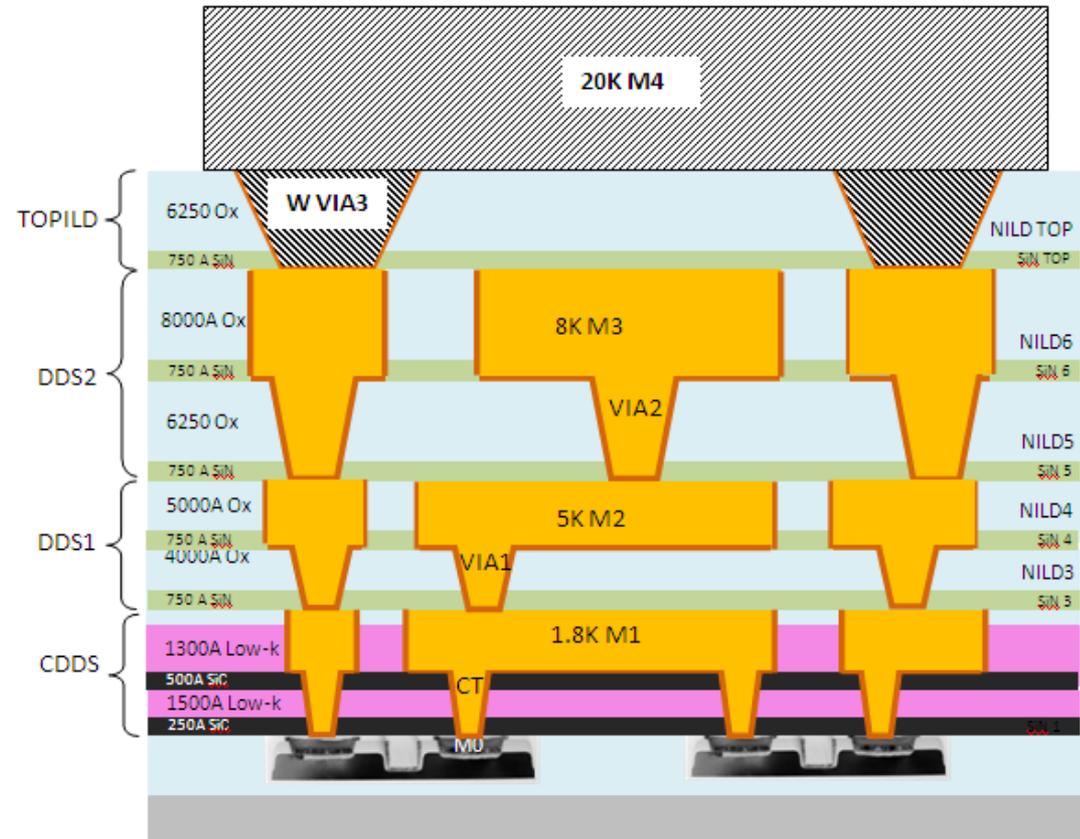
200mm Copper Low-k BEOL

- ✓ 45nm CMOS (DoME BEOL)
- ✓ 90nm CMOS
- ✓ 130nm CMOS (Flexfet BEOL)
- ✓ 180nm CMOS
- ✓ ITAR

Can be bolted on to any FEOL

Process Design Kit

- Metal sheet resistance data
- Contact/via sheet resistance data
- Layout design rules
- DRC and LVS rule decks
- Parasitic extraction rule deck
- Electromigration current limits
- Antenna rules
- Global and local alignment marks



This is a simplified illustration. Layers can be replicated and stacked as needed to meet customer requirements.

Dedicated Runs with Multi Layer Reticles (MLR)

- Your own mask set and dedicated run for less than the cost of traditional 45nm MPWs
- 10mm x 10mm Field
- Suitable for Prototype and Low Volume Production
- ~206 Gross Die Per Wafer (at 10mm x 10mm)
- ~9% Cost of a Traditional SLR 45nm Mask Set

MPW 45nm Multi Project Lots

- 1st Silicon Runs, iterative programs, one-off ASIC's
- 5mm x 5mm Field (typical, 2x2 to 10x10 available)
- Up to 300 die delivered per MPW tile
- MPW runs booking 2012 for R&D and Pre-qualification silicon
- **<25% of today's standard 45nm cost**

Thank You

This work was supported in part by the Air Force Research Laboratory under the following programs:

- DoME - Domestic Manufacturing of Electronics
- SHARE - Systematic Hierarchical Approach for Radiation Hardened Electronics
- CRADL - Commercial Rad-hard Advanced Digital Library
- ULP09 - Flexfet ULP CMOS Circuits for Space Electronics

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