# American Semiconductor Inc.

This work is sponsored by the
Air Force Research Laboratory (AFRL/RVSE)
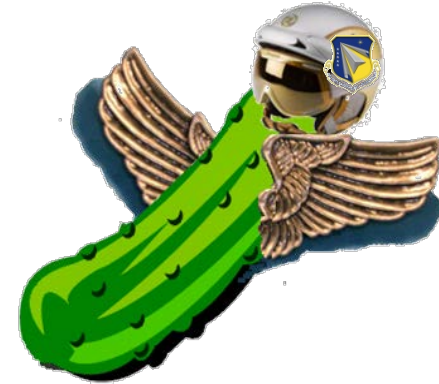TPOC: Mr. Keith Avery

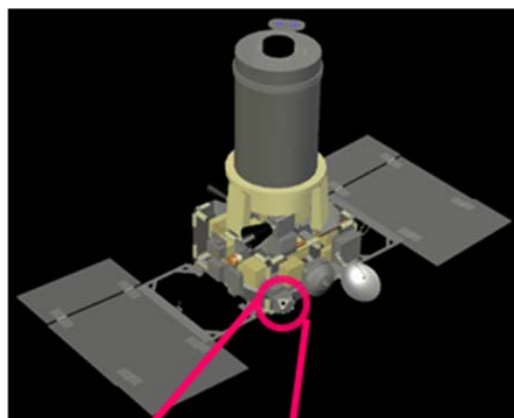# A SPA-1 ASIC Operating at 0.5V Fabricated in 130nm Double Gated CMOS

24 August 2011

www.americansemi.com

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Air Force SBIR/STTR

Goal – Ultra Low Power ASIMs for Satellite Plug-N-Play

- Phase 1 SBIR - Feasibility Demonstration
  - ▸ Ultra low power PIC (picL) microprocessor core
  - ▸ Performance capable of meeting ASIM needs
  - ▸ Radiation tolerant for space applications
  - ▸ Proved feasibility of Double Gate Flexfet technology for ASIC development

- Phase 2 SBIR – Build Prototypes of SPA-1 Mini-PnP ASIC

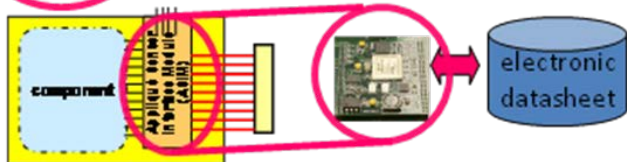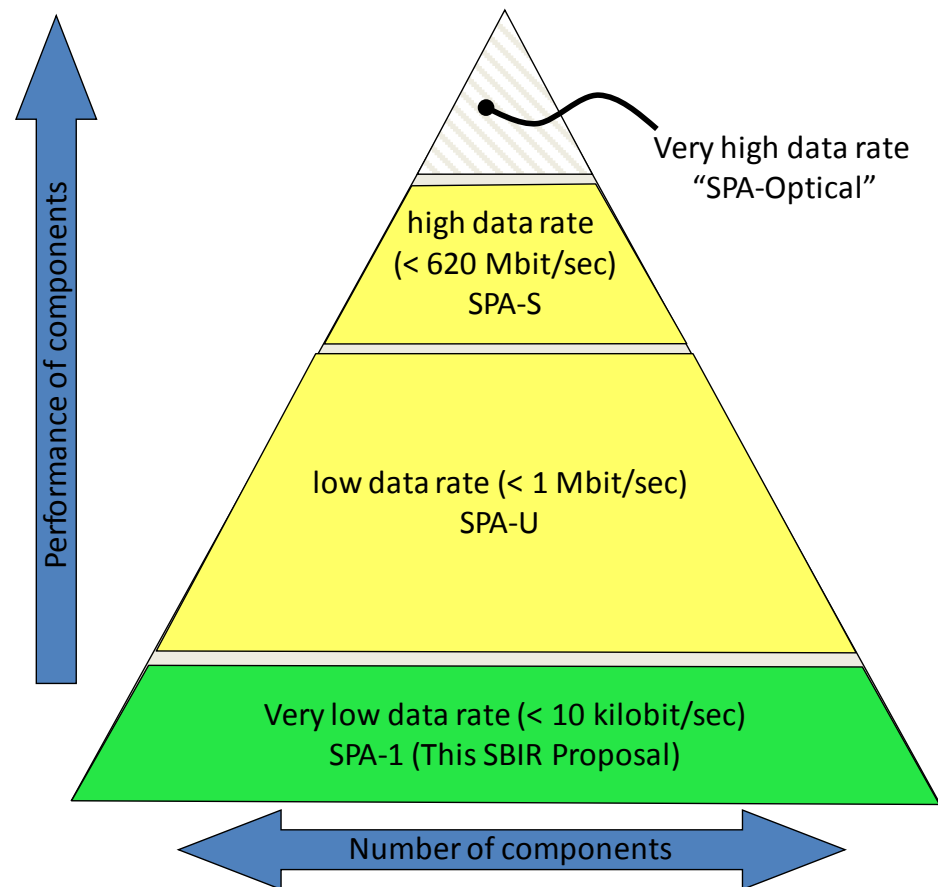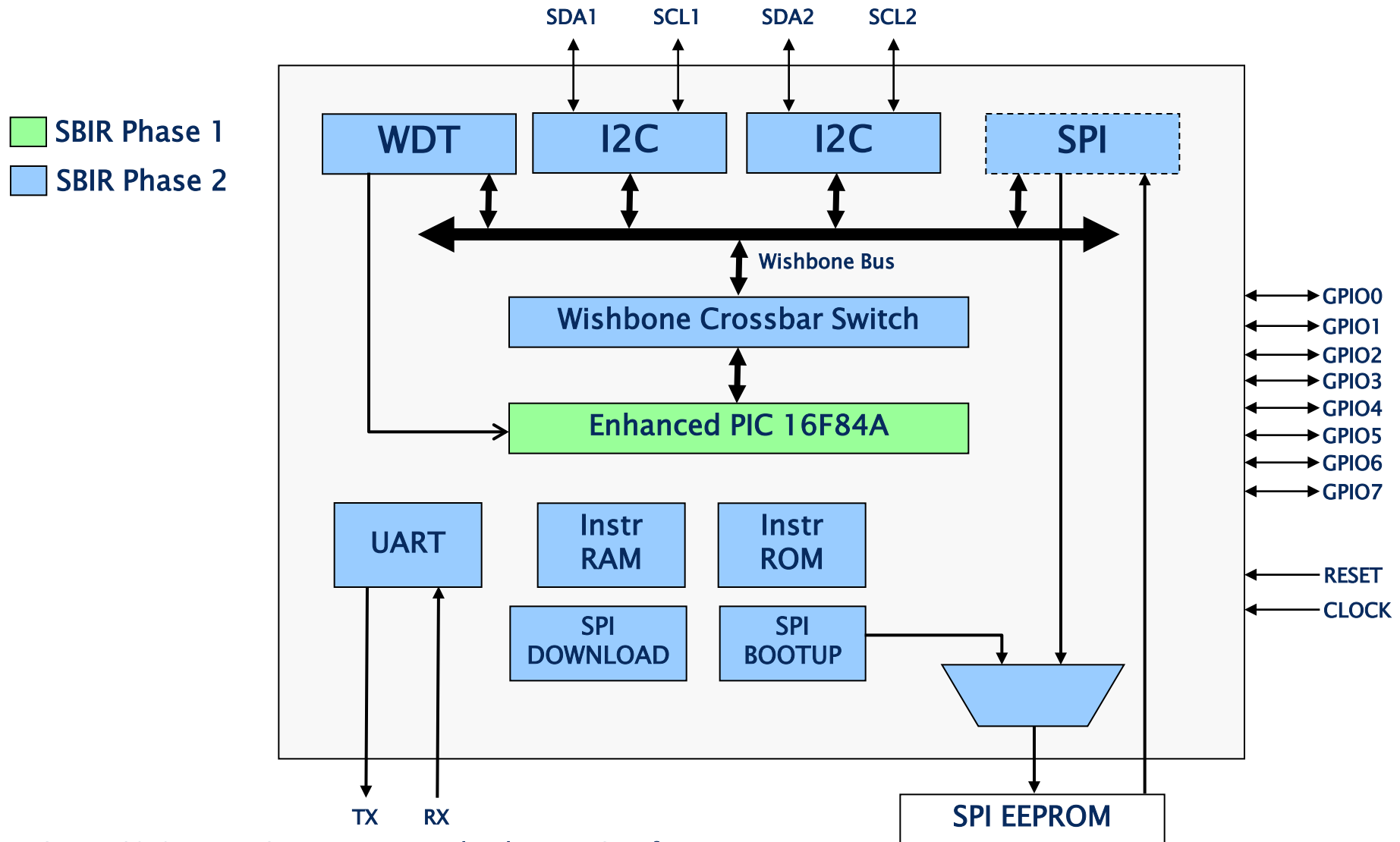- Phase 3 SBIR – Technical Qualifications, Flight Testing, and other ASIM Derivatives (SPA-U, SPA-S, …)

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SPA Satellite

SPA plug-and-play component

SPA interface module

component

Applique Sensor Interface Module (ASIM)

electronic datasheet

Performance of components

Very high data rate "SPA-Optical"

high data rate (< 620 Mbit/sec) SPA-S

low data rate (< 1 Mbit/sec) SPA-U

Very low data rate (< 10 kilobit/sec) SPA-1 (This SBIR Proposal)

Number of components

Source:  J. Lyke, "Bringing the Vision of Plug−and−play to High−Performance Computing on Orbit" HPEC 2009, Sept. 2009
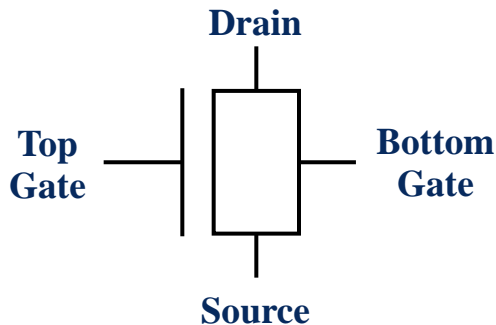
4



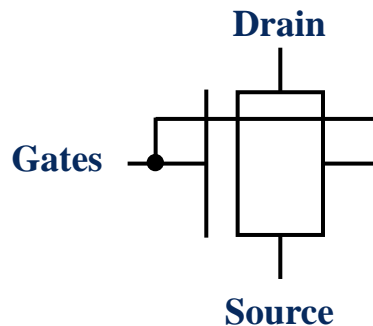Source: 2010 AFRL/RVSE Mini−PnP External Architecture Specification

## Flexfet features

- MIGFET (Multiple Independent Gate FET)
- MUGFET (Multiple Gate FET)
- Fully depleted SOI MOSFET Top Gate
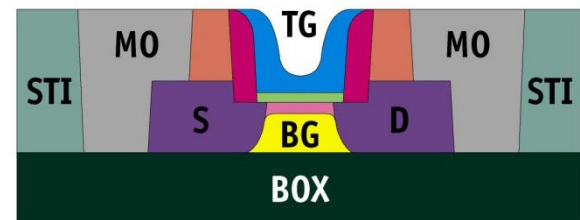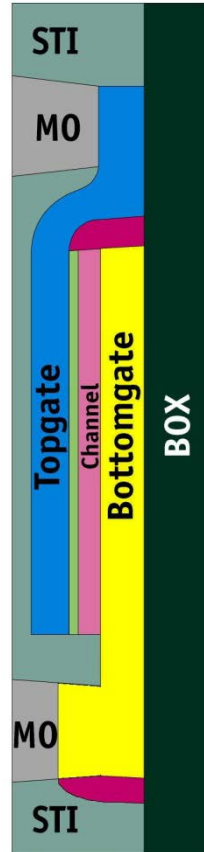- Self-aligned JFET Bottom Gate



MIGFET

**Benefit**
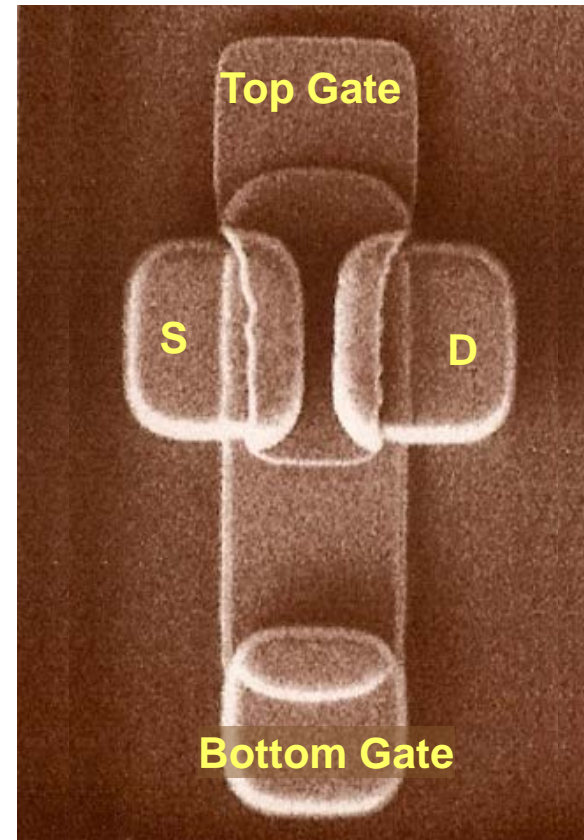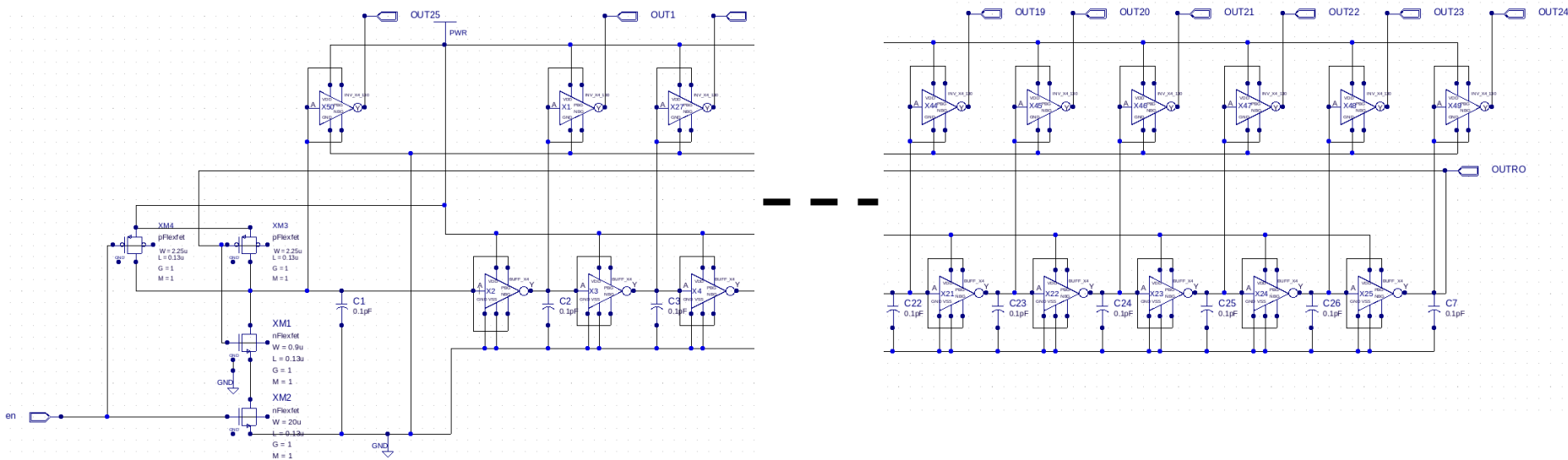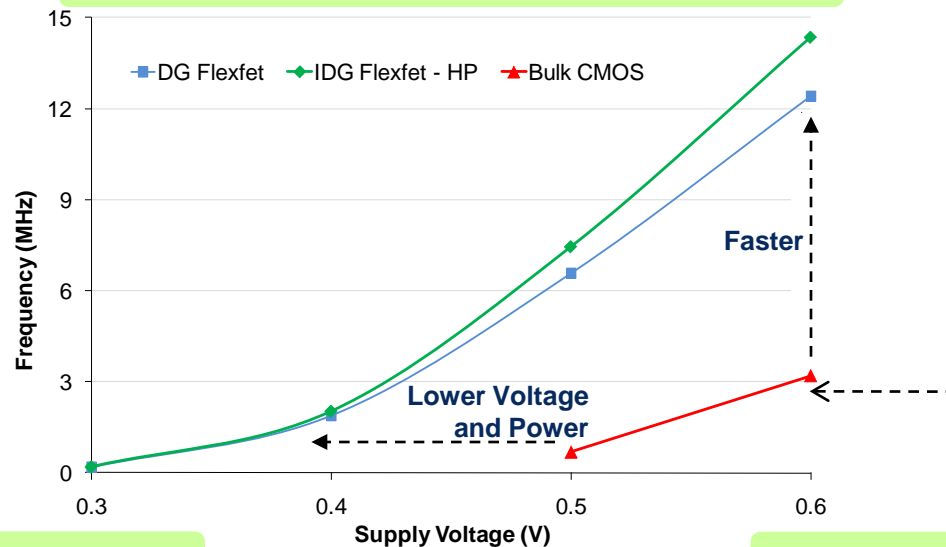**Dynamic Threshold Control**

MUGFET

**Benefit**
**Ultra Low Power**

- Ring oscillator performance comparison
  - 130nm Flexfet IDG, DG, and high volume commercial bulk CMOS
  - 25 inverters with loading of 4x inverter load plus wiring capacitance

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**Frequency – IDG and DG versus Bulk CMOS**

DG Flexfet   IDG Flexfet - HP   Bulk CMOS

Frequency (MHz)

Supply Voltage (V)

**Faster**

**Lower Voltage and Power**

**Conventional 130nm CMOS**



**Static Current: IDG vs. DG**

DG Flexfet   IDG Flexfet - LP

Static Current (nA)

Supply Voltage (V)



**Active Current: IDG vs. DG**

DG Flexfet   IDG Flexfet - HP

Active Current (uA)

Supply Voltage (V)

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## Analog Flow

| Schematic Entry | Spice Simulation | Custom Layout | DRC & LVS | Parasitic Extraction |
|---|---|---|---|---|
| Silvaco Gateway | Silvaco SmartSpice | Silvaco Expert | Silvaco Guardian | Silvaco Guardian |

**Spec**

## Digital Flow

| Design Entry | Behavioral Simulation | Synthesis | Place & Route | Static Timing |
|---|---|---|---|---|
| | Silvaco Silos | Incentia DesignCraft | Silvaco Spider | Silvaco Accucore |

## Mixed–Signal Chip Assembly

| Full-Chip LVS | Full-Chip DRC | Chip Assembly |
|---|---|---|
| Silvaco Guardian | Silvaco Guardian | Silvaco Expert |

**Tapeout**

SILVACO

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| Design Entry | → | RTL Simulation | → | Synthesis | → | Place & Route | → | Static Timing | → | Dynamic Timing |

Silvaco Silos — (RTL Simulation)
Incentia DesignCraft — (Synthesis)
Silvaco Spider — (Place & Route)
Silvaco Accucore — (Static Timing)
Silvaco Silos — (Dynamic Timing)

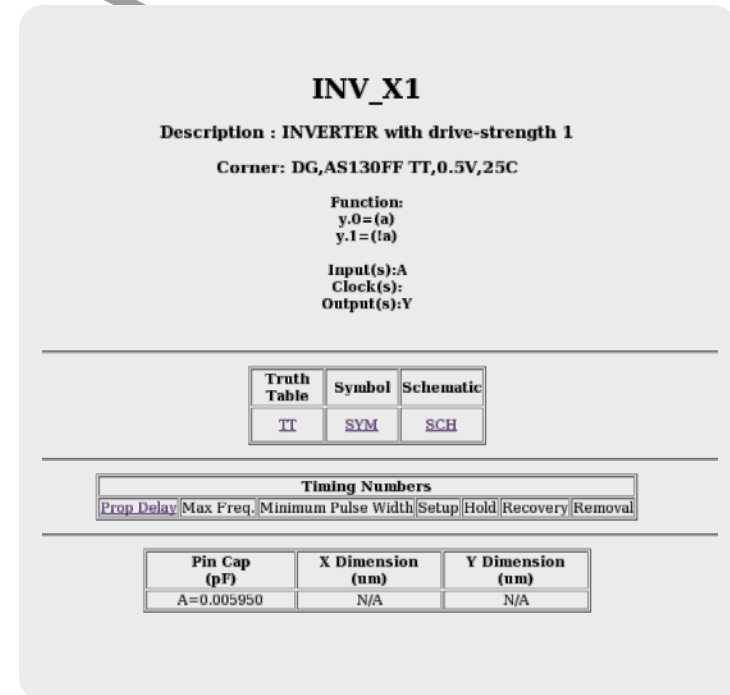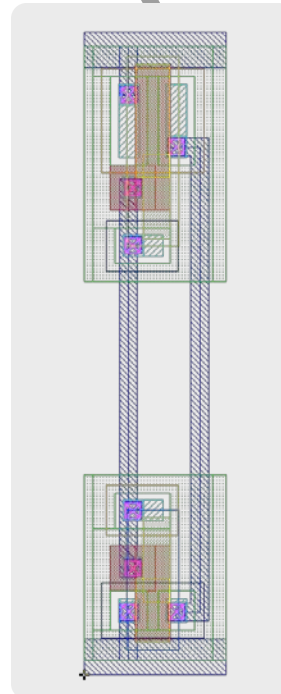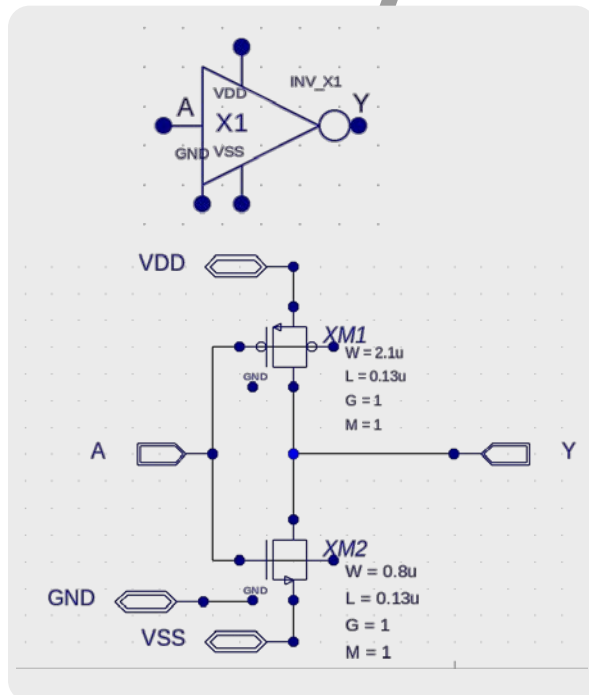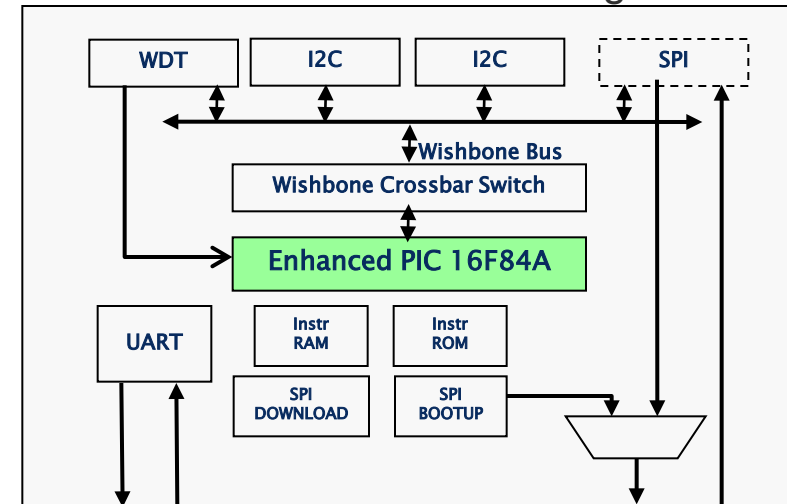| Process Selection | → | Library Prep |

Silvaco Gateway, Expert, Accucell

## Library of Standard Cells
- 47 gate types incl. Flip-Flops and Latch
- Library characterization, Synthesis and Layout successfully completed for picL, Mini-PnP and DG Flexfet Test Chip



INV_X1 schematic: A, X1, Y, VDD, GND VSS

VDD
XM1  W = 2.1u, L = 0.13u, G = 1, M = 1
A ─── Y
GND
XM2  W = 0.8u, L = 0.13u, G = 1, M = 1
VSS



### INV_X1

**Description : INVERTER with drive-strength 1**

**Corner: DG,AS130FF TT,0.5V,25C**

**Function:**
y.0 = (a)
y.1 = (!a)

**Input(s):A**
**Clock(s):**
**Output(s):Y**

| Truth Table | Symbol | Schematic |
|---|---|---|
| TT | SYM | SCH |

| Timing Numbers | | | | | | |
|---|---|---|---|---|---|---|
| Prop Delay | Max Freq. | Minimum Pulse Width | Setup | Hold | Recovery | Removal |

| Pin Cap (pF) | X Dimension (nm) | Y Dimension (nm) |
|---|---|---|
| A=0.005950 | N/A | N/A |

## AFRL Mini-PnP Block Diagram



| WDT | I2C | I2C | SPI |

Wishbone Bus

Wishbone Crossbar Switch

**Enhanced PIC 16F84A**

UART

Instr RAM

Instr ROM

SPI DOWNLOAD

SPI BOOTUP

700um

## picL ULP Core

– PIC 16F84A Core

– 50MHz Synthesis at 0.5V

– Clock tree inserted

– 2063 components

– 2420 signal nets, 1clock net

– 3 layer metal with local interconnect

# Synthesis Comparison

| 50MHz synthesis | Flexfet 0.5V, 130nm | Bulk CMOS 1.5V, 130nm | Unit |
|---|---|---|---|
| Cells used | 2063 | 1610 | # |
| Total Cell Input switching power | 0.43 | 1.41 | mW |
| Leakage Power | 61.9 | 45.2 | nW |
| Average Leakage power per cell | 30.2 | 28.1 | pW |

- No area penalty for Flexfet's second gate

| Std Cell Example | Flexfet 130nm (um²) | Bulk CMOS 130nm (um²) |
|---|---|---|
| NAND2, NOR2 | 58.3 | 53.7 |
| D-type Flip-Flop | 279.9 | 348.5 |
| Inverter x1 | 46.7 | 40.3 |
| Total picL cell area | 183,246 | 183,986 |

## NAND Gates

DG Flexfet 130nm
4.5um X 12.96um

Bulk CMOS 130nm
4.9um X 12.1um

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1400um
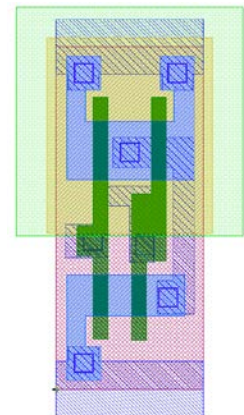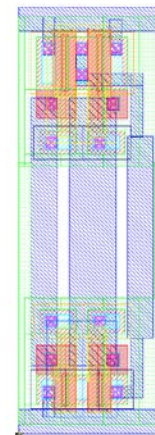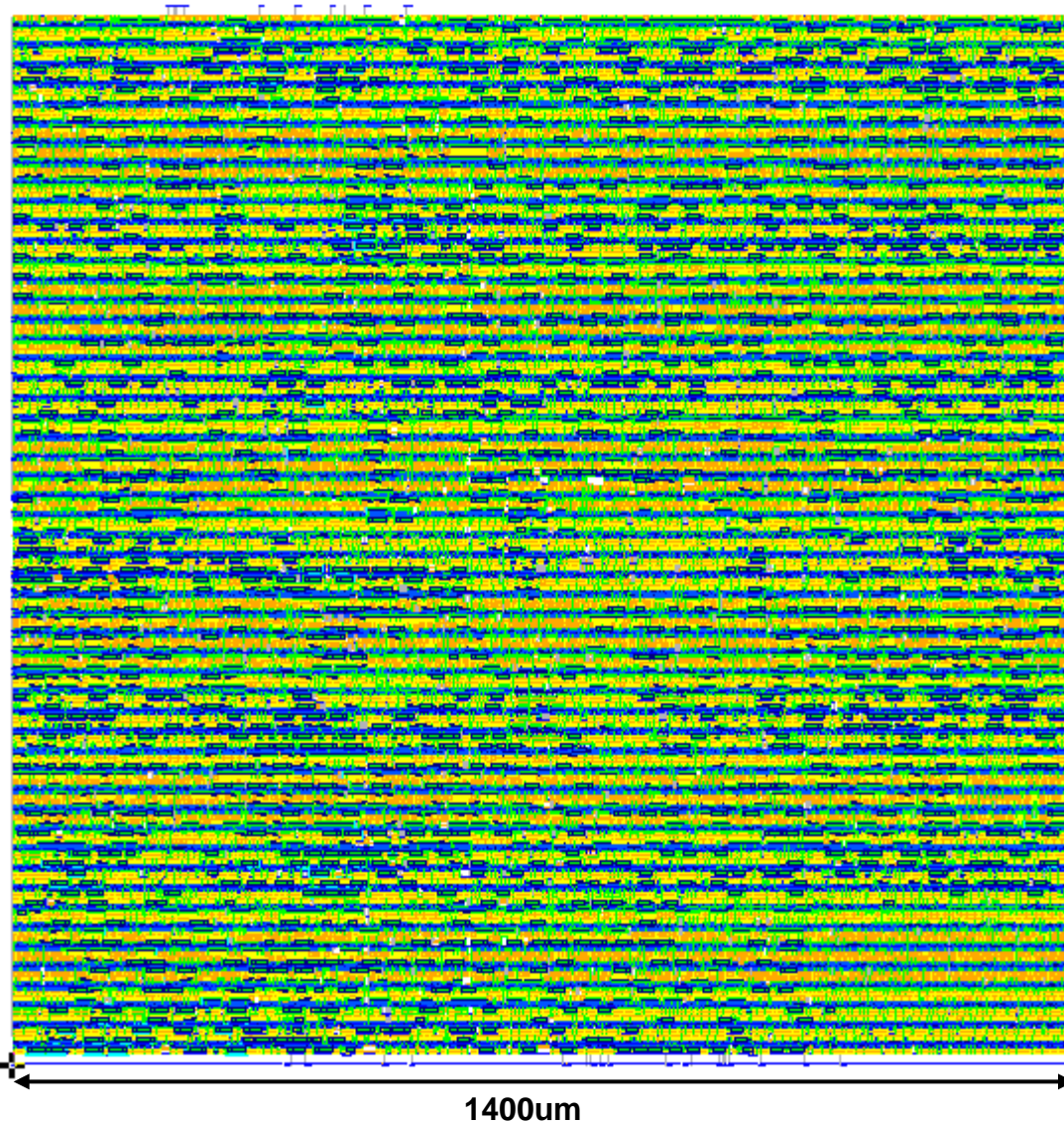
## AFRL Mini-PnP Block Diagram
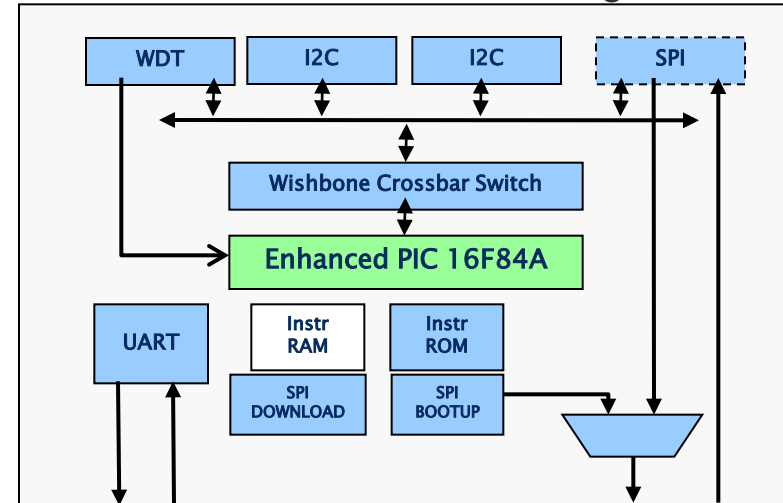


## Top Level Mini-PnP

– Synthesized ROM

– Required Latches, Set and Reset FFs, and Tri-State buffers

– 50MHz synthesis at 0.5V

– Clock tree inserted

– 14504 Components

– 14987 Signals, 1 clock net

– 3 Layer metal

- SEL:  Flexfet is an SOI process (inherently immune to latch-up)

- TID:  Flexfet bottom gate is designed to minimize the effect of charge trapped in the BOX

- SET:  Cell library design - Rising and falling logic delays were balanced to minimize pulse spreading associated with Single Event Transients

- SEU:  Mitigation per AFRL recommendations
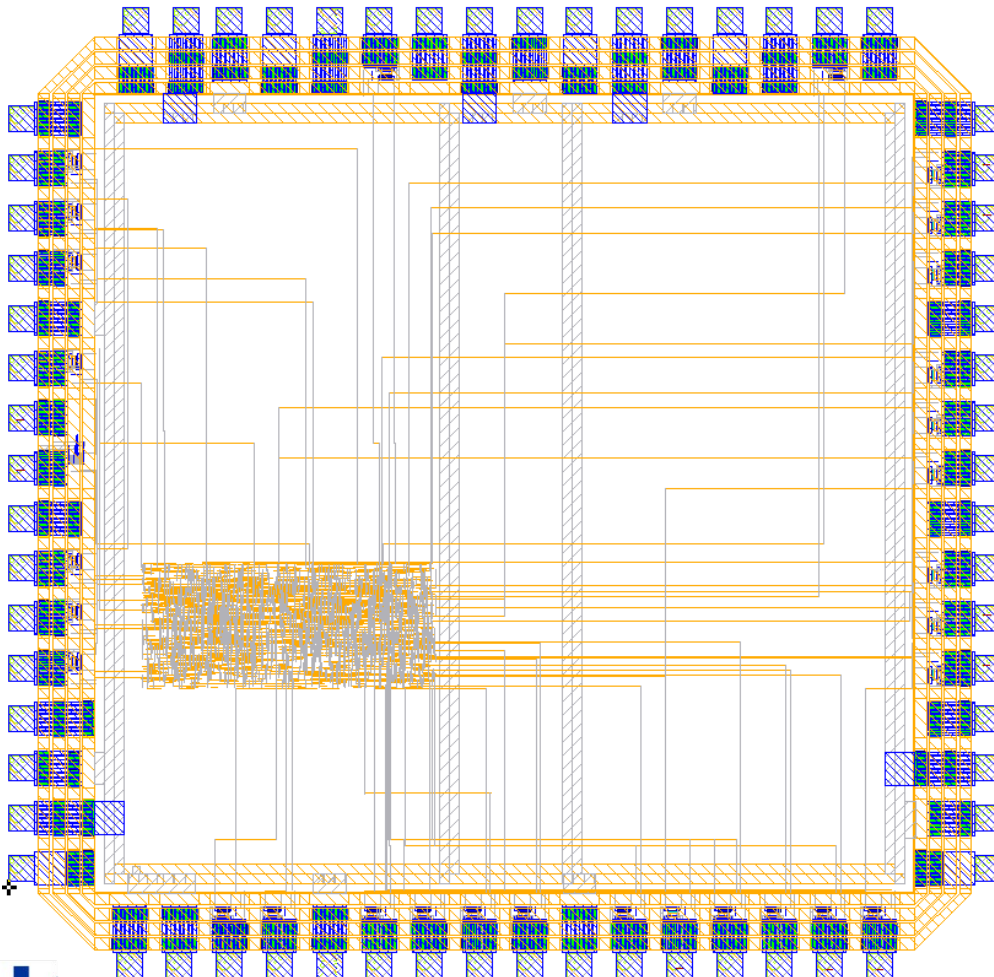  - Added DICE Flip-Flops to DG standard cell library
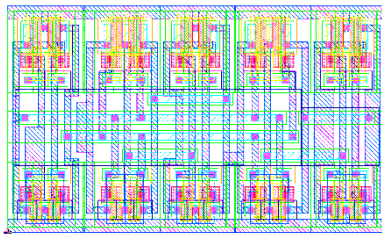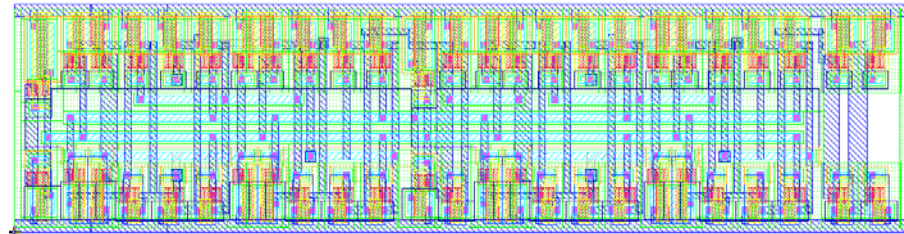
Standard Flip-Flop                          DICE Flip-Flop

  - EDAC to be incorporated into SRAM

- Radiation Testing
  - Pending support and access to AFRL test facilities

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- Silicon in a Phase 1 SBIR

- Design and Layout using 0.5V DG Flexfet cell library and digital design flow developed for picL

- Demonstrates 0.5V DG Standard Cells

- Evaluates SPICE models against silicon results

- Enhances Phase 2 effort

Test Chip Circuits
- 16-bit configurable Timer
- Scan chain with all combinatorial logic gates observable
- Ultra low voltage pads (0.5V)
- Clock oscillator for use with external crystal

In cooperation with the ULP'09 program AFRL/RVSE

- Phase 1 – Complete
  - Technology evaluation
  - Microprocessor core selection
  - Library preparation and design flow development
  - Performance, power, and radiation tolerance analysis
  - Test circuits in silicon
  - Initial place and route of SPA-1 ASIM RTL
- Phase 2 – Awaiting Contract
  - ASIM ULP SPA-1 Prototype Design Start 2011
    - Detailed device specification
    - RTL design optimization
    - Rad-hard SRAM with compiler
    - Rad-hard ROM with compiler
    - I/O library
  - 1st Silicon ULP SPA-1 Prototype 2012
  - 2nd Silicon ULP SPA-1 Prototype 2013
- Creates Platform and Design Capability for Derivative Products
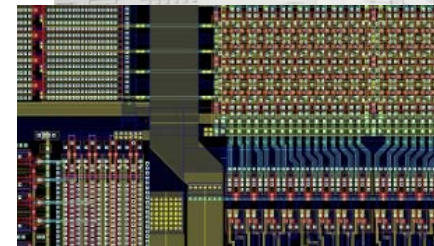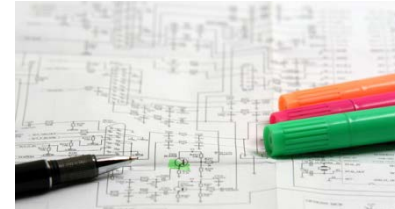
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# Thank You

View a video demonstration of ultra-low-power Flexfet at
americansemi.com/Flexfet

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