Electrical Performances and Radiation Qualification Test Results of a Highly Integrated and Space Qualified Point of Load Converter

Timothée Dargnies
1. Introduction to Point of Load (PoL) Converters
2. 3D Plus Point of Load characteristics
3. Radiation effects mitigation techniques
4. Radiation Test Description and Results
5. Conclusion
1. Introduction to Point of Load (PoL) Converters

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5. Conclusion
Introduction to Point-Of-Load (POL) Converters

A Point-Of-Load Converter is a highly miniaturized and high performance DC/DC Converter used as a key element:

- to simplify the architecture of a low voltage power distribution system for ASICs, FPGAs (ACTEL, XILINX,…) and Memory (SDRAM, DDR, DDR2,…) and
- to increase the flexibility and the efficiency of the Power Distribution for Space Applications

Typical Power Distribution Architecture with POL Converters

![Diagram of typical power distribution architecture with POL converters]

**Typical Application’s schematic with 3D Plus POL Converter:**

The POL can be commanded ON by application of a voltage greater than 3.3V on the ON pin.

The Output voltage is locally sensed by Vsense. Vout is set to 3.3V by selecting R1 = 1.33kΩ.
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General Features:

- Radiation Hardened design
- Space Qualified Product (fully screened High Rel. component)
- Simplified and Optimized
- Flexible and Scalable (adjustable output voltages, ON/OFF command for sequencing capability – one single product with bulk procurement for multiple applications)
- Small Size, Low Weight (as it can be used multiple times on a board)
- Low Cost (one type procured and used multiple times on a board)
- All-in-One Component, easy to use (No need for additional glue electronics and input/output filters – easy to use on a digital board)
- Worldwide Delivery guarantee – Free of Exports Restrictions (ITAR Free)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>5V ± 5%</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>Adjustable down to 1.25V</td>
</tr>
<tr>
<td>Output Current</td>
<td>5A max</td>
</tr>
<tr>
<td>Efficiency</td>
<td>&gt; 88% (3.3V/3A)</td>
</tr>
<tr>
<td>EMC Filters</td>
<td>Integrated</td>
</tr>
<tr>
<td>ON/OFF Command</td>
<td>External</td>
</tr>
<tr>
<td>Dimensions</td>
<td>26.5 x 25 x 10 mm</td>
</tr>
</tbody>
</table>
- Buck topology at fixed frequency (400kHz)
- Integrated Input and Output filters
- All needed functions are provided to the users to simplify system integration:
  - Input under voltage detection,
  - Internal over temperature protection,
  - Secondary Over Load Protection,
  - Power Good signal for Output voltage monitoring,
  - ON/OFF Command with Soft Start function.
- Output voltage adjustment in the range 1.2V to 4V thanks to an external resistor
- Manufacturing based on 3D Plus Space Qualified Stack Technology
- Radiation Hardened by design and relevant add-on parts selection
POL Start-up by TC ON
CH1 = ON, CH2 = Vout, CH3 = PGood

POL at output short circuit application
CH2 = Vout, CH3 = Iout

POL restart when Short circuit is removed
CH2 = Vout, CH3 = Iout
3D Plus POL Converter Performances

POL Transient Response
\[ I_{\text{out}} = 1 \text{A to 4A} / V_{\text{out}} = 3.3 \text{V} \]

Noise at module output for 3.3V/3A

Efficiency vs output load (Vin = 5V)
\[ V_{\text{out}} = 3.3 \text{V (Blue)} / 2.5 \text{V (Red)} / 1.5 \text{V (green)} \]
- Full Discrete Electrical Design spread over 3 Layers:
  - 2 OP Amps – 2 types
  - 1 Comparator – 1 type
  - 1 Voltage Ref. – 1 type
  - 2 Standard Logic – 2 types
  - 5 bipolar Transistors – 1 type
  - 1 MOSFet – 1 type
  - 14 Shottky Diodes - 3 types
  - 87 passive devices (CC and CR) various types

113 Components in Total

- Very Dense Physical Lay-out – 3D Stack of 25 x 26 x 10 mm:
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Radiation effects mitigation techniques

- **Buck Topology**
  P-Channel MOSFET for the high side switch of the Buck converter for its immunity to SEE.
  Schottky diode for the low side switch. This avoids the risk of input short circuit if two transistors are commended ON at the same time following a perturbation in the control/command circuits due to a Single Event.

- **RC filters on Integrated Circuit supplies**
  Serial resistor to limit the IC supply current and minimized capacitor value to reduce the peak current when Single Event arrives
  => Reduced risk of latch-up & No permanent damage.

- **Filters at IC outputs**
  RC filters at IC outputs reject potential transient perturbations due to an heavy ions (SET) without modifying the POL operation.

- **Large capacitor values at POL output**
  This solution is selected for two reasons:
  - to reduce voltage change at POL output in case of output current transient,
  - to cancel output voltage perturbation if POL control circuits are disturbed during few switching cycles by a Single Event.
Radiation effects mitigation techniques

- **POL State not latched**
  
  ON/OFF state of the POL converter is set by an external permanent command. This solution avoids storing the state into a digital latch (or something equivalent). State of the POL cannot be permanently changed by a Single Event.

- **Charge Pump to Power the MOSFET driver**
  
  Higher supply voltage for the MOSFET driver to have margins on the ON/OFF voltage level for the P-Channel MOSFET of the power cell.
  
  Margins allow the POL to tolerate the drift on the gate voltage threshold due to the cumulated irradiation dose.
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SEL/SEGR tests were performed at UCL for each basic device

- According ESCC-25100 and JEDS57, on 3 unscreened components
- At high temperature (+125°C) to be in the worst case and cover the operation temperatures of the product.
- At 66 MeV.cm²/mg & **80 MeV.cm²/mg**
- Fluence: $10^6$ to $10^7$ particles / cm²
- Worst case bias as per the POL design justification document (Application specific)
- Monitoring of:
  - Power supply Voltage and current for SEL
  - Drain/Gate Voltages and currents for SEGR (MOSFET)
Example of the SEGR test for the P channel transistor embedded in the POL product:

**Test Biasing Configuration**

**Device preparation**

**Irradiation and Test**

**Results and Conclusion**
## Radiation Description & Tests Results – SEL/SEGR (3/3)

<table>
<thead>
<tr>
<th>Type</th>
<th>SEL (per mask)</th>
<th>SEGR/SEB (per mask)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>In Accordance With PoL design Requirement</td>
<td></td>
</tr>
<tr>
<td>Diodes</td>
<td>Immune</td>
<td>Immune</td>
</tr>
<tr>
<td></td>
<td>Immune</td>
<td>Immune</td>
</tr>
<tr>
<td></td>
<td>Immune</td>
<td>Immune</td>
</tr>
<tr>
<td>Transistors</td>
<td>Immune</td>
<td>Immune</td>
</tr>
<tr>
<td></td>
<td>Immune</td>
<td>&gt;80MeV</td>
</tr>
<tr>
<td>Inverter</td>
<td>&gt;80MeV</td>
<td>Immune</td>
</tr>
<tr>
<td>D-Latches</td>
<td>&gt;80MeV</td>
<td>Immune</td>
</tr>
<tr>
<td>Comparator</td>
<td>&gt;80MeV</td>
<td>Immune</td>
</tr>
<tr>
<td>Ampli-Ops</td>
<td>&gt;80MeV</td>
<td>Immune</td>
</tr>
<tr>
<td>Voltage Ref.</td>
<td>Immune</td>
<td>Immune</td>
</tr>
</tbody>
</table>

=> The POL Converter is guaranteed for 80 MeV.cm²/mg at +125°C
SEU/SET tests were performed at UCL for each basic device

- As part of the product design and characterization activity,
- According ESCC-25100 and JEDS57, on 3 unscreened components at ambient temperature.
- Starting at 80 MeV.cm²mg and decreasing LET till determine the SET threshold.
- A run is stopped for a Fluence of $10^6$ particles / cm² or after 100 events.
- Worst case bias as per the POL design justification document (Application specific)
- Monitoring of the Outputs
Example of the SET test for the voltage reference embedded in the POL product:

- Test Biasing Configuration
- Device preparation
- Tests at UCL facilities

**SET Results – Worst case**

- Analysis in Accordance with the POL Design Requirements
- Improvement of mitigation
- Hard Ware

Updated SET immune schematic
SET tests at POL product level performed

- To Guarantee system Immunity
- On 3 samples of the 2D POL board with de-capped active semiconductor devices (4 sensitive references)
- performed at 25°C at UCL,

- Successive irradiation of sensitive devices
- Vout monitoring
No SET observed at the output of the POL Converter thanks to its Rad Hardened design.
TID tests were performed at UCL for each basic device

- Lot dependent test => Procurement of the largest batch as possible for each active device.
- According ESCC-22900 on 10 components,
- Worst case bias as per the POL design justification document (Application specific)
- 60Co source
- Maximum dose rate : 230 rad(Si)/h
- Up to 50 krad(Si) with interim tests
- Results analysed regarding Manufactures datasheets and PoL Design requirement.
Example of the TID test for a fast comparator embedded in the POL product:

**Test Biasing Configuration**

<table>
<thead>
<tr>
<th>Samples</th>
<th>1 to 5</th>
<th>6 to 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias Configuration</td>
<td>Configuration 1</td>
<td>Configuration 2</td>
</tr>
<tr>
<td>High Current Sensing</td>
<td>Low Current Sensing</td>
<td></td>
</tr>
<tr>
<td>Assembly technology</td>
<td>Brazed on PCB</td>
<td>Brazed on PCB</td>
</tr>
</tbody>
</table>

**Irradiation & test**

**Results**

- Analysis in Acordance with The POL Design Requirements

**Conclusion**
## Test results

<table>
<thead>
<tr>
<th>Type</th>
<th>IAW Manufacturer Datasheet</th>
<th>IAW PoL design Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Diodes</strong></td>
<td>&gt;50Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td></td>
<td>&gt;50Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td></td>
<td>&gt;50Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td><strong>Transistors</strong></td>
<td>&gt;50Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td></td>
<td>&gt;50Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td><strong>Inverter</strong></td>
<td>7Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td><strong>D-Latches</strong></td>
<td>5Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td><strong>Comparator</strong></td>
<td>&gt;50Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td><strong>Ampli-Ops</strong></td>
<td>9.8Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td></td>
<td>4.9Krad</td>
<td>&gt;50Krad</td>
</tr>
<tr>
<td><strong>Voltage Ref.</strong></td>
<td>15.4Krad</td>
<td>&gt;50Krad</td>
</tr>
</tbody>
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=> PoL Converter is guaranteed for 50 krad(Si)
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Thanks to the design and test methodology applied to develop its POL module, 3D Plus has demonstrated performance and the radiation hardening of the product:

- TID: >50 Krads
- SEL/SEGR: 80 MeV/mg.cm² at +125°C
- SET: Immune

3D Plus proposes a highly integrated and Space Qualified PoL Converter

- Flight models available since December 2010
- -> 500 pcs delivered in August 2011.
- Detailed datasheet and application note (examples of use) available

For in depth evaluation, a Demo Board is available on request.
Don’t hesitate to contact us to discuss your needs…in the 3rd Dimension:

**www.3d-plus.com**

“Innovating for More Electronics in Less Space”

<table>
<thead>
<tr>
<th>Technical Center</th>
<th>Sales Center</th>
</tr>
</thead>
<tbody>
<tr>
<td>3D Plus USA Inc.</td>
<td>3D Plus USA Inc.</td>
</tr>
<tr>
<td>43136-108 Christy Street</td>
<td>6633 West Eldorado Pkwy - Suite 420</td>
</tr>
<tr>
<td>Fremont, CA, 94538</td>
<td>McKinney, TX, 75070</td>
</tr>
<tr>
<td>Tel: (510)824-5591</td>
<td>Tel: (214)733-8505</td>
</tr>
<tr>
<td><a href="http://www.3d-plus.com">www.3d-plus.com</a></td>
<td><a href="http://www.3d-plus.com">www.3d-plus.com</a></td>
</tr>
<tr>
<td><a href="mailto:tdargnies@3d-plususa.com">tdargnies@3d-plususa.com</a></td>
<td><a href="mailto:jquinn@3d-plususa.com">jquinn@3d-plususa.com</a></td>
</tr>
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