



Single Event Upset Tolerant Sub-100nm Electronics for Space Craft Systems

Sterling R. Whitaker¹, Gary K. Maki¹ Paul Winterrowd², Lowell Miles¹, Penshu Yeh³, Larry R. Foore⁴, and Richard Meitzler²

¹ICs, LLC,

²Applied Physics Laboratory Johns Hopkins University,

³NASA Goddard Space Flight Center,

⁴NASA Glenn Research Center

August 24, 2011

ReSpace/MAPLD 2011



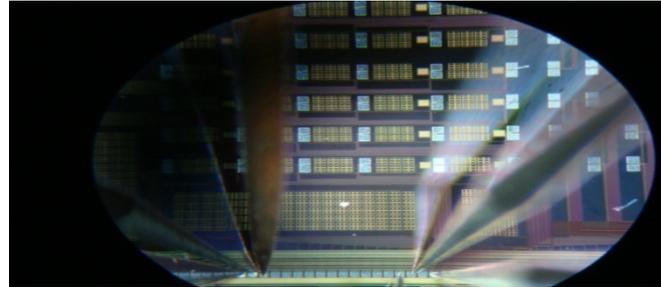
1

8/24/2011

NASA SBIR NNX11CD99P

DARPA N66001-08-1-2075

Motivation for Sub-100nm Commercial Electronics



Higher Density

Higher Speed

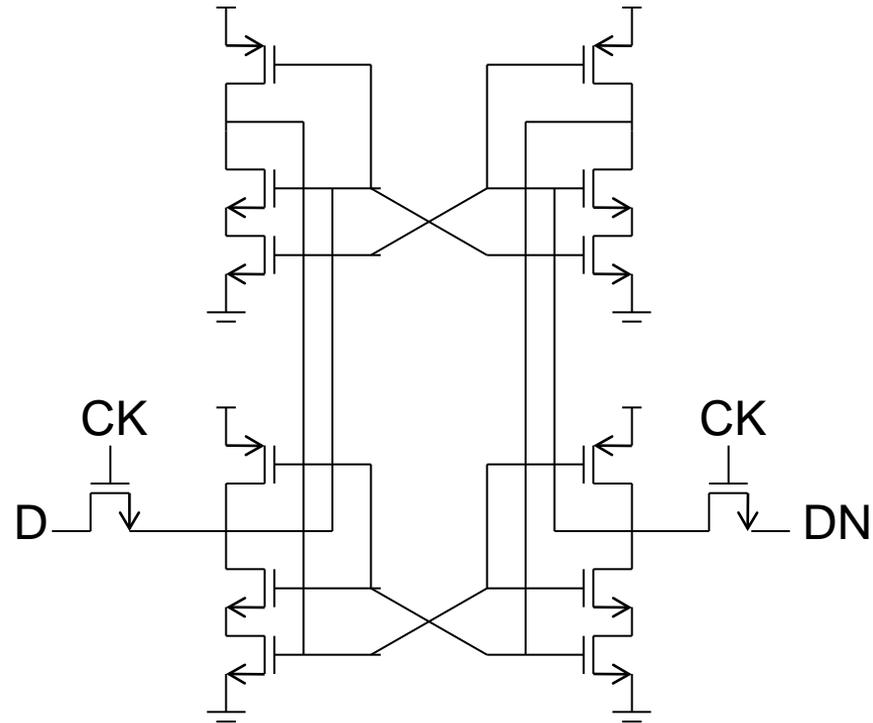
More System Performance

Sub-100nm Radiation Tolerance

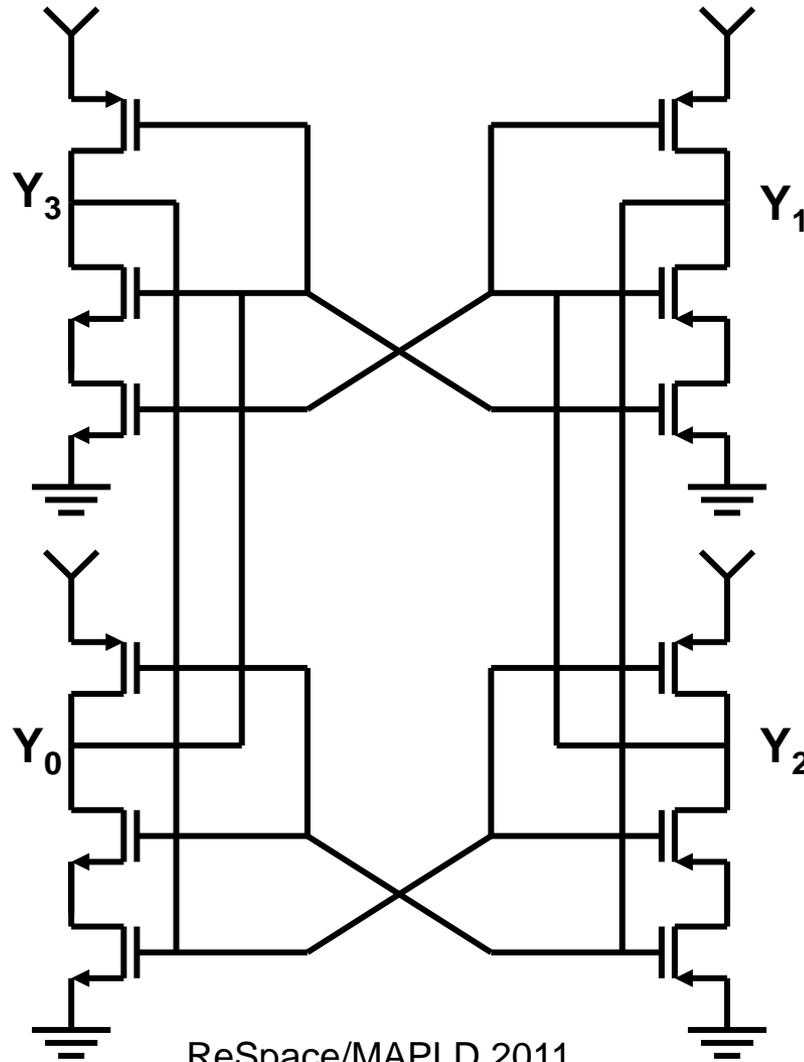
- **Single Event Effects:** Total dose and latch-up protection look good
- **Problem 1:** Multiple clock cycle SEU duration
- **Problem 2:** Single Event Upsets
 - NASA needs 40 LET
 - 0.25um processes flip flop designs > 100 LET
 - Sub-100nm legacy flip flop designs < 5 LET
- **Solution:** Self Restoring Logic (SRL)
 - Initial test chip designed, fabricated, functionally tested, SEE tested

RHBD – Legacy SERT Latch

- **Math based design**
 - Asynchronous Sequential State machine
 - ECC State Assignment
 - Licensed to ICs
- **Applied**
 - Many VLSI chips
 - SEU > 120 LET
- **Constraints**
 - Node Spacing



SERT Latch Next State Equations



$$Y_0 = y_1y_3(0) + y_1'(1)$$

$$Y_1 = y_0y_2(0) + y_2'(1)$$

$$Y_2 = y_1y_3(0) + y_3'(1)$$

$$Y_3 = y_0y_2(0) + y_0'(1)$$

SERT Latch

Asynchronous Circuit Model

y_0y_1		y_2y_3			
		00	01	11	10
y_2y_3	00	1111	Z111	Z11Z	111Z
	01	11Z1	0101	010Z	11ZZ
	11	1ZZ1	0Z01		10Z0
	10	1Z11	ZZ11	Z010	1010

Two stable states

State Transition Table

y_3 SEU faults to 0

		y_0y_1			
		00	01	11	10
y_2y_3	00	1111	Z111	Z11Z	111Z
	01	11Z1	0101	010Z	11ZZ
	11	1ZZ1	0Z01	0000	10Z0
	10	1Z11	ZZ11	Z010	1010

State Transition Table

y_3 SEU faults to 0

		y_0y_1			
		00	01	11	10
y_2y_3	00	1111	Z111	Z11Z	111Z
	01	11Z1	0101	010Z	11ZZ
	11	1ZZ1	0Z01	0000	10Z0
	10	1Z11	ZZ11	Z010	1010

State Transition Table

y_3 SEU faults to 0

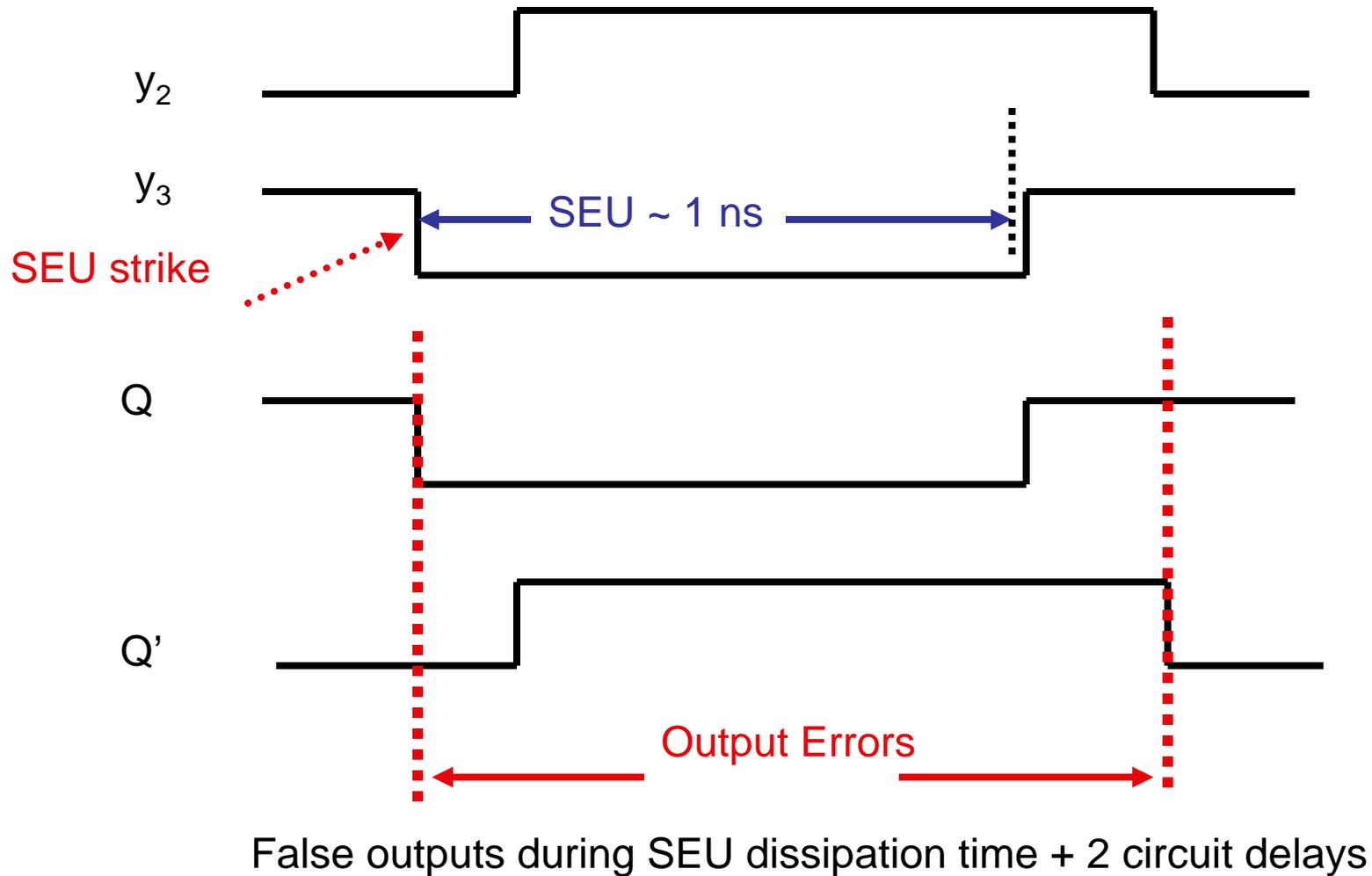
		y_0y_1			
		00	01	11	10
y_2y_3	00	1111	Z111	Z11Z	111Z
	01	11Z1	0101	010Z	11ZZ
	11	1ZZ1	0Z01	0000	10Z0
	10	1Z11	ZZ11	Z010	1010

State Transition Table

y_3 SEU faults to 0

		y_0y_1			
		00	01	11	10
y_2y_3	00	1111	Z111	Z11Z	111Z
	01	11Z1	0101	010Z	11ZZ
	11	1ZZ1	0Z01	0000	10Z0
	10	1Z11	ZZ11	Z010	1010

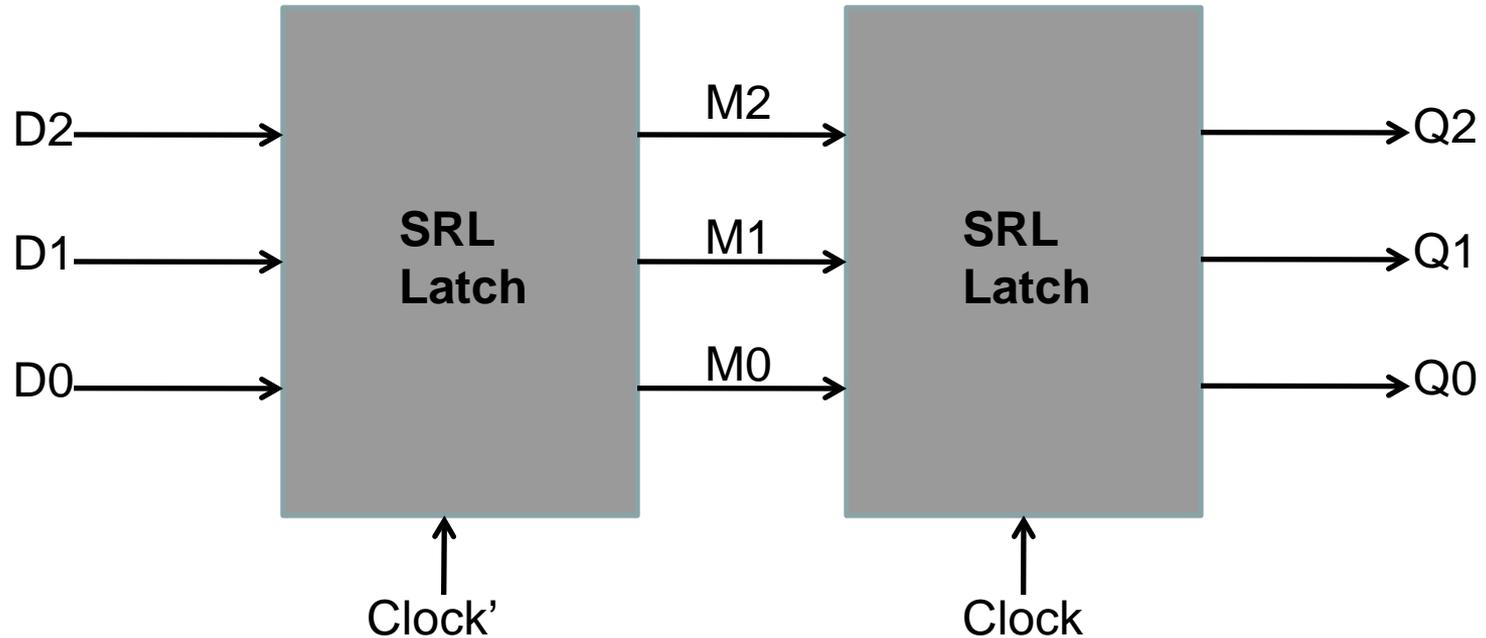
Output Errors During Cell Recovery



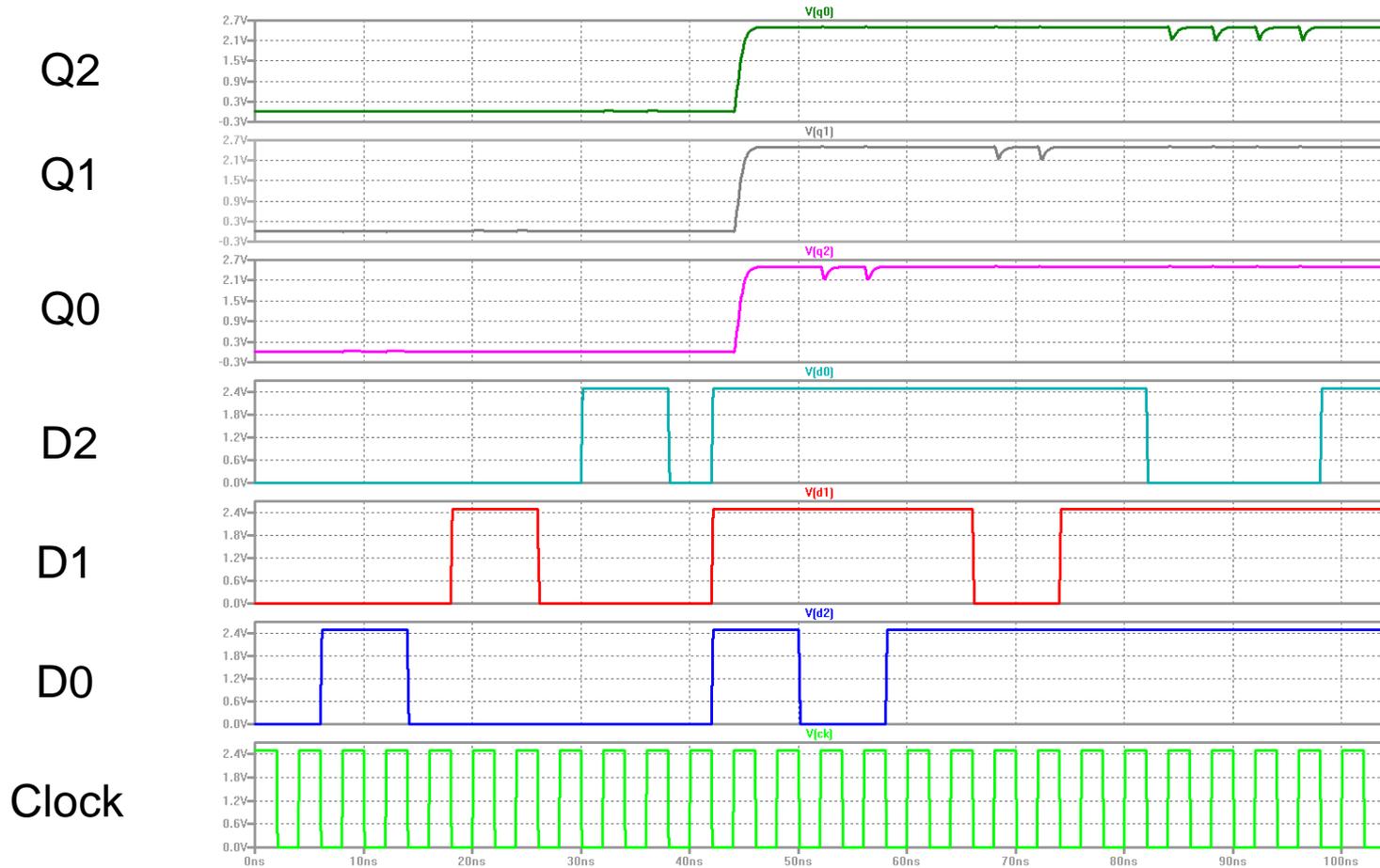
Conclusions on Problem 1 - Speed

- Spacing transistors has no impact
- All legacy RHBD FF designs have this problem
- New solution is required

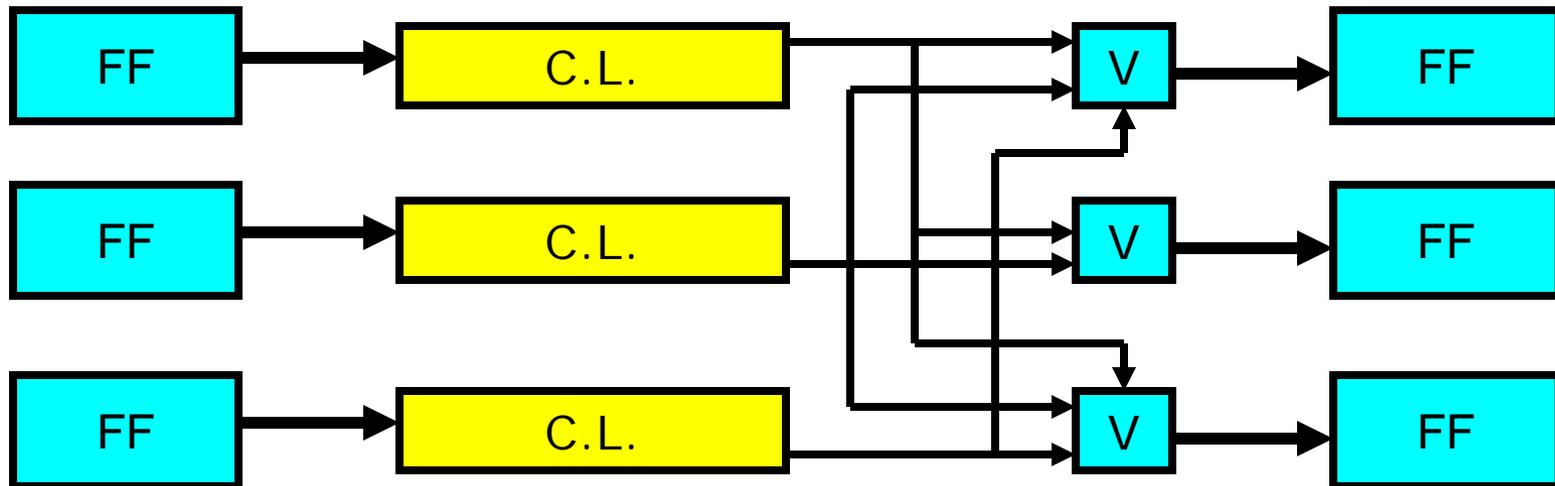
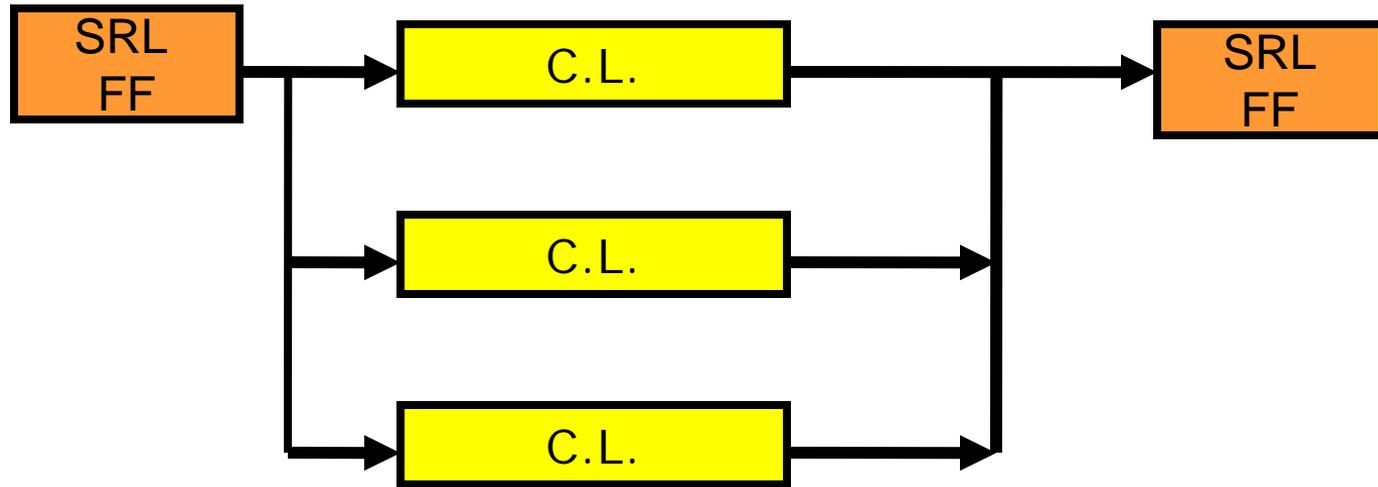
SRL Based Flip Flop



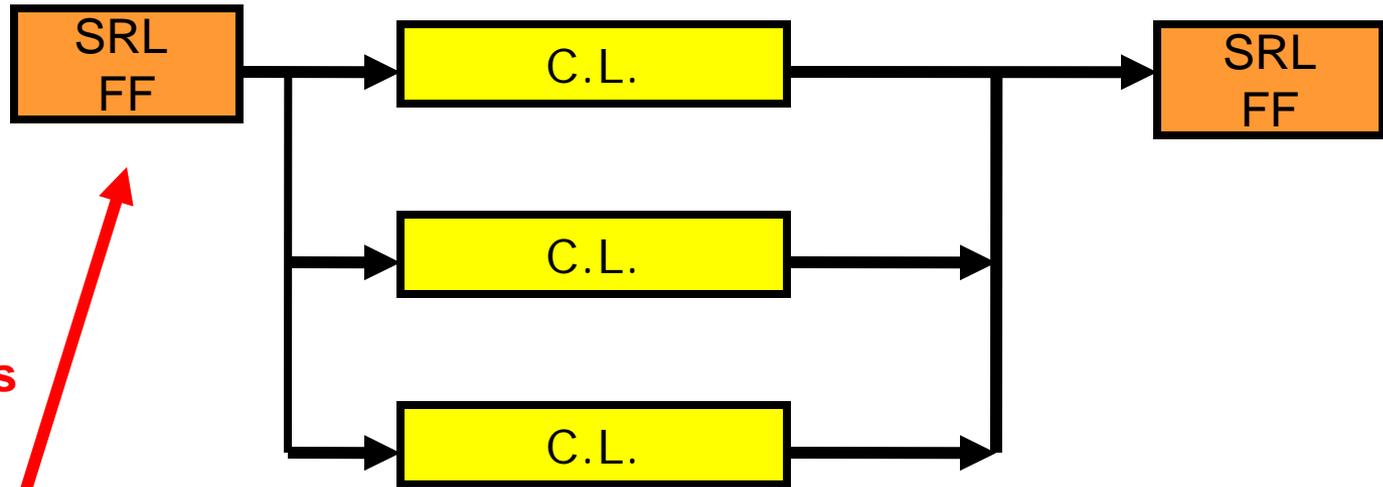
SRL Simulation



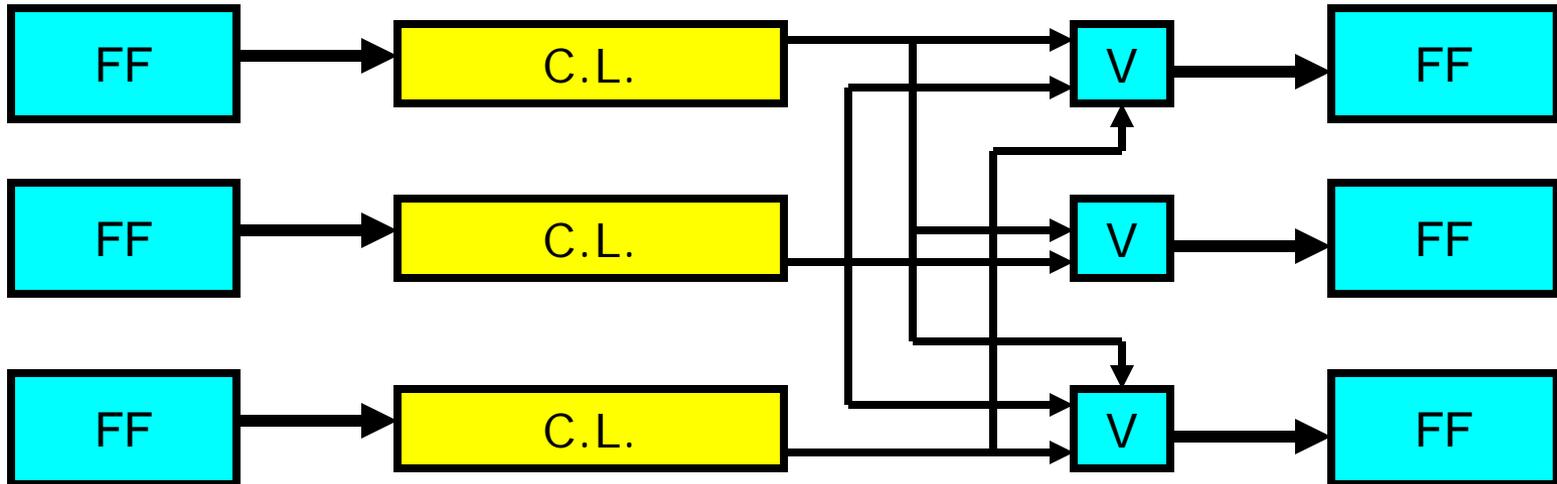
SRL vs TMR Comparison



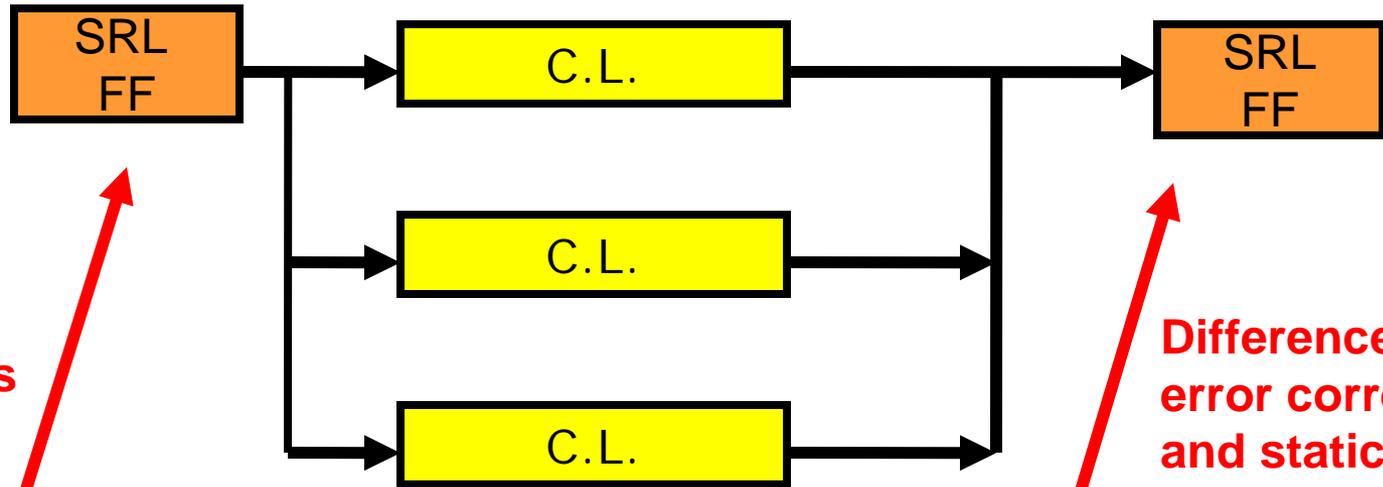
SRL vs TMR Comparison



Difference:
1 FF vs 3 FFs

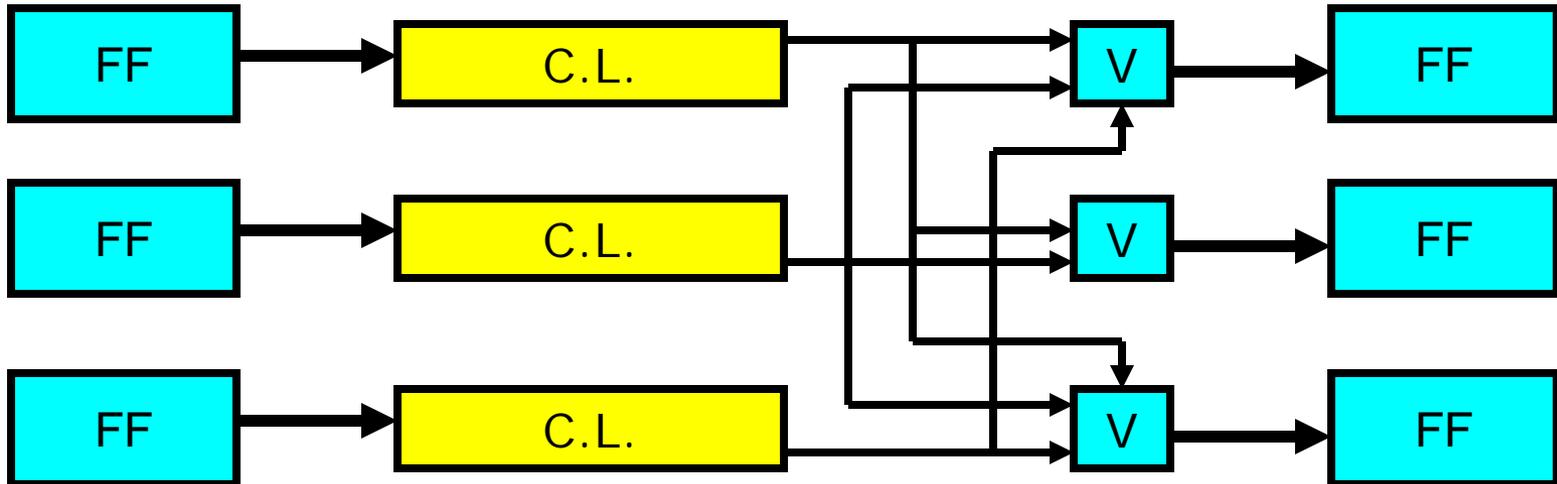


SRL vs TMR Comparison



Difference:
1 FF vs 3 FFs

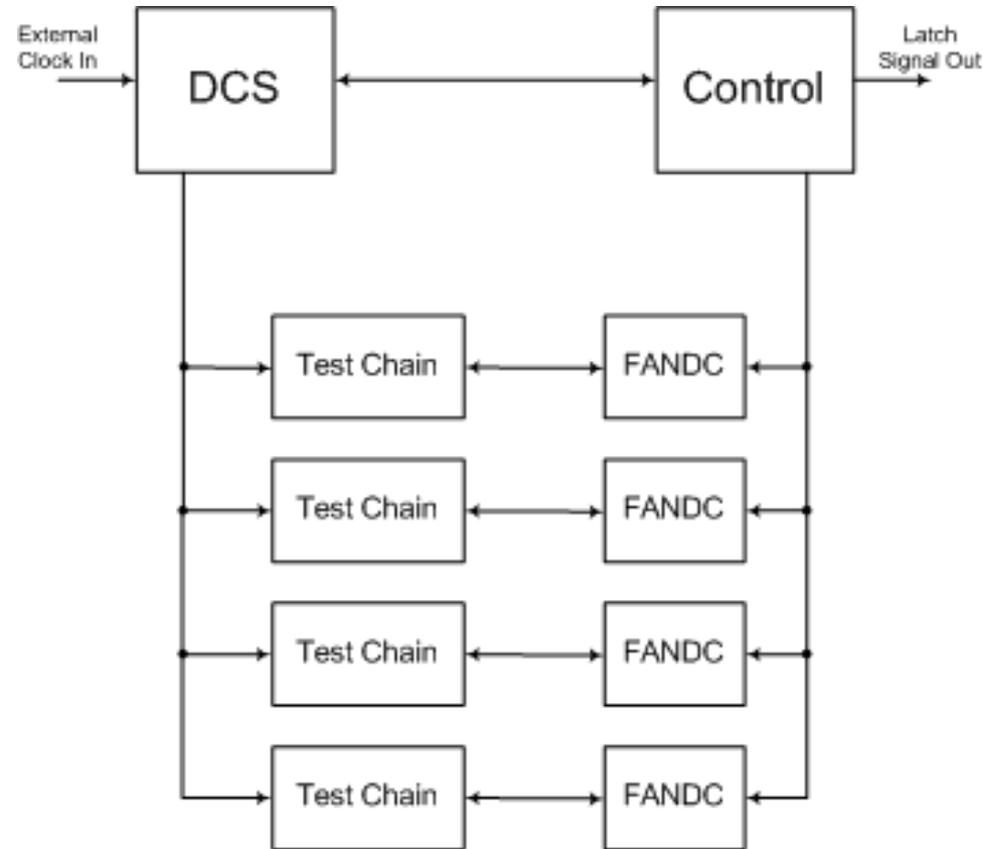
Difference: Voter,
error correction,
and static hold
uniquely merged



Hardware Comparisons

	SRL FF	54	
	TMR – 3 SERT FFs	144	
	TMR – 3 Voters	30	
	Total SERT based TMR	174	
style	TMR FF DICE cell [3 x 32]	96	transistors
	TMR Voter	30	
	Total DICE based TMR	126	
	Total non-RT FF [3 x 14]	42	
	TMR voter	30	
	Total non-RT	72	

90nm Bulk CMOS Test Chip Architecture for TAMU Tests

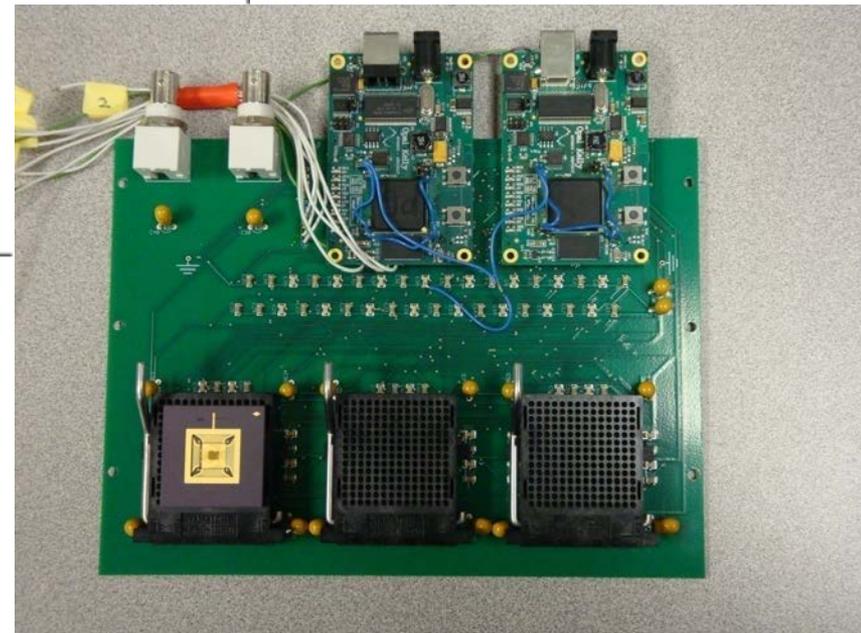
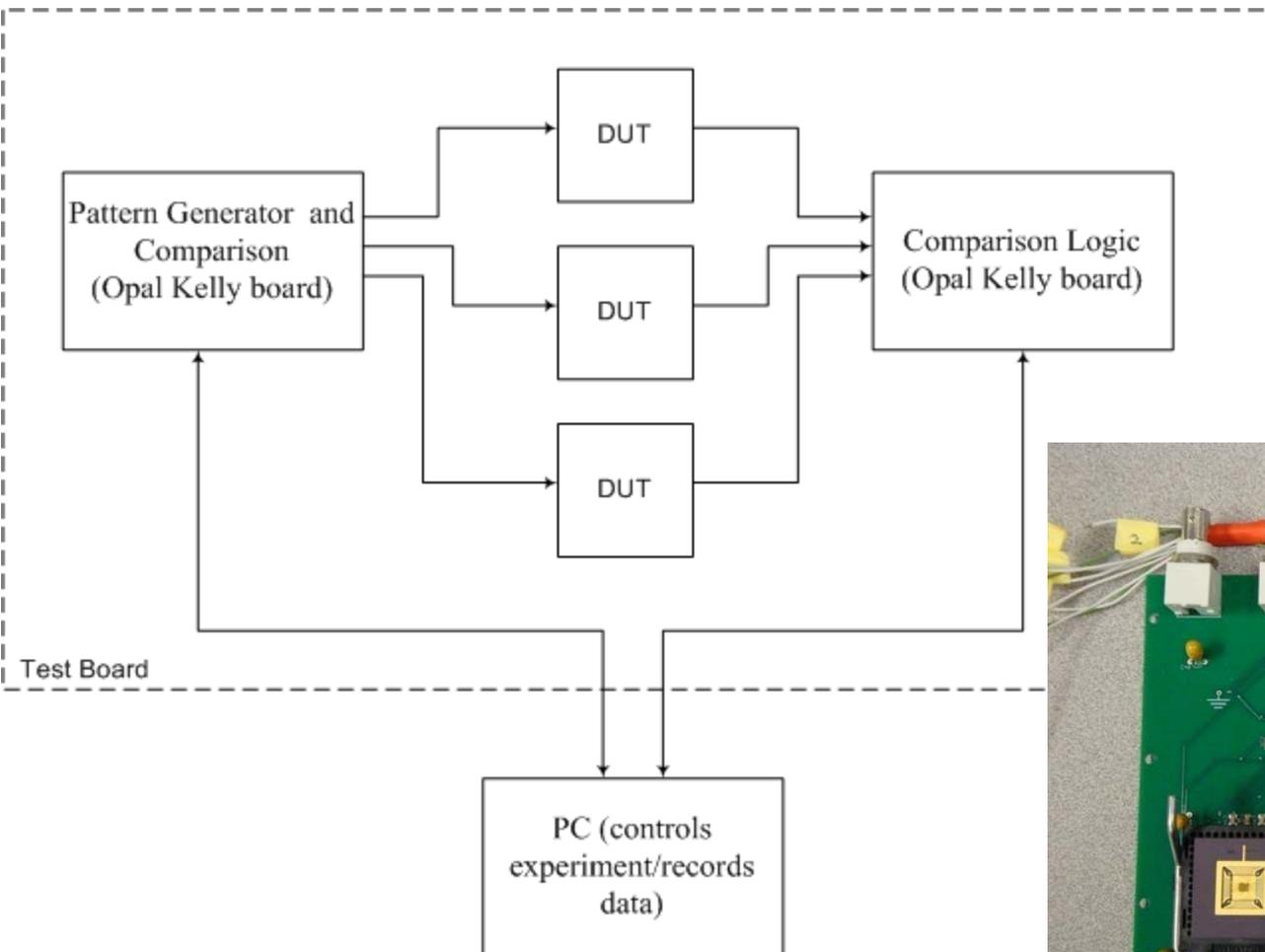


- DCS – Digital Clock Synthesis
- Control – Generated periodic block reset and external latch signals
- FANDC – Feed and Check block responsible for feeding simple pattern into test chains and verifying matching output
- DCS, Control and FANDC blocks were designed using extreme RHBD methods
- Test Chains varied from simple flip-flop to triple rail SCL logic

Test Chains

- Sixteen functional chains
- Memory elements included different versions of SERT and SRL cells with varying spacing between sensitive nodes
- Some chains included logic trees for characterizing SETs
- Some chains dedicated to determining rad-hard-by-sizing constraints
- One chain was dedicated to FANDC block only

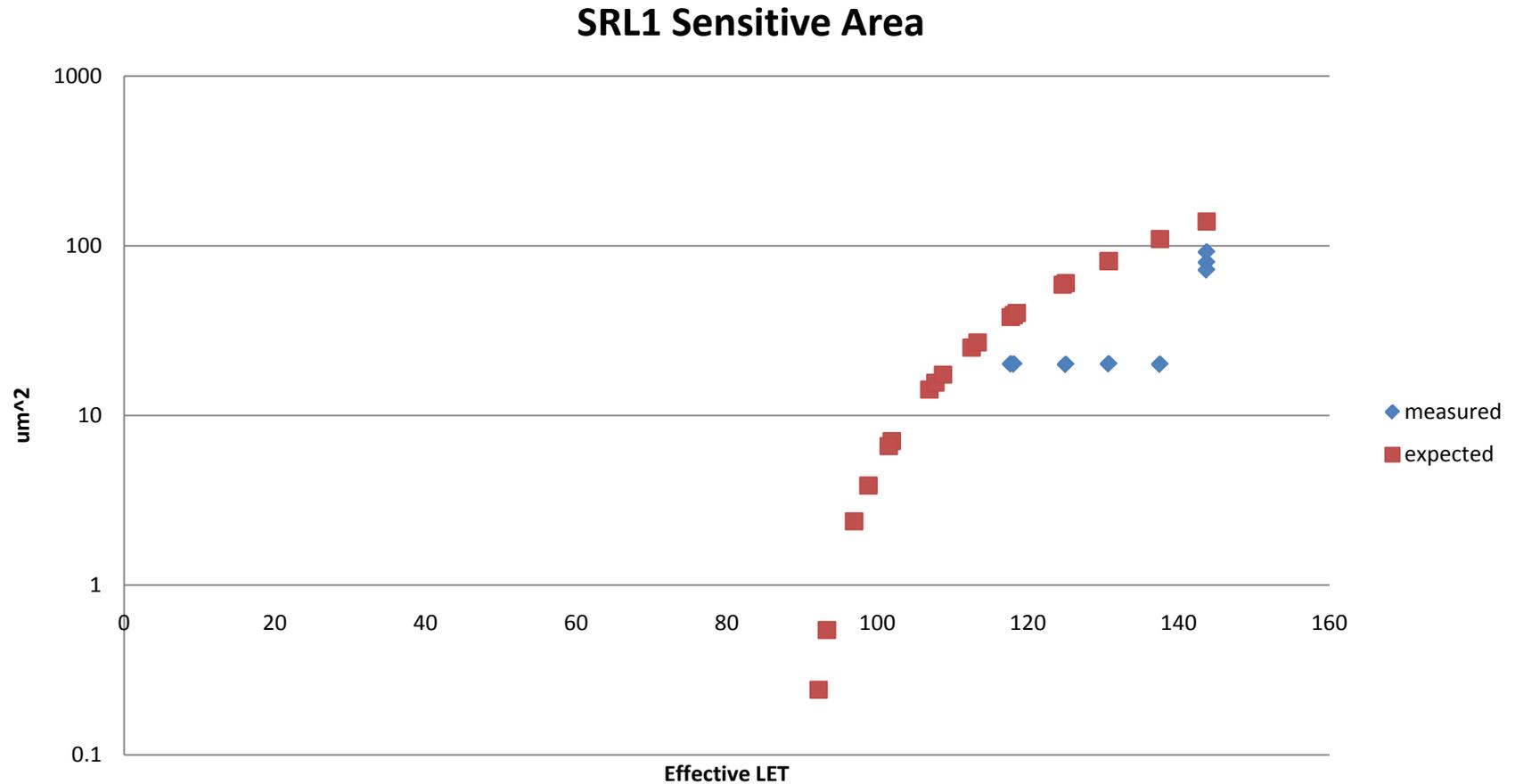
Test Board Architecture



Test Conditions at TAMU

- Parts were left at room temperature
- Clock rate was set to 160Mhz
- Voltages were set at nominal 1.2V core and 2.5V I/O
- Various beam types from krypton to gold were used
- Various angles from 0 to 52 degrees were used.
Two trips to TAMU to collect a complete set of data points.
- Shallow angle beams aligned for east-west track propagation

TAMU SEU Results for SRL FF



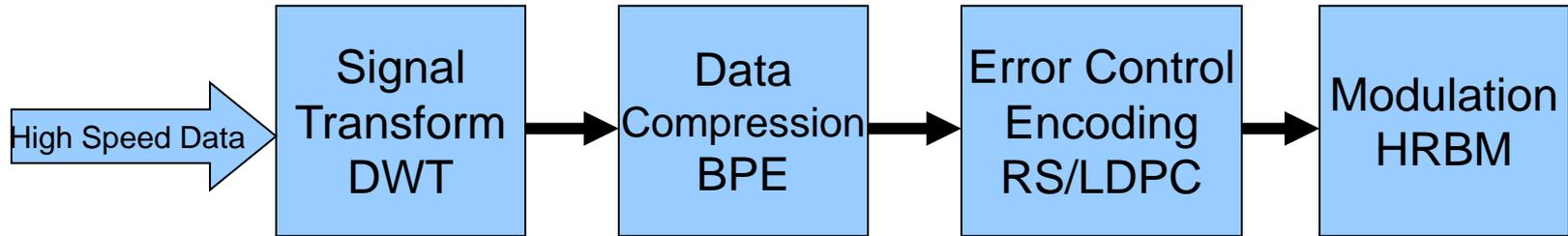
Conclusions on Main Issues

- Problem 1 – Speed versus upset duration
 - Solved with SRL electronics
- Problem 2 – Low SEU LET
 - Preliminary results of SRL show promise

Next Steps

- Design robust test chip
 - Compare with existing legacy devices
 - Determine maximum speed for on set SEU
- Create micro synthesis library
- Create macro synthesis library
- Communications SoC
- SRL design tool
- Macro cell design tool

0.25 μ m SERT Based Signal Processing



Function	Transistors	Speed	Data Rate
DWT	5 Million	100 MHz	320 Mb/s
BPE	8 Million	20 MHz	480 Mb/s
RS/LDPC	500 K	67 MHz	1 Gb/s
HRBM	2 Million	100 MHz	480 Mb/s

DWT + BPE
Compression
Board



LDPC + Modulator
Channel Processing
Board



Development Team Members

- Glenn Research Center
 - Communications Systems
- Goddard Space Flight Center
 - Communication, payload, instrument systems
- Applied Physics Lab
 - Radiation Test, macro cell design
- ICs
 - SRL library, macro cell design, CAD tools

Thank You

- Contact Information
 - ics [@ics-rhbd.com](mailto:ics@ics-rhbd.com)
 - Phone (208) 315-0029