BOEING

Engineering, Operations & Technology
Boeing Research & Technology

90nm RHBD ASIC Design Capability

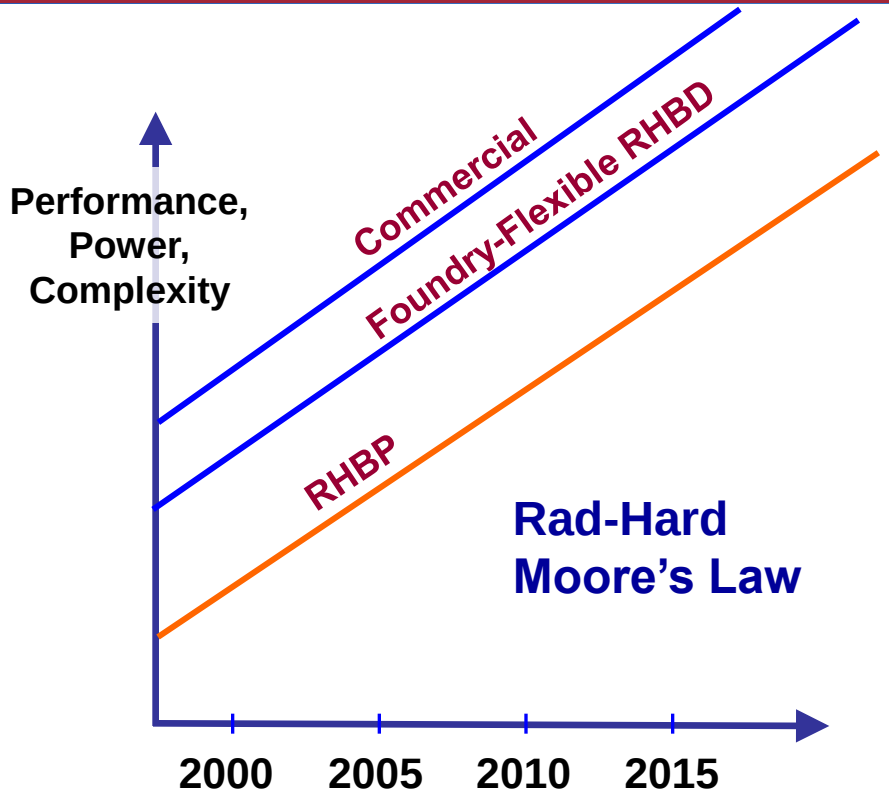
ReSpace/MAPLD 2011

Tony Amort, Warren Snapp, John Evans, Jeremy Popp, Manuel Cabanas-Holmen, Ethan Cannon

This work was sponsored in part by the Defense Threat Reduction Agency under contract #: HDTRA1-05-D-0001-0002. Opinions, interpretations, conclusions, and recommendations are those of the author and are not necessarily endorsed by the United States Government.

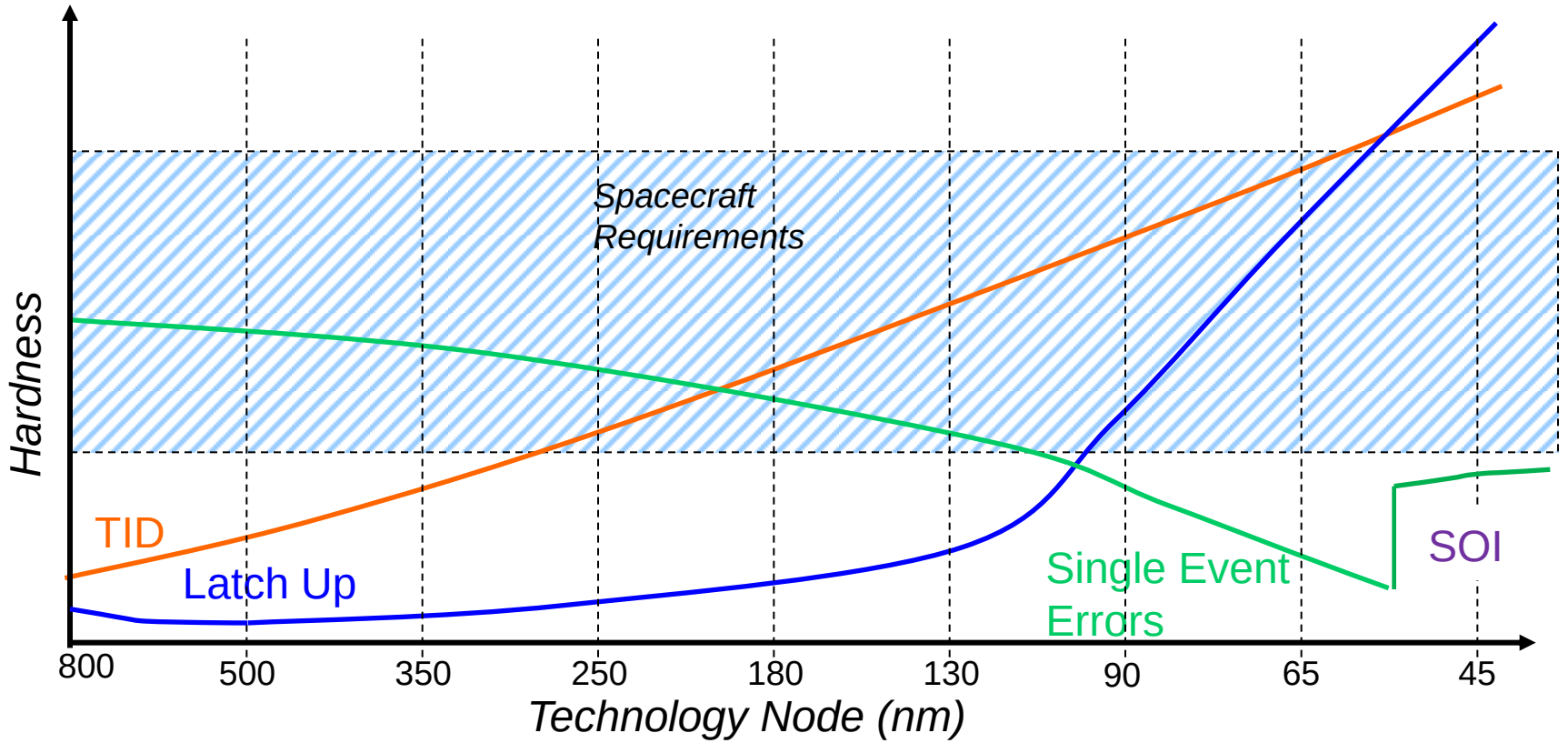
Motivation for RHBD on Commercial

- State-of-the-art performance
- Continuity of foundry access
- Leveraging the investment of commercial foundries including IP, EDA, QC



RHBD with leading-edge commercial device technologies provides a sustainable option which ensures the supply of radiation-hardened components for future space systems.

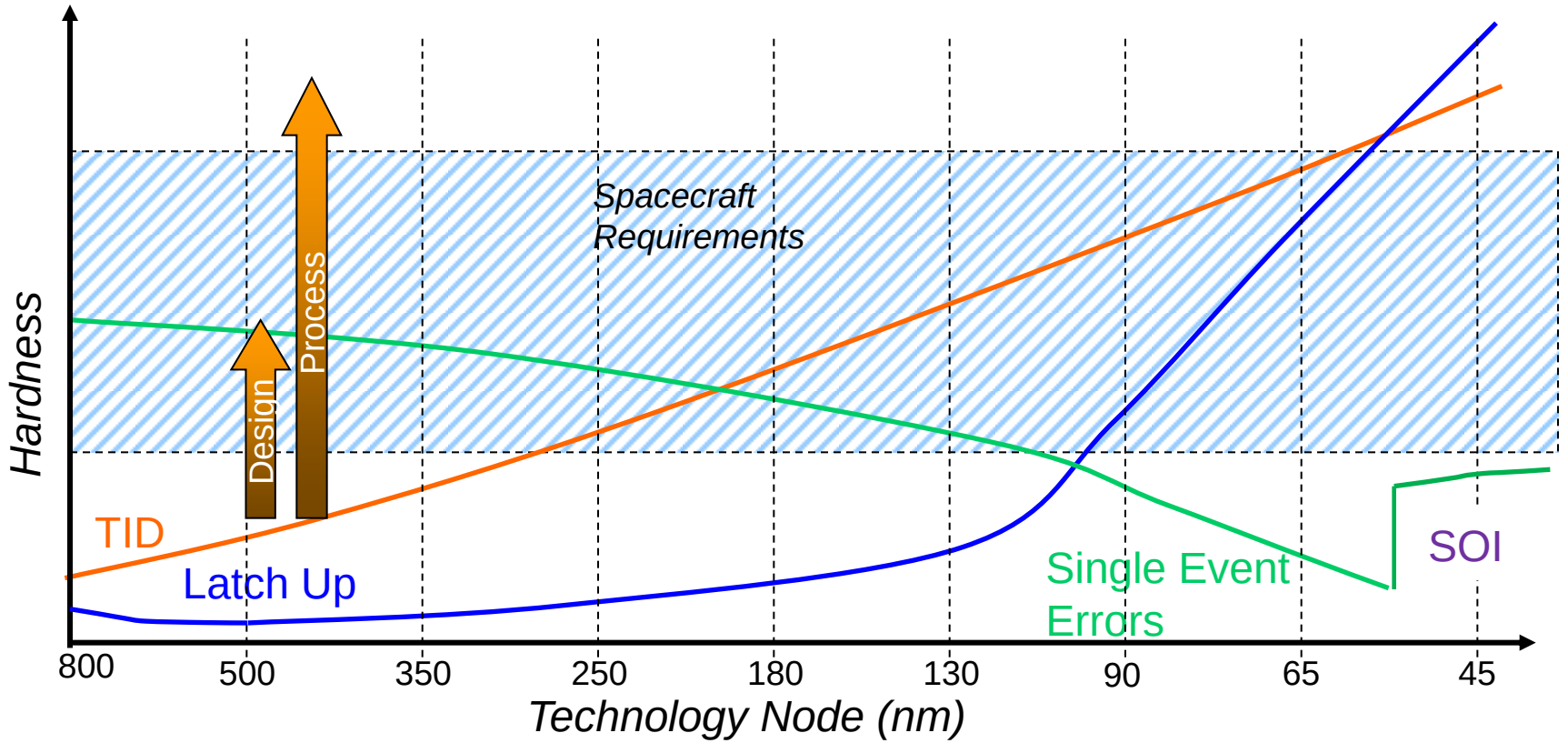
Commercial CMOS Hardness Trends



Commercial process improvements reduce need for TID or Latchup Mitigations

Design methods to mitigate Single Event Errors are increasingly important

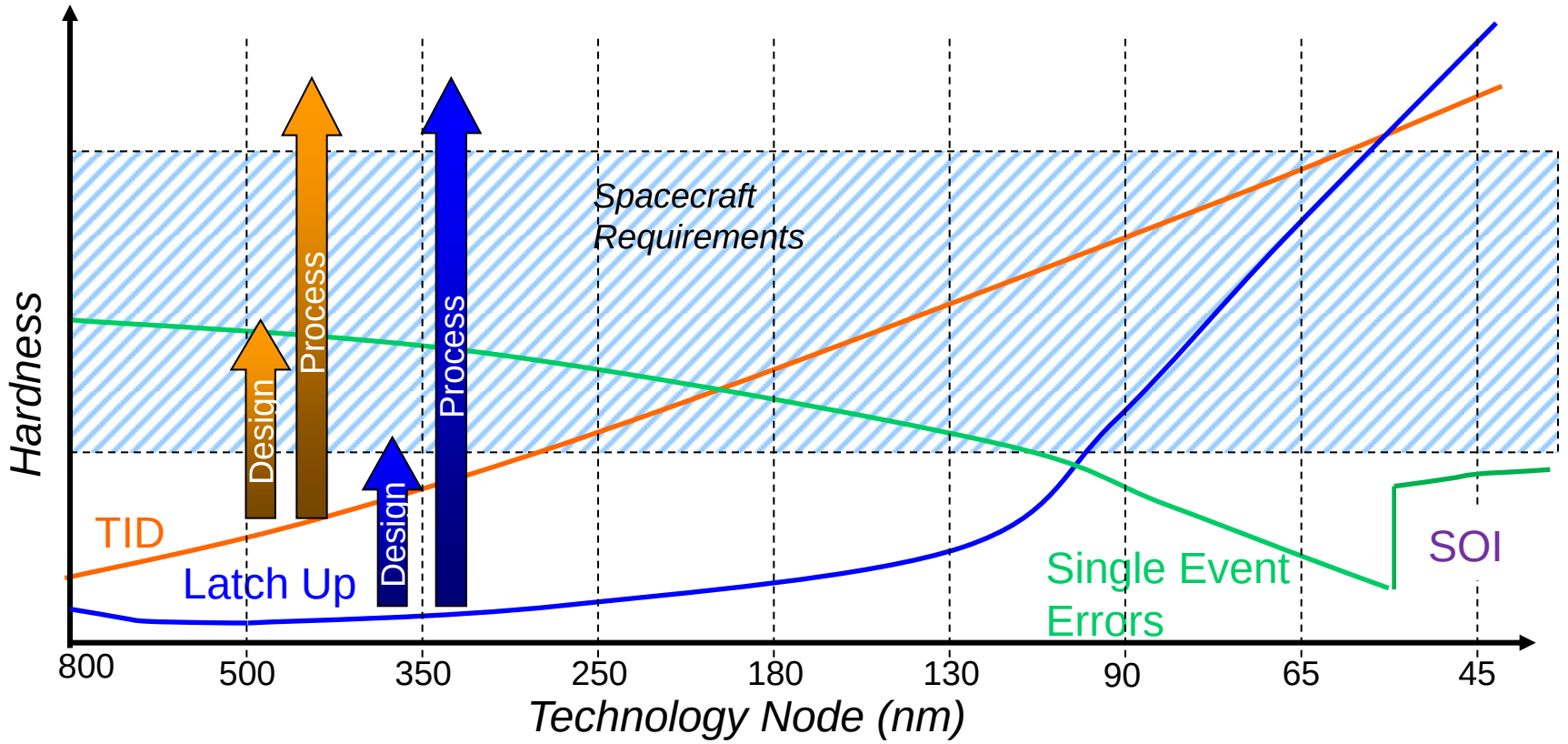
Commercial CMOS Hardness Trends



Commercial process improvements reduce need for TID or Latchup Mitigations

Design methods to mitigate Single Event Errors are increasingly important

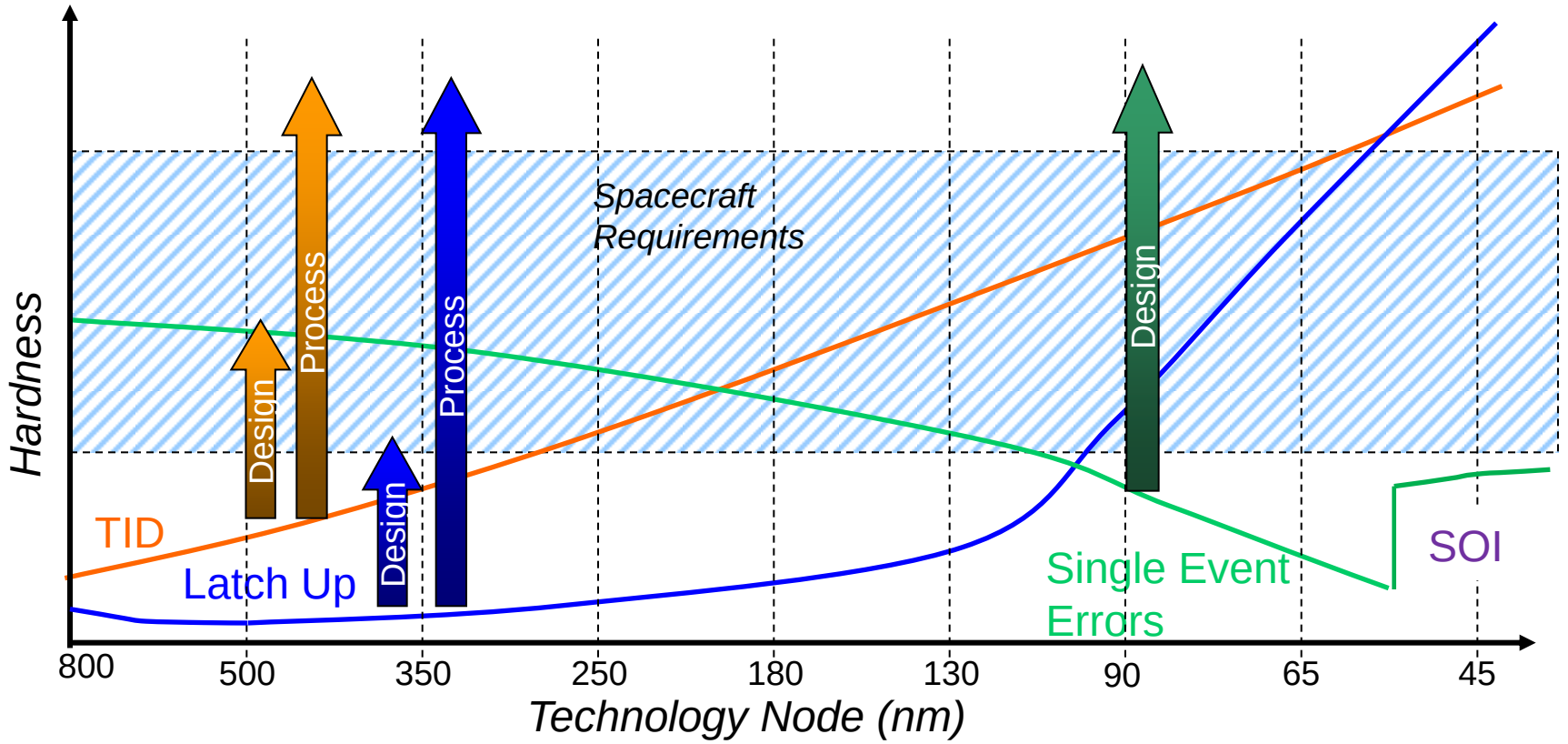
Commercial CMOS Hardness Trends



Commercial process improvements reduce need for TID or Latchup Mitigations

Design methods to mitigate Single Event Errors are increasingly important

Commercial CMOS Hardness Trends



Commercial process improvements reduce need for TID or Latchup Mitigations

Design methods to mitigate Single Event Errors are increasingly important

High Performance Communication Satellite DSPs Require Advanced ASICs

Parameter	ICO	Thuraya	Spaceway	Today's Capability
ASIC Technology	0.7µm RHBP	0.25µm Commercial	0.18µm Commercial	90nm RHBD
Number of ASICs	2300	360	390	76
Performance (TOPS)	3.6	14	62	105
Mass (Kg)	270	190	124	90
Power (W)	2200	2300	2100	1575

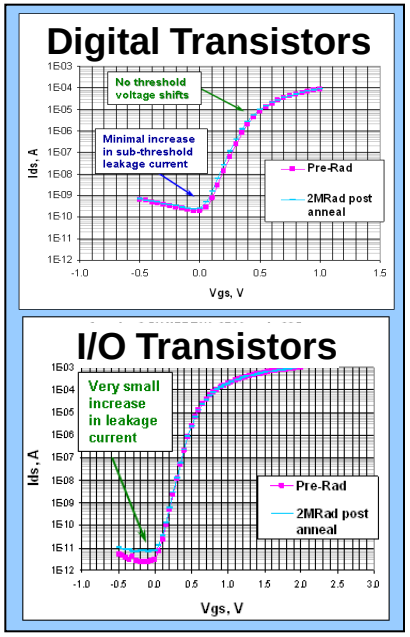
Next Gen 45nm SOI RHBD

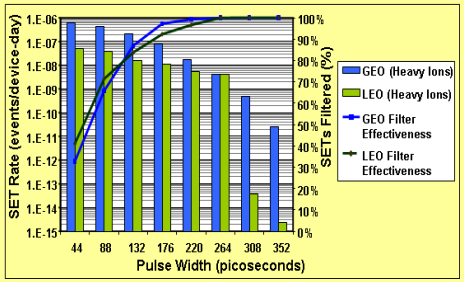
RHBP RHBA RHBD

Switchover to commercial ASIC technologies enabled major advances in functionality and performance

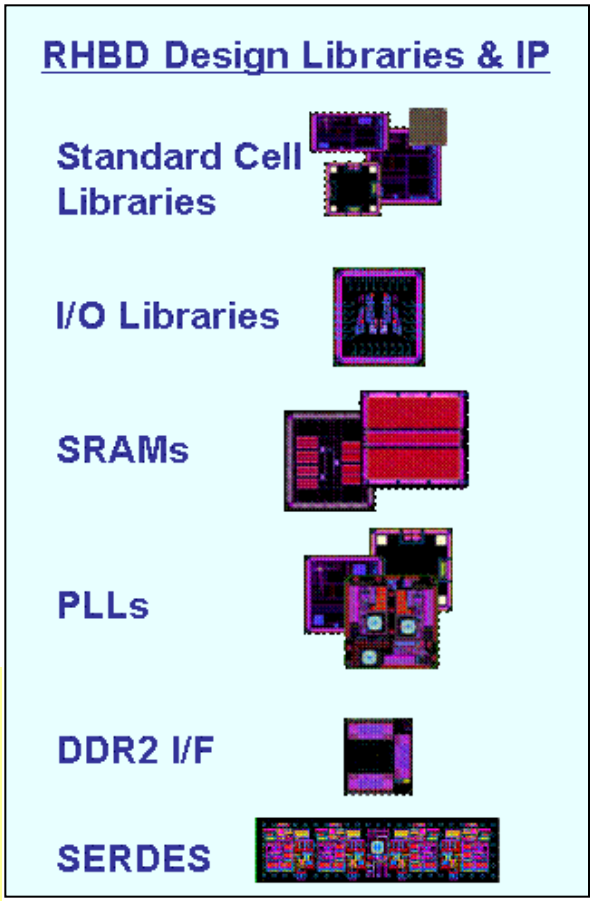
RHBD90 Development

Technology Characterization





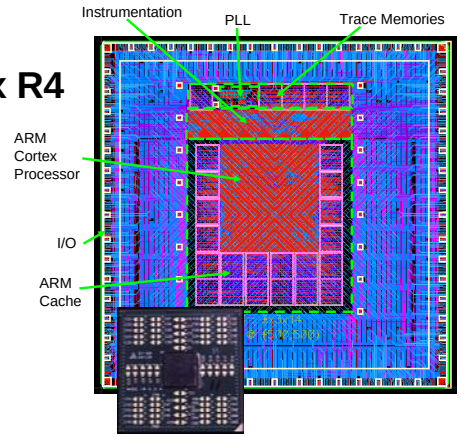
Design Enablement



Demonstrations

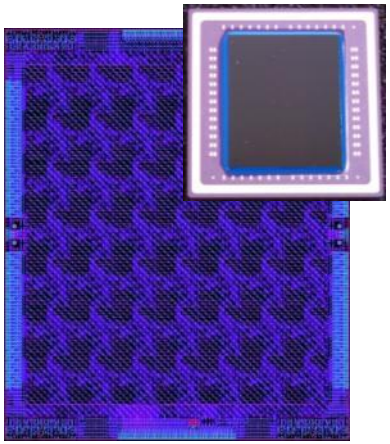
RH Cortex

- ARM Cortex R4
- 22 million transistors
- 430 MHz



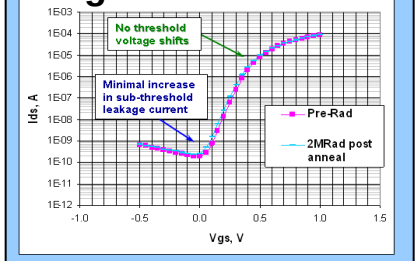
MAESTRO

- 49 core processor
- 10 Gbps SERDES
- 750 million transistors
- 7,000 C4 Bumps

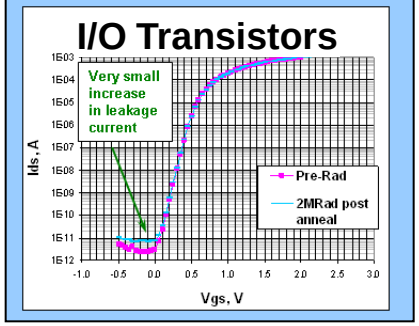


RHBD with Commercial 90nm CMOS TID Response

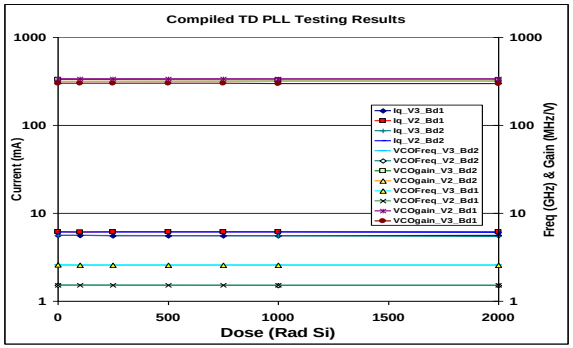
Digital Transistors



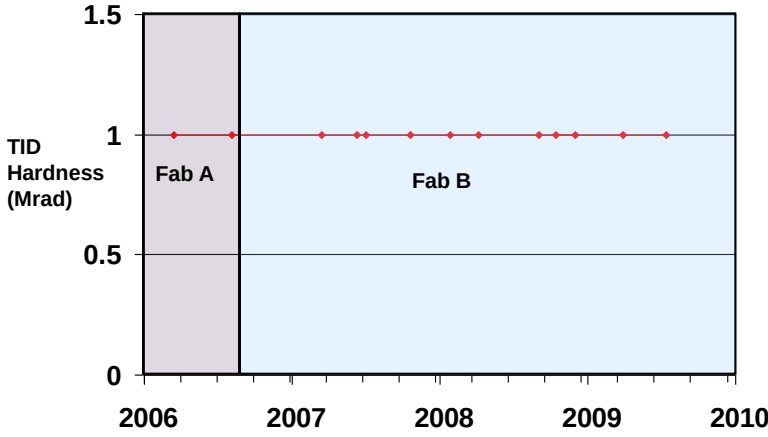
I/O Transistors



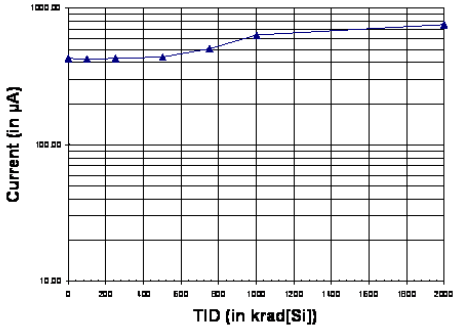
Phase-Locked Loop



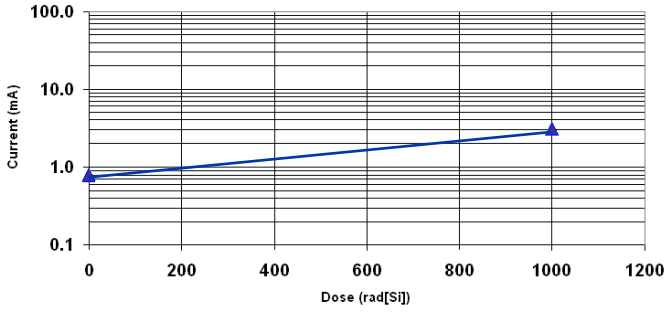
TID Lot-to-Lot



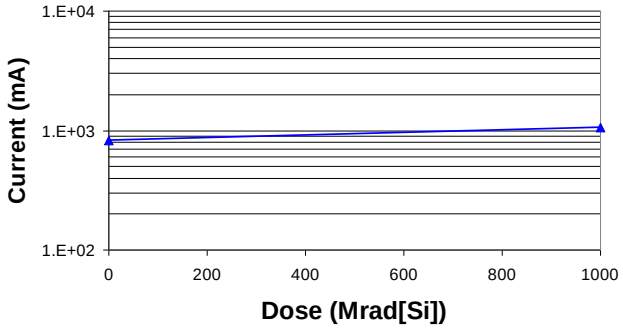
Logic Block



SRAM



RH Cortex Processor



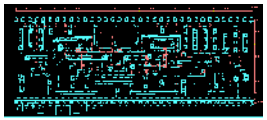
TID Hardness Demonstrated at Device, Circuit and SoC Levels

RHBD with Commercial 90nm CMOS
Single-Event Effects – Flip-Flop Upsets

Flip-Flop Options

FF Type	SEU Rate (errors/bit-day)	Area	Speed	Power
Soft	10^{-6}	1X	1X	1X
DICE	$6x10^{-9}$	2X	1.5X	2X
TMR	10^{-12} (depends on spacing)	4X	1X	4X

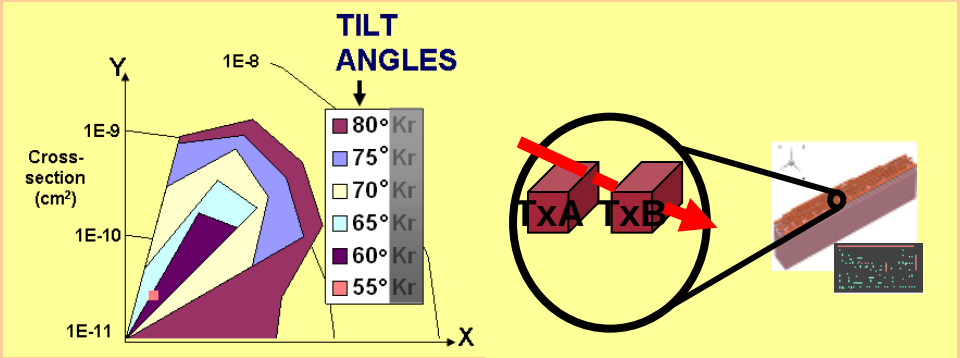
Soft FF (8.4µm x 3.36µm)



DICE FF (15.4µm x 3.36µm)

Cross-section depends on incident angle

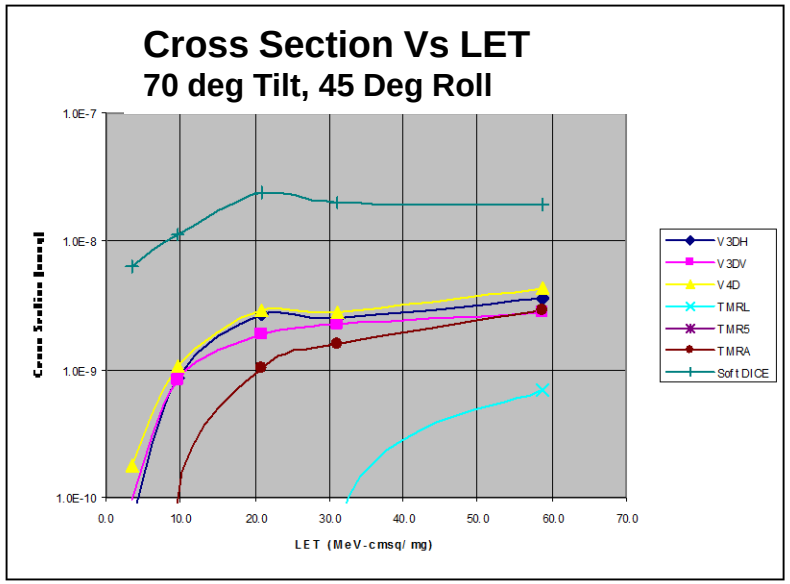
New Analysis Methods Developed

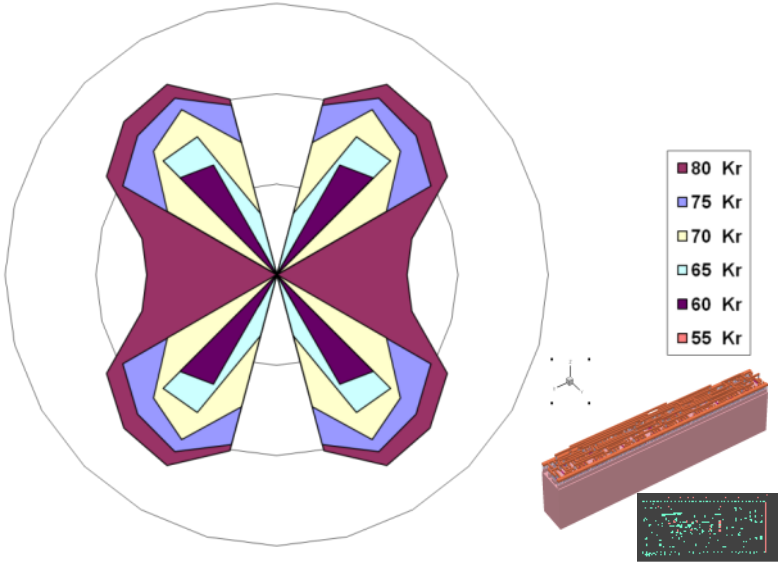


- **Classical methods of SEU rate analysis are not applicable to redundant designs**
- **Pursued three analysis paths:**
  - **Boeing FastGT**
  - **VU/ISDE MRED**
  - **Robust Chip Monte-Carlo/Accuro**
- **Good agreement among all 3 analysis methods**

SEU can be Mitigated Effectively

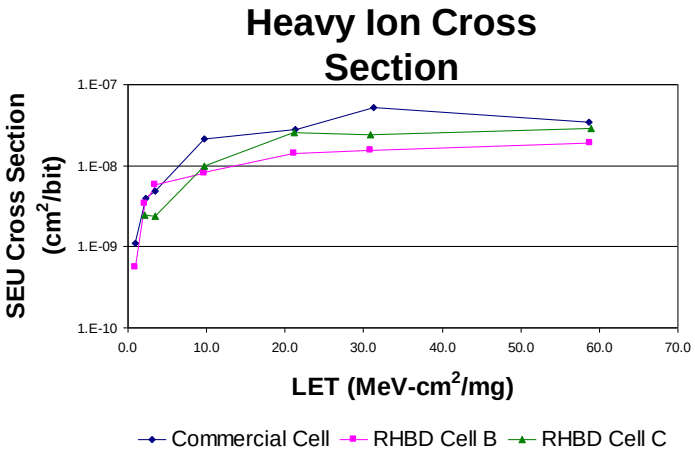
Flip-Flop SEU Analysis

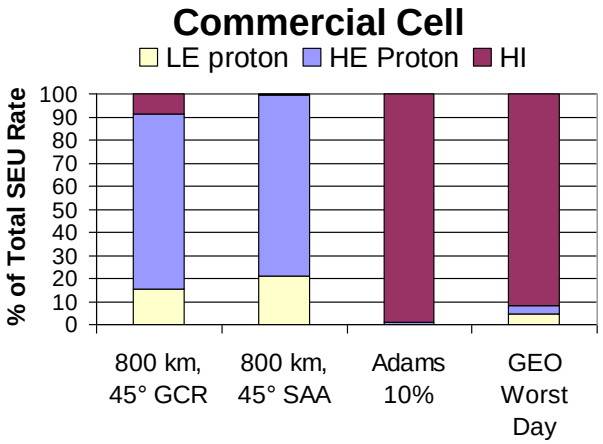




- **Classical methods of SEU rate analysis (such as CREME96) are not applicable to redundant designs**
  - **Use single sensitive volume**
  - **Neglects geometric effects**
- **Angular effects must be accounted for**
  - **DICE is SEU Immune for ions with inclination at or less than 60 degrees**
  - **Soft DICE SEU Rate > 1000 times greater than DICE**

RHBD with Commercial 90nm CMOS
Single-Event Effects – SRAM Upsets





SEU Rate Components by Environment

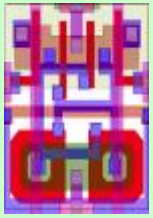
RHBD techniques include

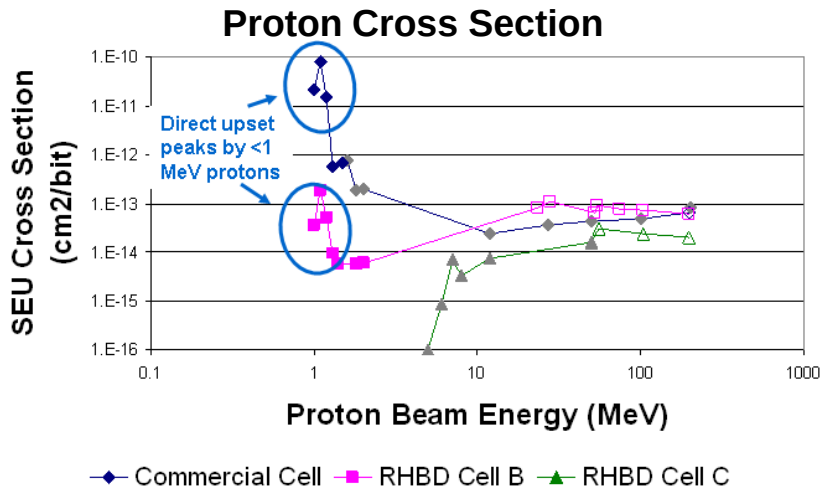
- Bit spacing
- Scrubbing
- Error detection
- Bit cell design
- Peripheral ckt design

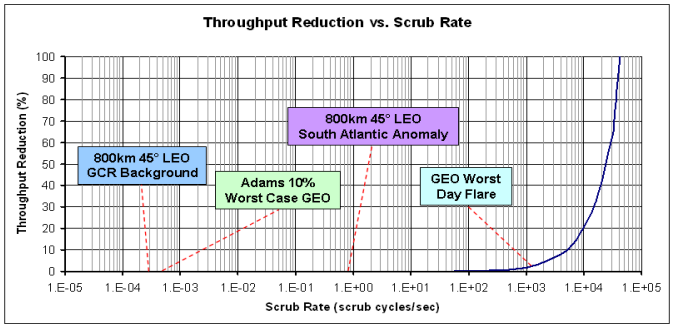
Commercial Cell

RHBD Cell B

RHBD Cell C





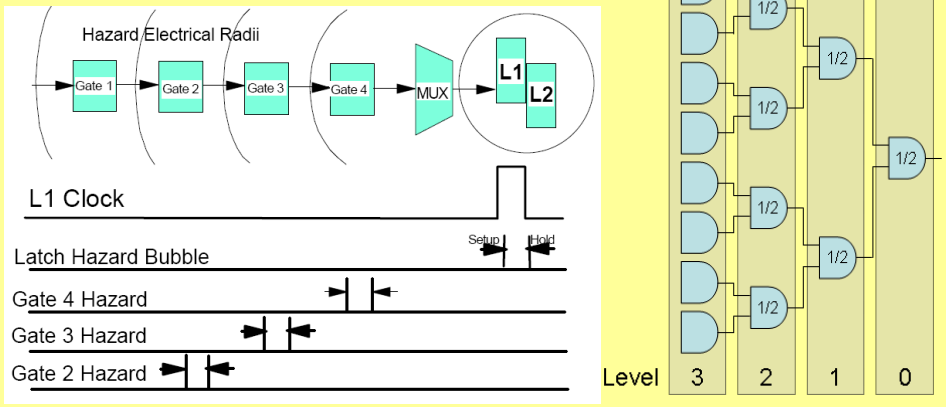


Negligible Impact on Processor Performance

SEU Mitigated for Heavy Ions, High and Low Energy Protons

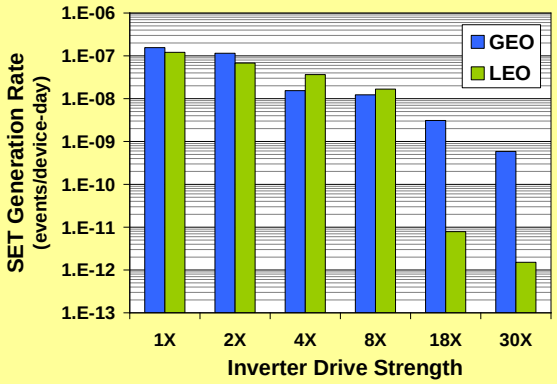
RHBD with Commercial 90nm CMOS
Single-Event Effects—Transients

- System-level error rate methodology includes temporal and logical masking
  - Characterized pulse spectra vs. LET
  - Determined SET generation rate for multiple environments



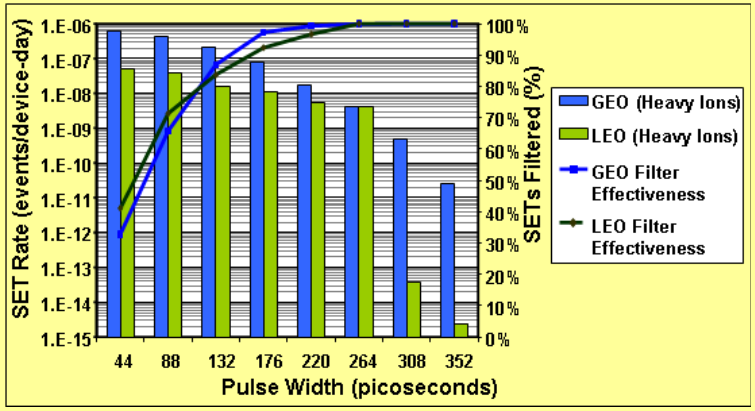
SETs leading to errors depend on timing and logical masking

Buffer sizing for clock/reset trees



RHBD Library includes temporal filter elements

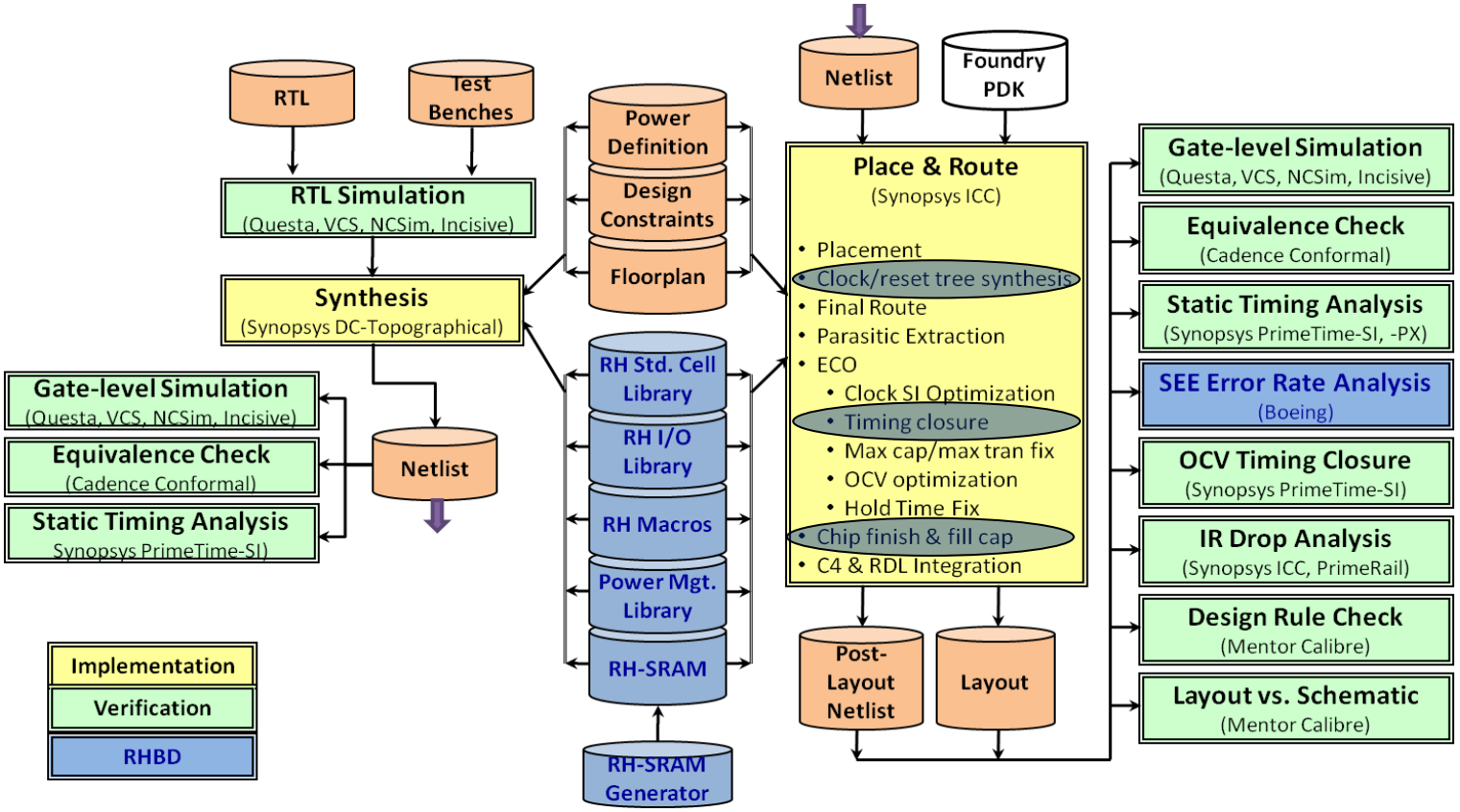
Temporal filter reduces error rate



Variety of mitigation techniques allows design trades

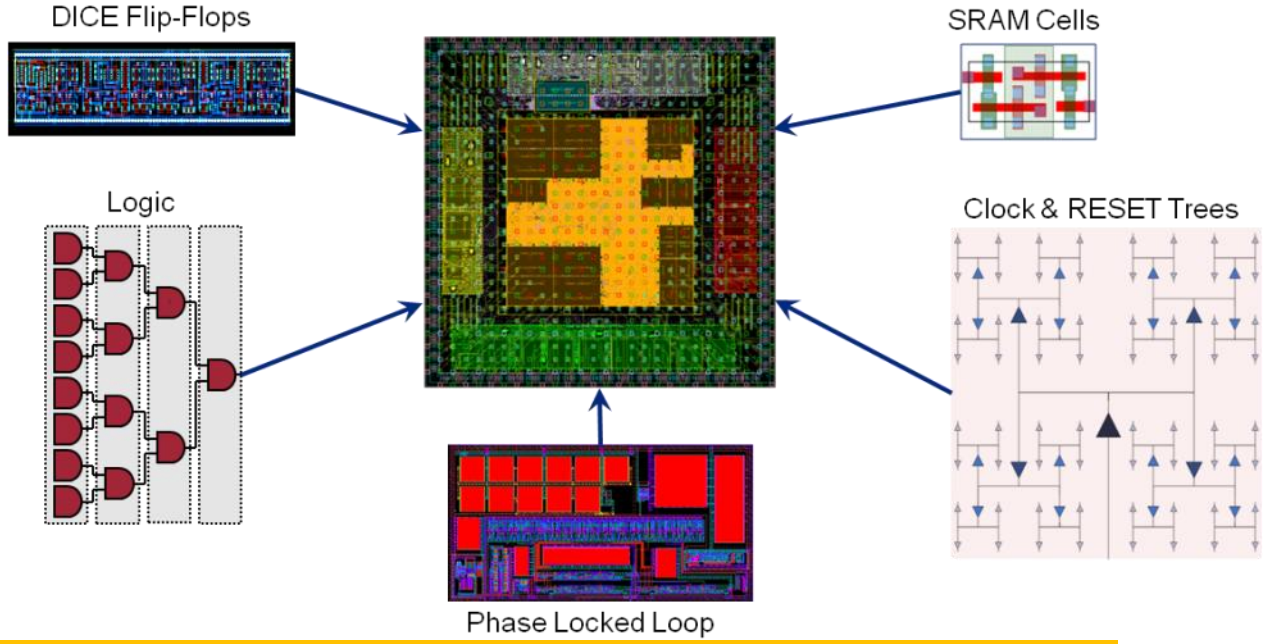
RHBD Design Flow

- **Proven design flow based on Synopsys Recommended Methodology (RM) flow**
- **Radiation effects mitigation and analysis added**



SEE Analysis Overview

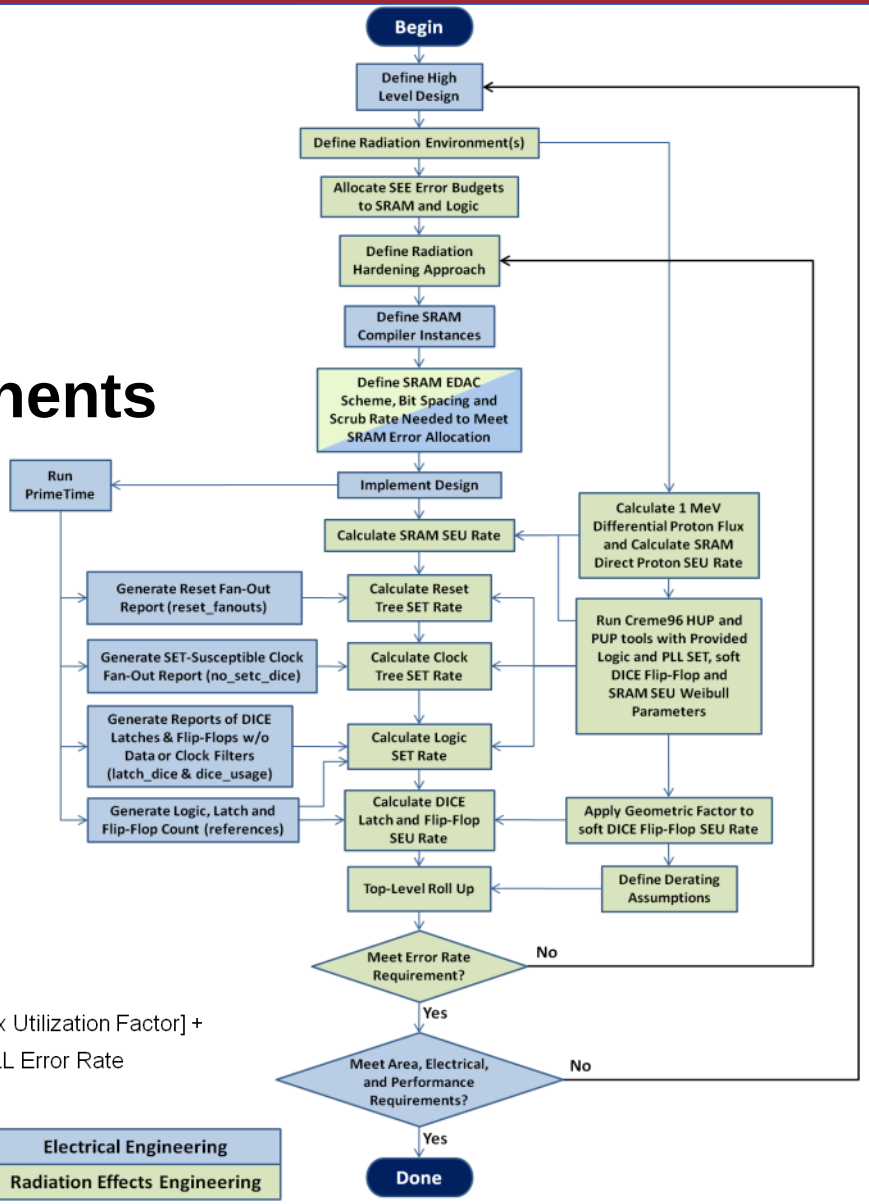
- **Single-Event Effects drive radiation performance in sub-100nm technology**
- **System effects differ on different circuits and environments**
- **To solve this complex problem we developed an algorithm and methodology to quantify system effects**



SEE analysis in design loop allows performance vs. error-rate tradeoff

SEE Analysis Flow

- **Inputs from**
  - **Radiation environment**
  - **System error budget**
  - **Design timing reports**
- **Calculate error-rate components**
  - **SRAM**
  - **Clock/Reset trees**
  - **SET**
  - **Flip-flop/latch SEU**
- **Combine with derating for top-level error rate**



Single Event Error Rate =

(SET $rate_{RESET}$ x RESET SET Derating x Utilization Factor) +

(SET $rate_{CLOCK}$ x Clock SET Derating x Utilization Factor) +

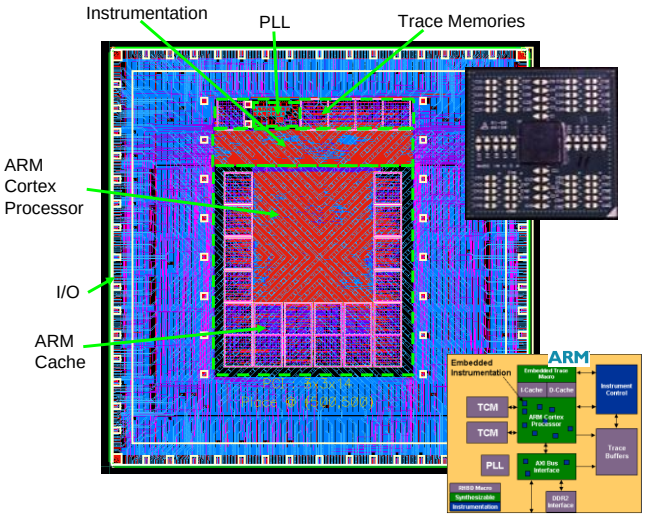
[(SEU $rate_{Flip\text{-}Flop}$ + SET $rate_{Flip\text{-}Flop}$) x $ProbDataBits_{Flip\text{-}Flop}$ x Flip-Flop System Derating x Utilization Factor] +

(SEU $rate_{SRAM}$ x $ProbDataBits_{SRAM}$ x SRAM System Derating x Utilization Factor) + PLL Error Rate

RHBD90 Demonstrations

RH Cortex

- ARM Cortex R4
- 22 M Transistors
- 430 MHz
- Demonstrated
  - Hardening commercial IP
  - Integration of RHBD library with commercial EDA tool flow
  - Successful operation to specified performance
  - System error rate prediction



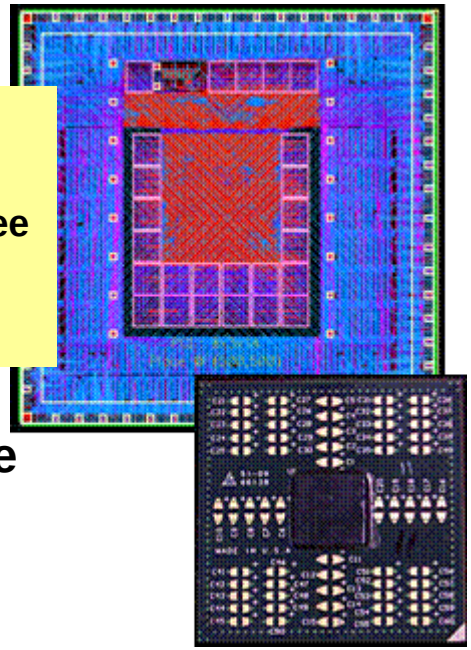
MAESTRO

- 49 core general-purpose processor
- 10 Gbps SERDES
- 750 million transistors
- 7,000 C4 Bumps
- Demonstrated
  - Design flow supports large, complex chips

RH-ARM Cortex R4

- **Industry-Leading Processor for Embedded Control & Sensor Applications**
- **Optimized for High-Performance, Real-Time operation**
  - **370 MHz @ 1.0V**
  - **1,065K Drystones**
- **Integrated Floating Point Processor**
- **Fault-Tolerance Support**
- **Extensive Software Development & Debug Infrastructure**

- **TID Hard to 1MRad**
- **SEU Hardened**
  - **Clock and reset tree hardening**
  - **FF & SRAM hardening**



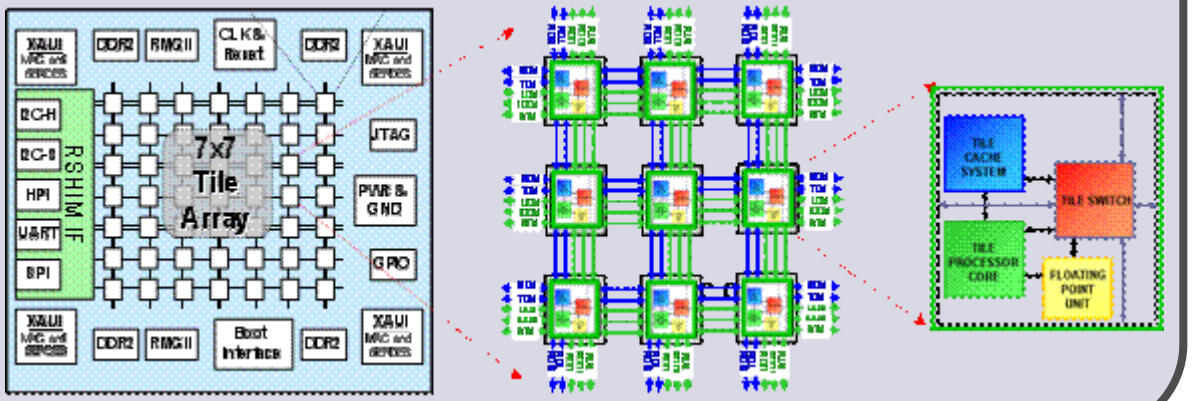
- **Successfully demonstrated:**
  - **Performance, power, and area RHBD metrics**
  - **Performance-optimized RH memory**
  - **Transient hardening of clock and reset trees**
  - **Radiation hardening of commercial IP**
  - **Error rate prediction analysis**
  - **Flip-chip Packaging**

Cortex Applications

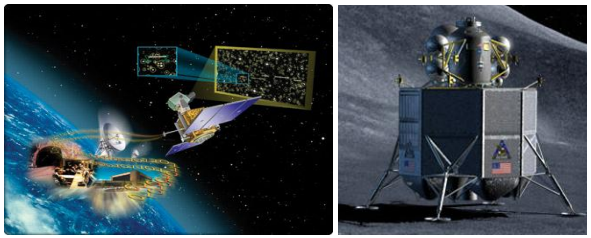
- ***Medical***
- ***Digital Imaging***
- ***Storage***
- ***Microcontrollers***

MAESTRO RH Multi-Core Processor

- **RHBD version of the Tilera 26480 processor:**
- **300MHz, 44 GOPS, 22 GFLOPS**
- **2D mesh of 49 cores with low latency networks**
- **Each core a general purpose processor with FPU**
- **High speed external serial interfaces (XAUI)**
- **DDR1 or 2**
- **18W, 500 kRad TID**
- **Software development environment in place**



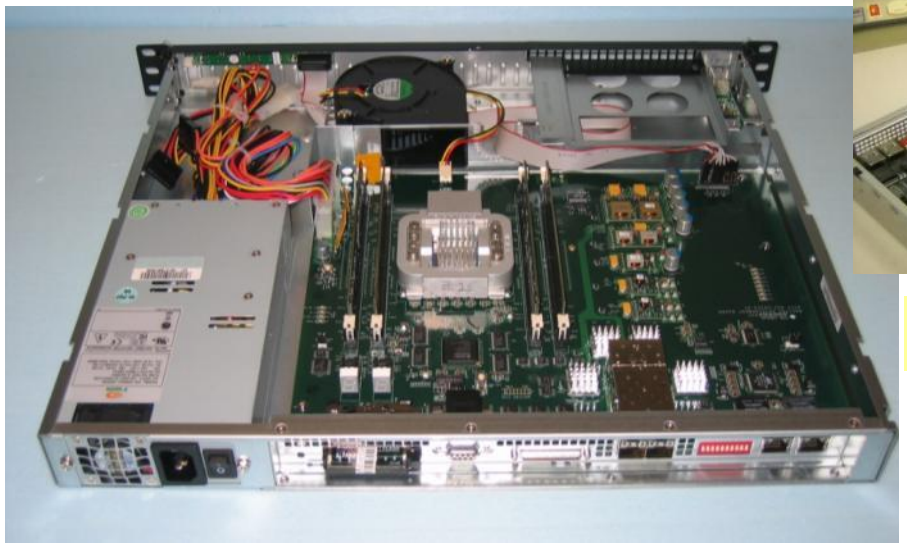
- **Excellent performance across processing domains**
- **FIR filter – 5 GFLOPS sustained performance (26% peak)**
- **FFT – 4 GFLOPS sustained performance (21% peak).**



- ***Autonomous operations***
- ***Parallel Processing***
- ***Sensor Fusion***
- ***ALTAIR – Lunar Lander***
- ***Europa – Deep Space***

MAESTRO RH Multi-Core Processor

- **Functional test complete**
- **MAESTRO Development Board (MDB) system available for software/hardware application development**

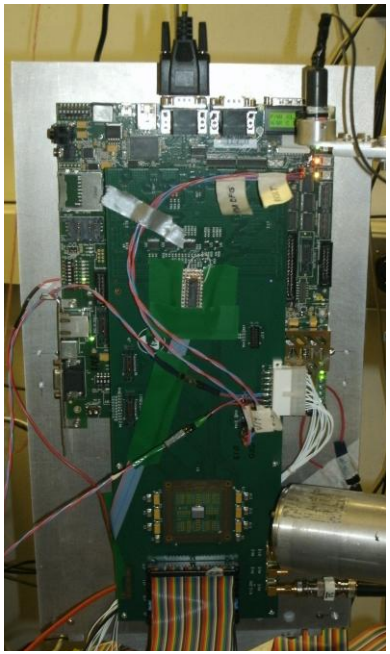


MDB system in use for software development

Demonstration Testing

- **Error Rates predicted**
  - **Errors classified by type**
    - **Uncorrectable SRAM errors**
    - **Recoverable errors**
    - **Un-recoverable errors**
  - **Predictions were used in design trades**
- **Heavy Ion testing performed**
  - **Scan chains**
  - **Functional at-speed testing**
  - **Variety of tilt and rotation angles**

RHBD ARM Cortex™ R4

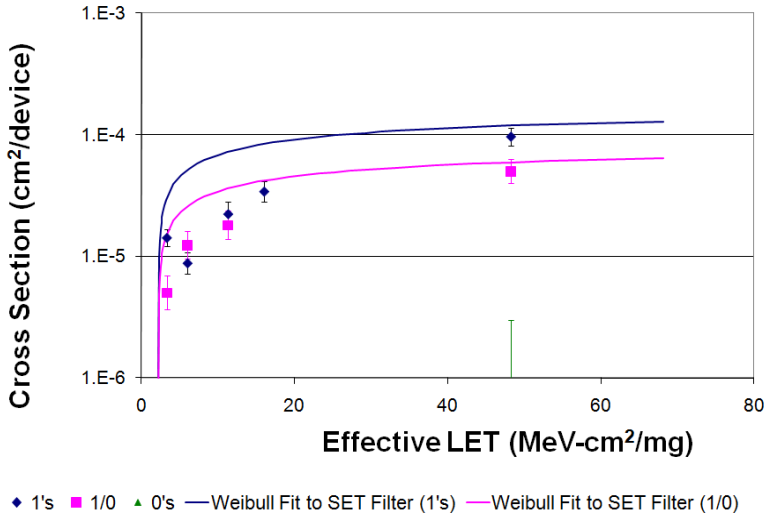


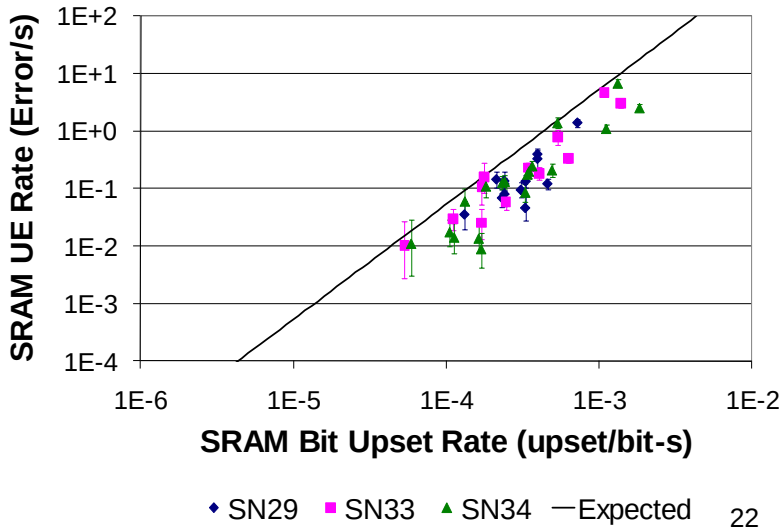
RHBD Single-Core Tilera

Reset Logic and SRAM Results

- **Reset tree Single Event Transient (SET) sensitivity of the RHBD ARM Cortex™ R4 processor**
- **Solid curves represent the predicted cross section from logic gates in the RESET tree, as identified in the bottom-up analysis**
- **Uncorrectable error rate in SRAM test array of the RHBD ARM Cortex™ R4 processor as a function of SRAM bit upset rate**
- **The expected error rate is also shown**

Validated our approach of predicting microprocessor sensitivity based on testing dedicated test structures in the same design environment



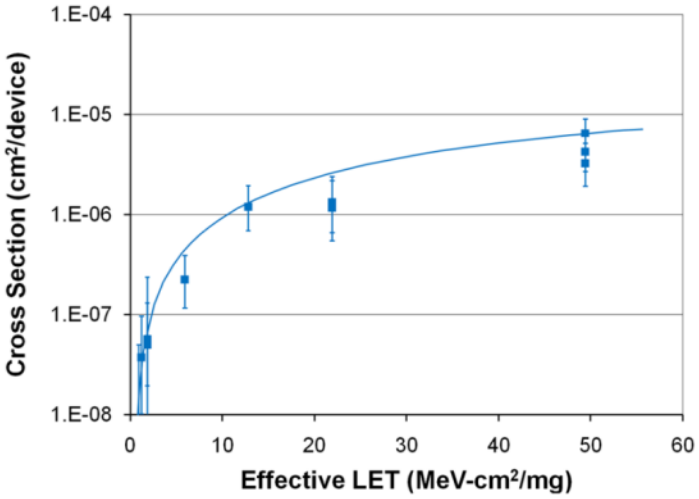


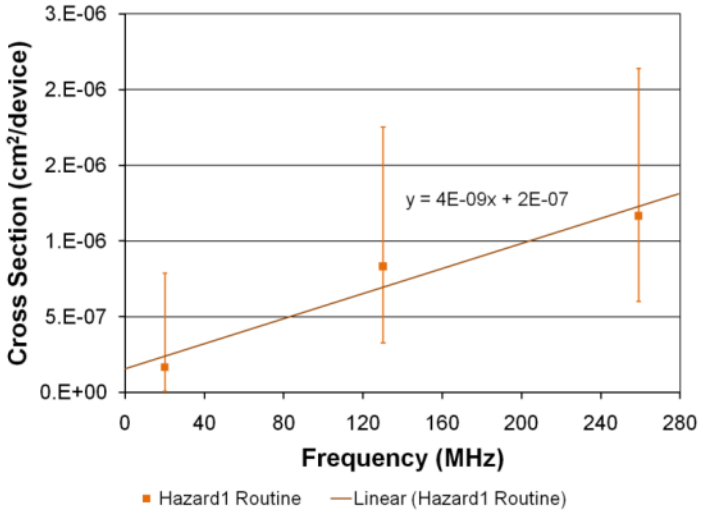
Functional Test Results – Recoverable Errors (SEFI)

- **All RHBD Single-Core Tilera processor test routines produced similar Recoverable Error (SEFI) cross sections**
- **Predicted Recoverable Error Rate was within 35% of the rate calculated from measured results**
- **Number of Recoverable Errors increased with frequency as predicted**
  - **Combined errors from logic SETs, clock tree SETs and RESET tree SETs**
  - **Errors from logic SETs dominated rate**

	Predicted Error Rate (errors/processor-day)	Measured Error Rate (errors/processor-day)		
		Add	Hazard1	Hazard5
Recoverable Errors	4.8E-05	3.2E-05	5.8E-05	5.7E-05

Recoverable Error Cross-Section





RHBD90 Library

- **Boeing has distributed the library to several government agencies and licensed it to several companies**
- **Aeroflex Colorado Springs is working to productize and qualify the RHBD90 ASIC design flow and library to QML V**

Conclusions

- **RHBD on *leading-edge commercial device technologies* provides needed performance and integration density with assured access**
- **Robust RHBD ASIC design environment in place at Trusted Design Center**
- **90nm Rad Hard by Design ASIC capability has been demonstrated in multi-million gate SoCs**


BOEING