Micro-RDC

Radiation Hardened by Design 90nm CMOS ASIM Chip for Spaceborne Sensor Applications

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Outline

- Structured ASIC 90nm IBM 9LP Process Overview
- Radiation Hardened by Design
- ASIM Block Diagram and Toplevel
- SASIC ASIM Features
- SASIC ASIM 7x7 mm Die Bonded Out to LGA 484 Package
- Evaluation Board with LGA 484 Socket
- SASIC ASIM Power Management and Power Consumption Measurements
- Post Silicon Verification Tests
  - Functional Tests
  - Wishbone Cores
  - Complex Flows
- Structured ASIC Verification
- Conclusions
- Questions

Funding Support

- The development of the ASIM Structured ASIC has been funded by the Air Force Research Laboratory (AFRL) during a Phase II SBIR.

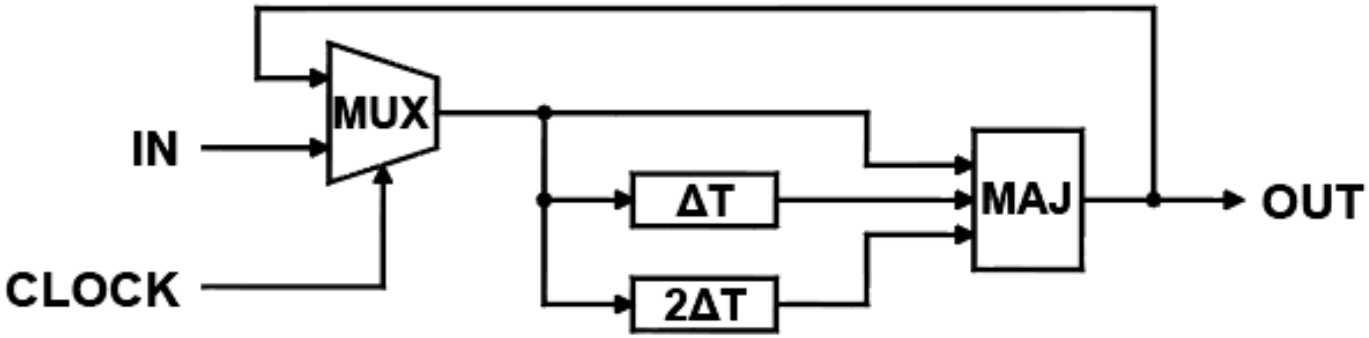
- The Post Silicon Verification effort has been funded through an AF SBIR Enhancement by AFRL to functionally test the ASIM chips and develop evaluation and radiation test boards and investigate a packaging road map.

Structured ASIC 90nm CMOS IBM 9LP Hardness Estimate:

- TID > 1Mrad(Si)
- SEU > 1e-5 Errors/day
- SEL > 100 MeV-cm2/mg (LET)

RHBD Circuit Approach (SEU and SET)

- **Data latch SEU/SET mitigation**
  - Temporal sampling to achieve both spatial and time redundancy
  - Variable sampling delay for hardness / performance tradeoff
  - Immune to multiple node strikes and transients on any node
  - Self scrubbing, does not integrate errors as normal TMR

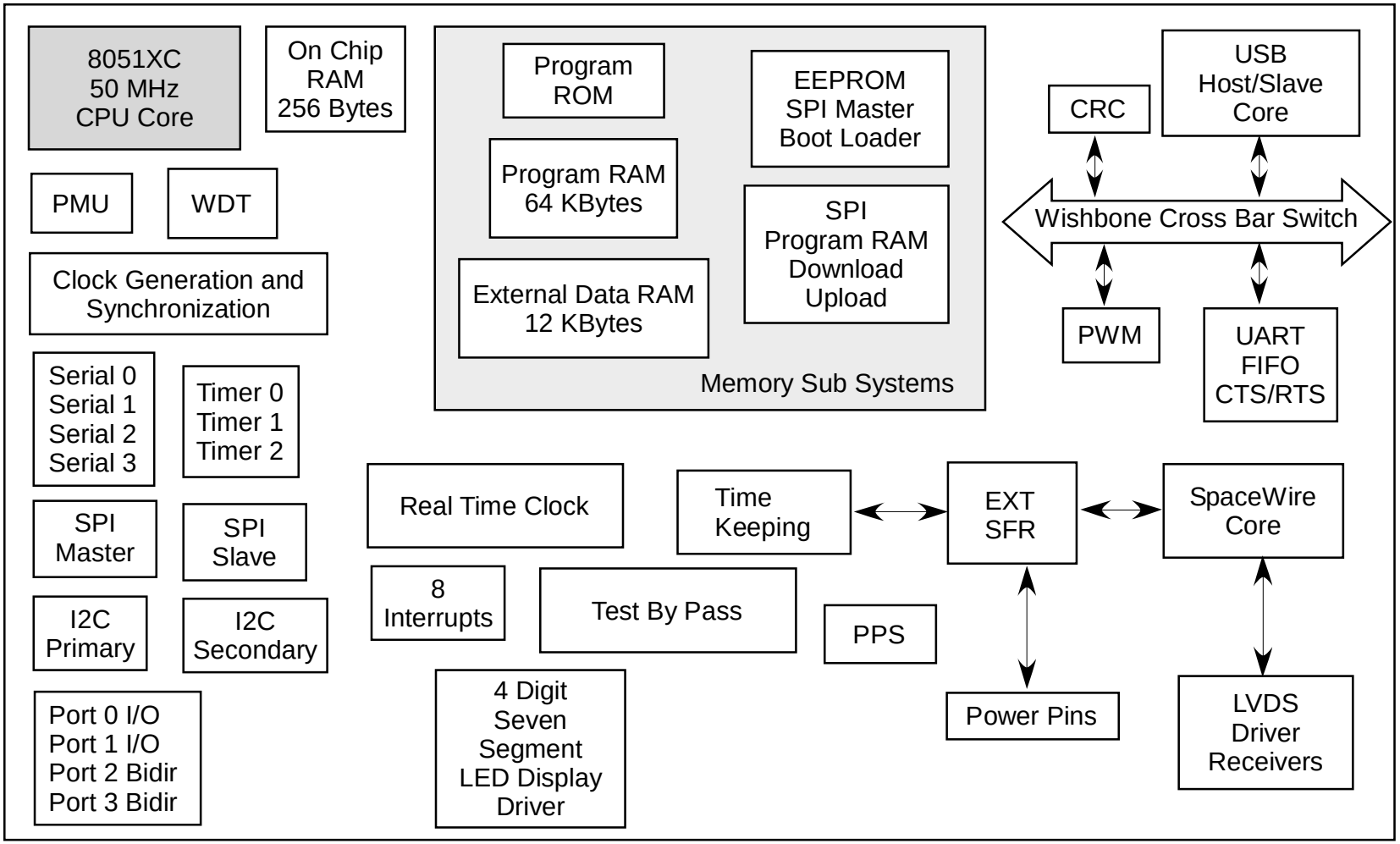


Ref: Mavis, Eaton 2002

- **SRAM SEU/MBU/SET mitigation**
  - Conventional 4T data storage with PMOS access (single and dual port)
  - EDAC for single bit errors
  - Scrubbing to reduce multiple bit error accumulation over time
  - Architectural solution to SETs and MBUs

Ref: Mavis, MRQW 2007

SASIC ASIM High Level Block Diagram



SASIC ASIM Features

8051XC CPU (CAST)
- 50 MHz Clock
- Average 8x Speed Up Over Standard 8051
- ALU Performs 8-bit Arithmetic, Multiplication and Division, and Boolean Manipulations
- Write to Program Memory RAM
- Two 8 bit I/O Ports (32 lines)
- Two 8 bit Bi-Directional Ports
- Three 16-bit Timer/Counters
- Real Time Clock (RTC)
- Watch Dog Timer
- 8 External Interrupts

Memory Sub Systems
- On Chip Internal RAM (256x8)
  - Temporal Latch based Flip Flops
- On Chip External 12 Kbytes Data RAM
  - Design Hardened Distributed SRAM
- On Chip 64 Kbytes Program RAM
  - Bootup from External SPI EEPROM
  - Design Hardened 64K Program SRAM w/EDAC
- On Chip ROM for Testing and Bootup
- SPI Slave for Firmware Download and Upload to Silicon
- Support for 128 Kbytes External SPI Non Volatile Memory

Power Management Unit
- Idle and Stop (Deep Sleep)
- Power Pins (Do not Change in Idle or Deep Sleep or Wakeup)

Communications
- UART with FIFO and CTS/RTS DTR/DCD Support
- Four Serial Ports with Independent Baud Rate Generators
- USB 1.1 Host/Slave Controller
- SpaceWire Multiple Rates Including 10 Mbps and 50 Mbps
- LVDS Driver/Receiver for SpaceWire

Peripherals
- I2C Primary Master
- I2C Secondary Master
- SPI Master with 8 Slave Selects
- SPI Slave
- Test By Pass
- CRC Accelerator
- PWM
- PPS Input (Pulse Per Second)

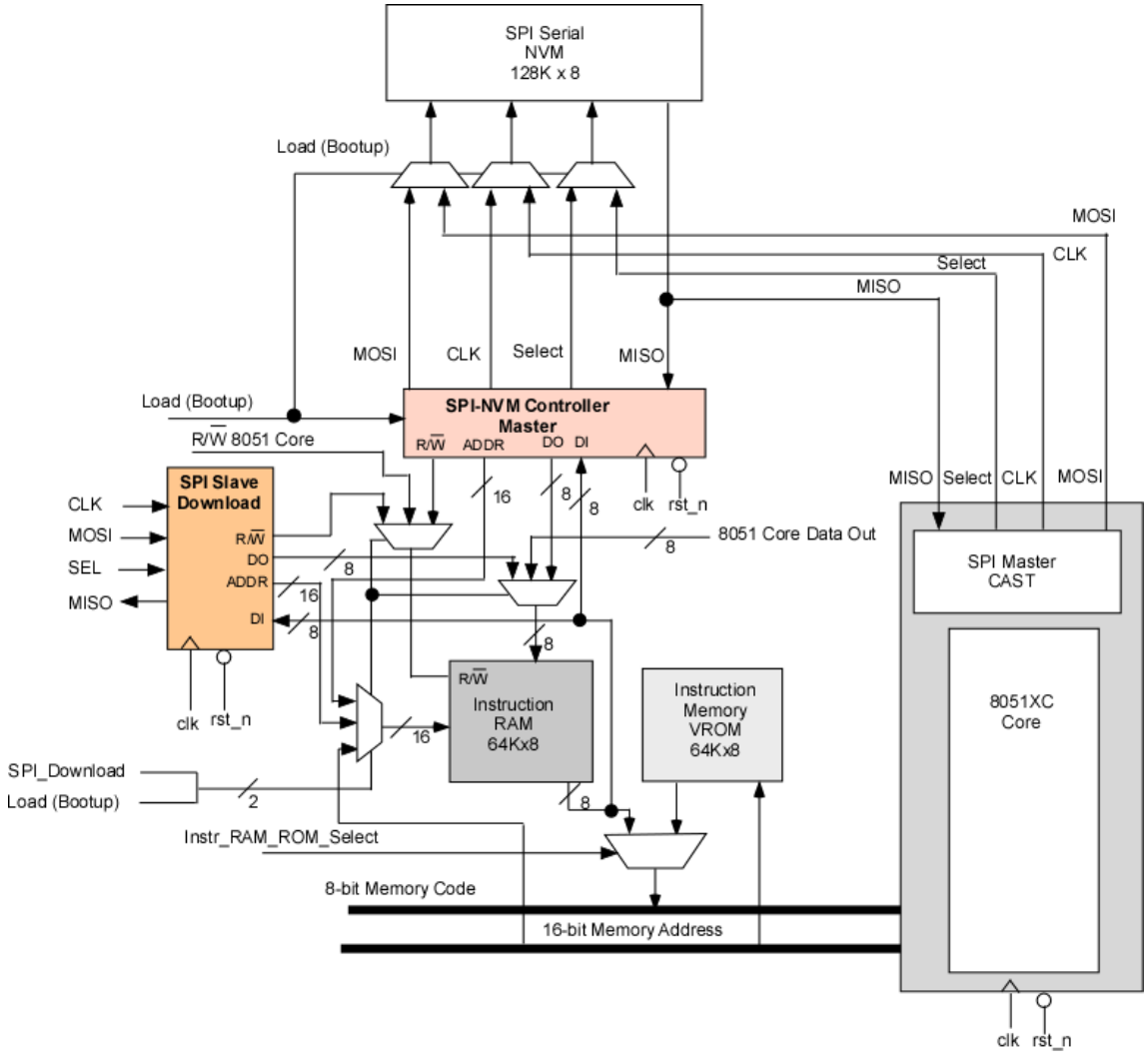
Power Supply
Dual Voltage Supply 1.2 V Core and 1.2V to 3..3V I/O

Software Development Support

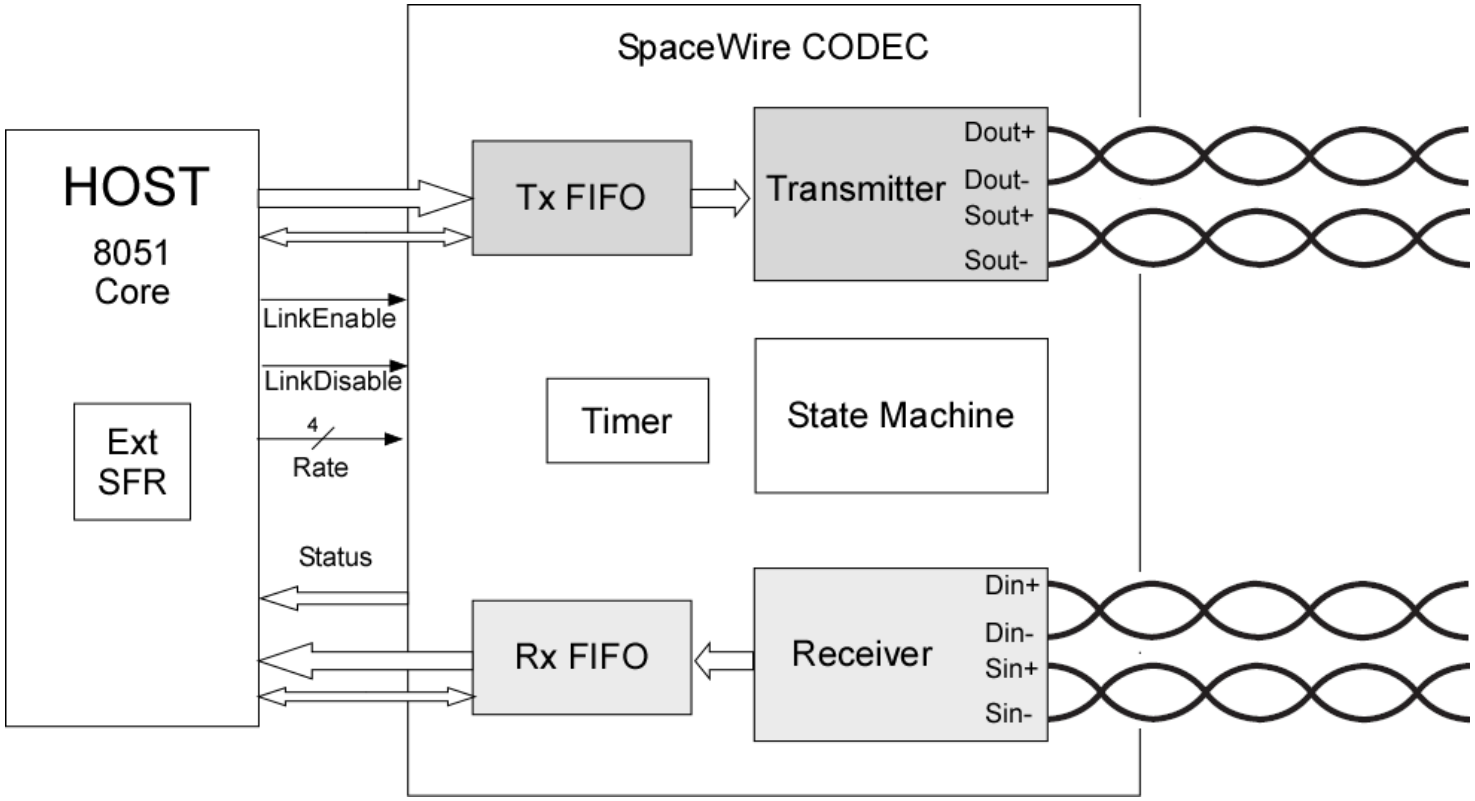
Software Support (Separate License Required for Keil)

- Full Support for Keil C and Assembly Firmware Development
- Support for Keil TinyOS
- Macro Assembler 8051 (ASEM-51)
- C API for SpaceWire, SPI Master, I2C, Serial Interfaces
- Firmware Download to Silicon via USB/SPI Interface
- Tool for EEPROM Programming from Intel Hex Checksum File
- Tool to Write XTEDS to EEPROM

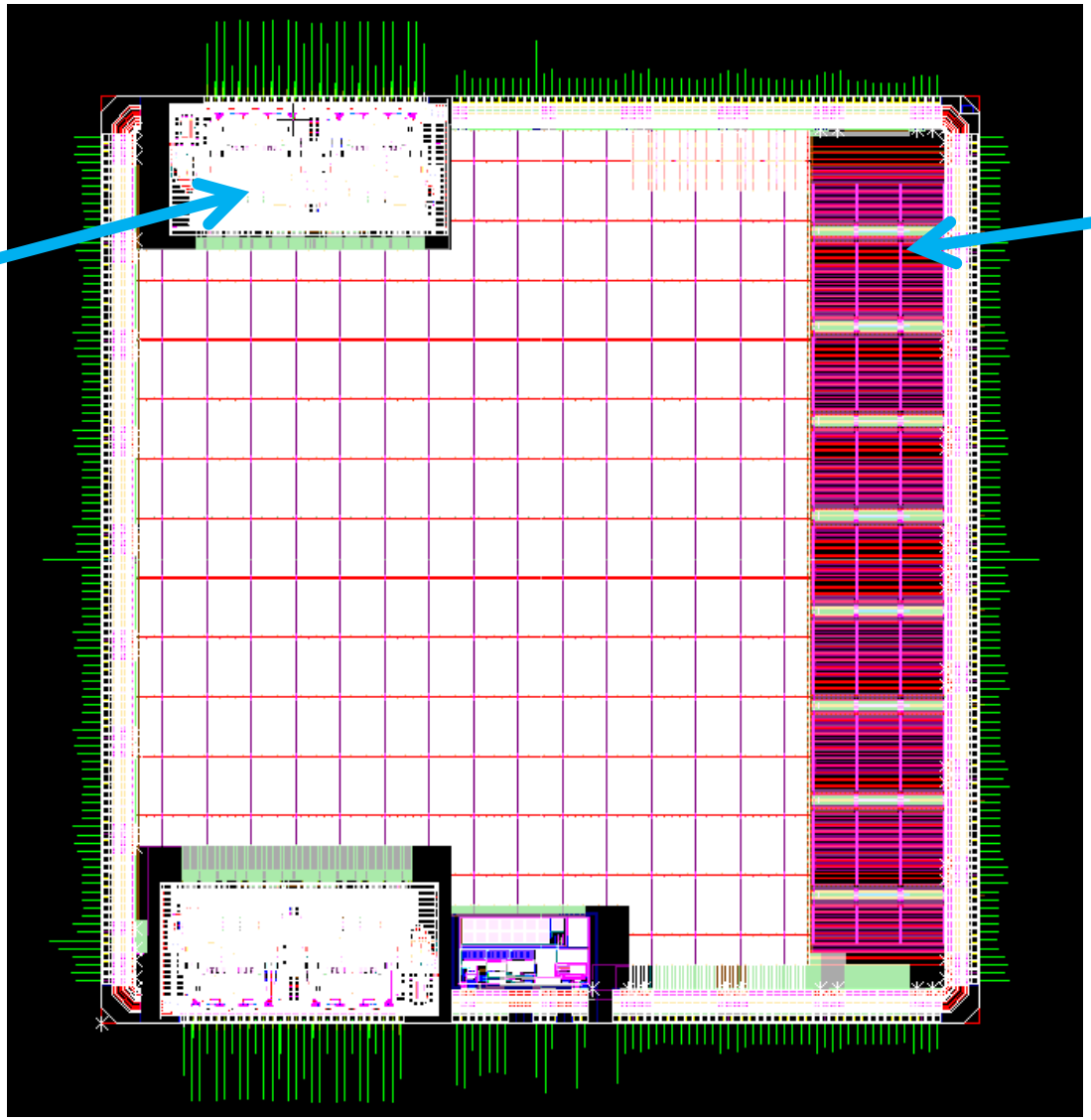
SASIC ASIM Memory Subsystem, Bootup and XTEDS Support



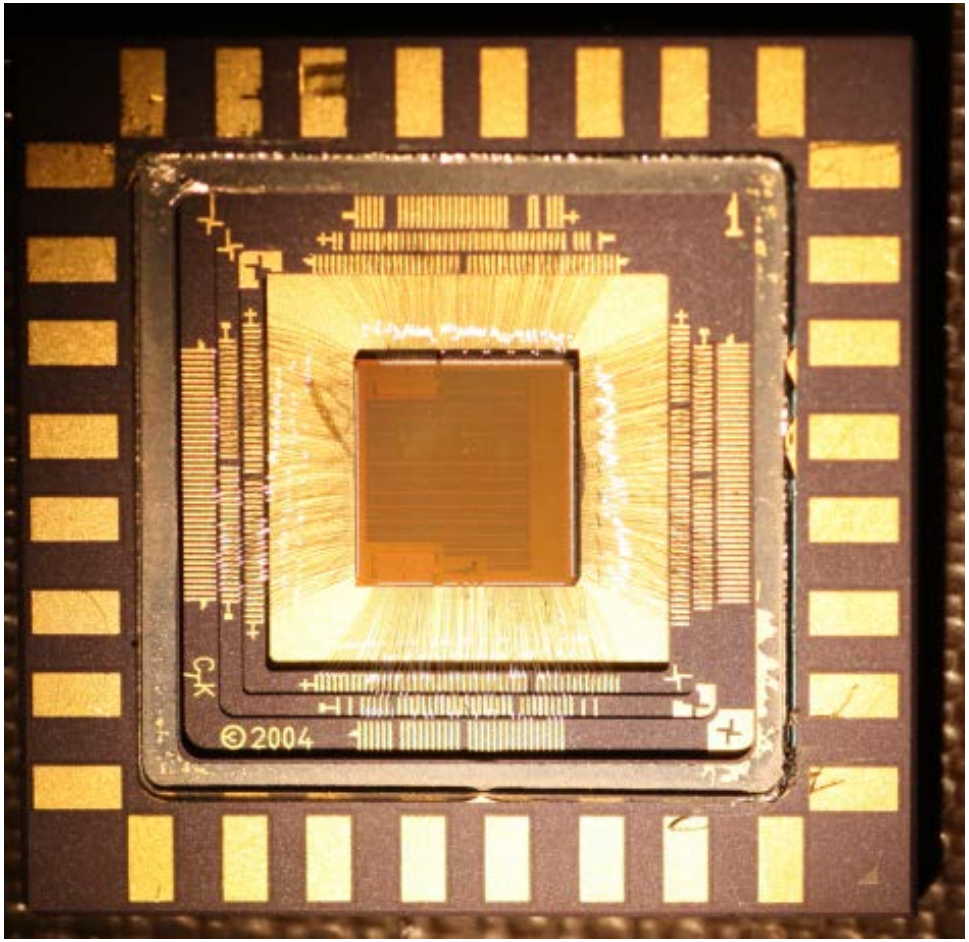
SpaceWire Interface



SASIC 7x7mm Full Featured Part



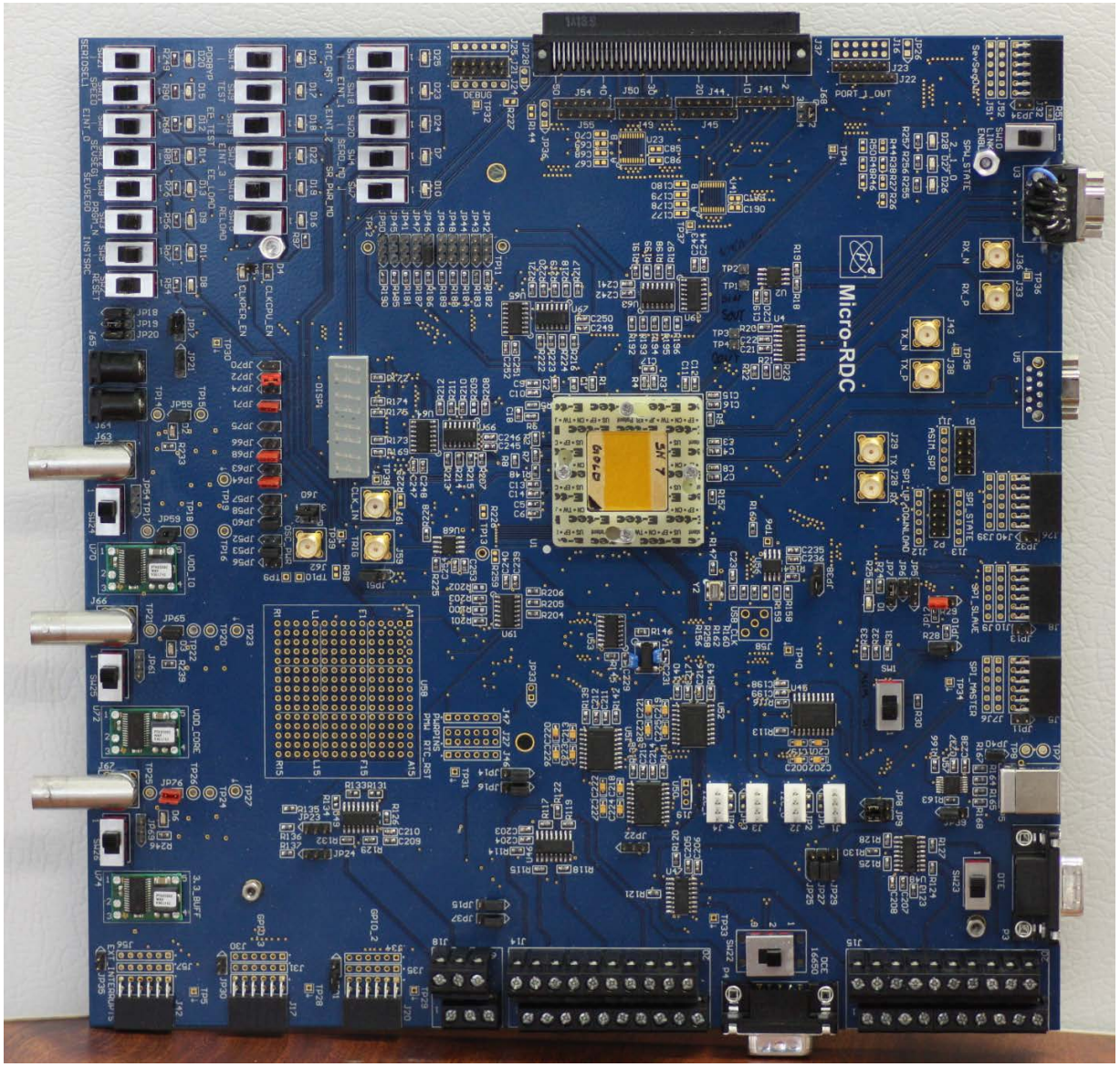
SASIC ASIM 7x7 mm Die Bonded Out to LGA 484 Package



SASIC ASIM Evaluation Board

- LGA 484 Socket
- Separate supplies for Core (1.2V), Chip IO (3.3v) and Peripherals (3.3V).
- Current monitoring of all supplies.
- Single 5V supply support.
- Support for 16 input and 16 output signals.
- Support for 16 GPIO signals.
- Space Wire external LVDS drivers and Receivers and socket.
- 4x RS-422 Drivers and Receivers.
- Debounced switches for reset, SPI Download, manual Bootup, automatic Bootup, interrupts.
- Differential LVDS lines and SpaceWire connector for on-chip LVDS support.
- Program Counter for logic analyzer monitoring and debug.
- RS-232 DCE and DTE (with RTS/CTS hardware flow control).
- USB Physical Layer and 48 MHz clock.
- SMA CPU Clock input.
- Dual I2C Buss interface
- On Board ATMEL Flash (128Kx8) for Bootup and XTEDS.
- Connectors for SPI Firmware download/upload via USB/SPI interface to PC.
- 4 digit Seven Segment display for debug and software development.
- SpaceWire state monitoring.
- Support for SPI Master and Slave using PMODs (12 pin).
- Prototype Area

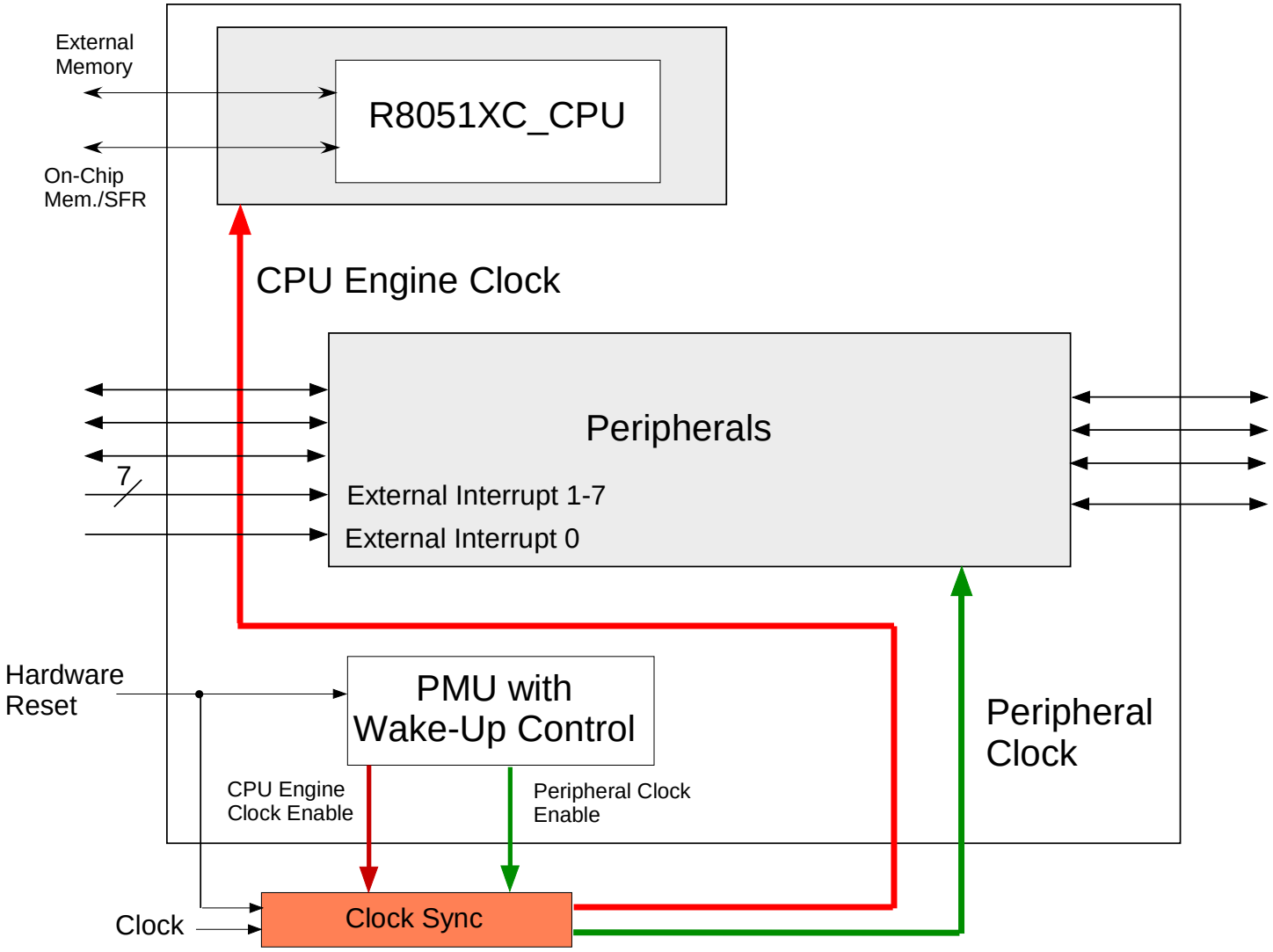
Assembled SASIC ASIM Evaluation Board



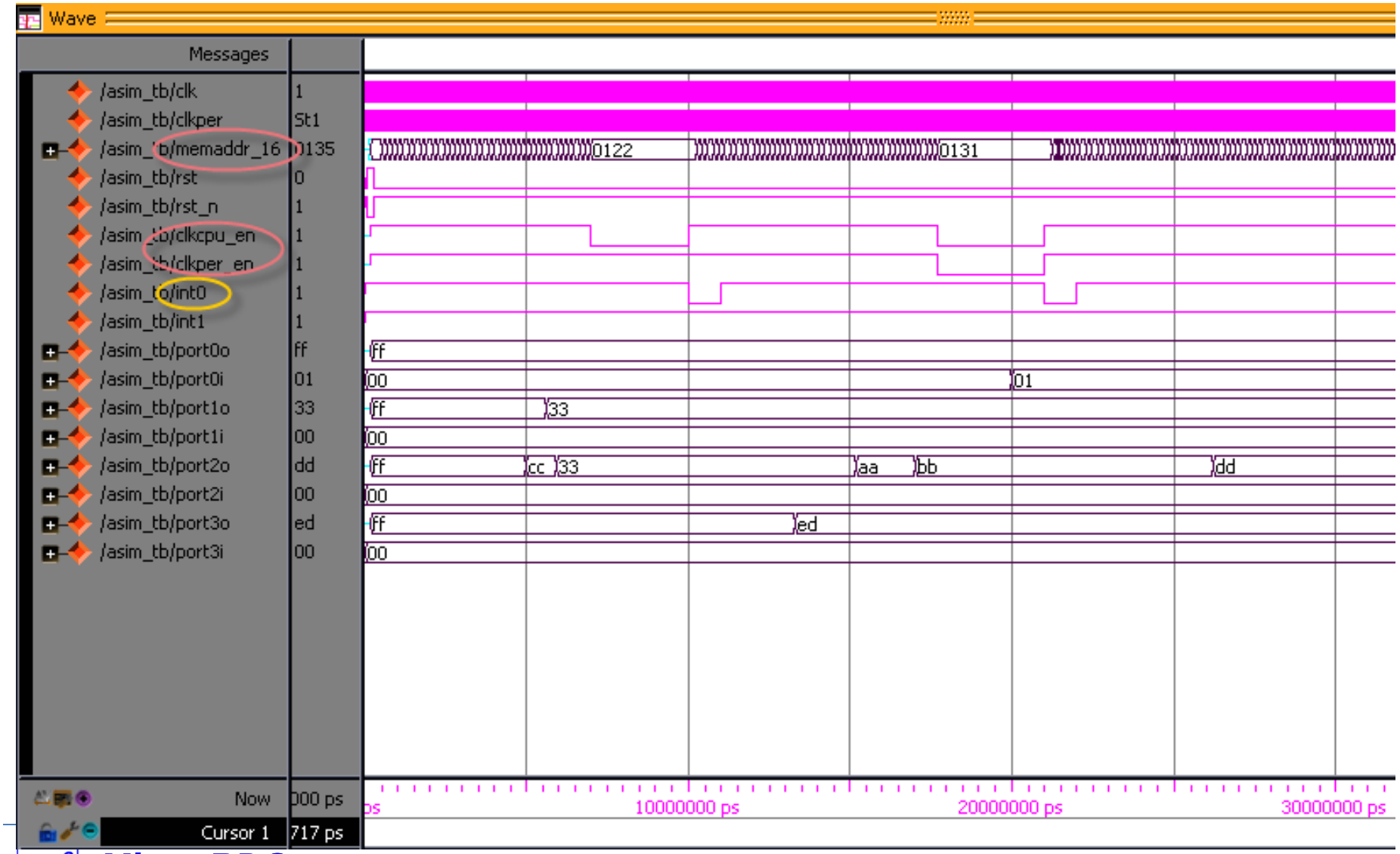
SASIC ASIM Power Management

- Idle Mode
  - CPU Clock Off
- Deep Sleep
  - CPU and Peripherals Clock Off

ASIM CAST Core Power Management Idle and Deep Sleep Modes



Power Management Timing Diagram

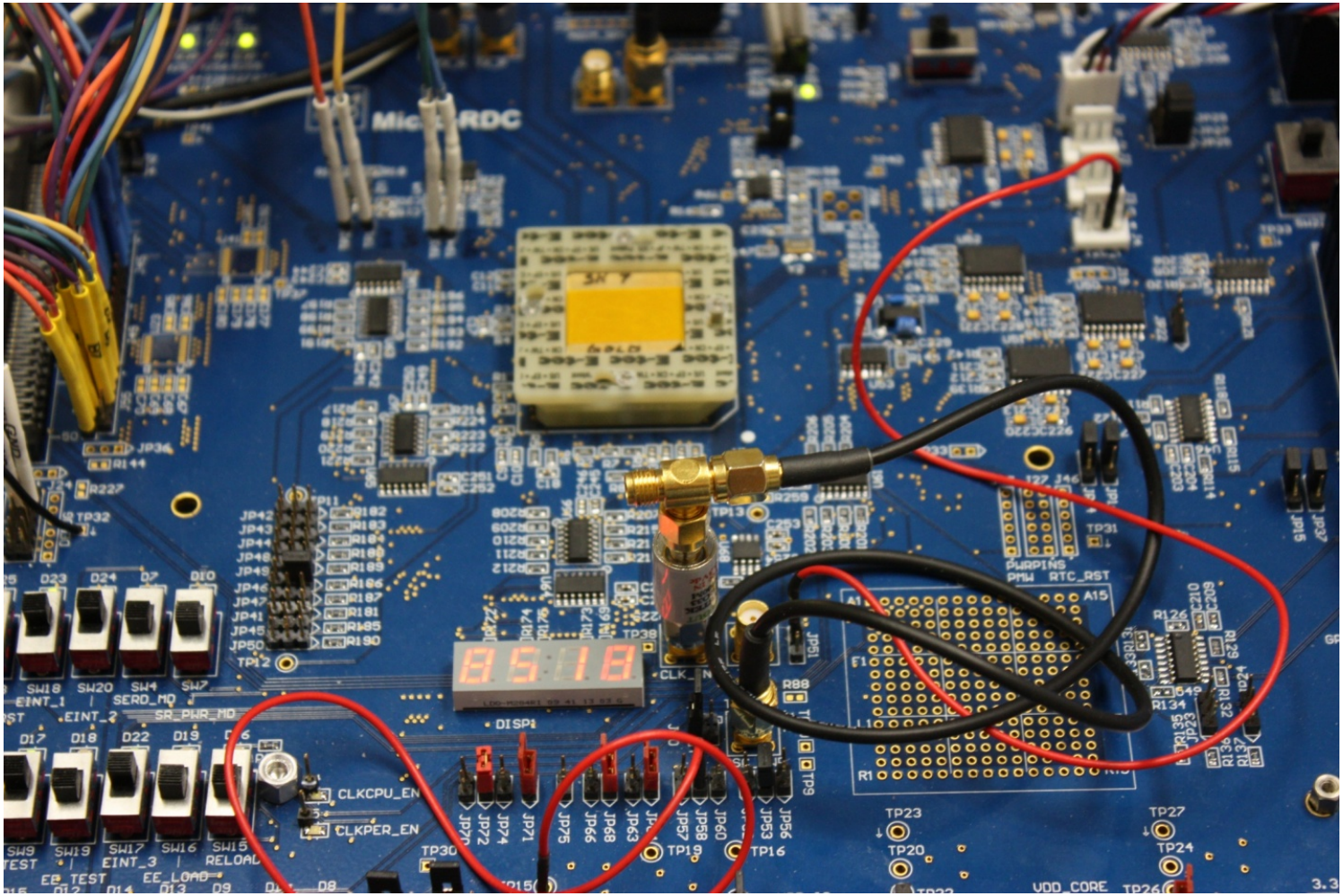


SASIC ASIM Built in ROM with Idle and Deep Sleep Test Modes

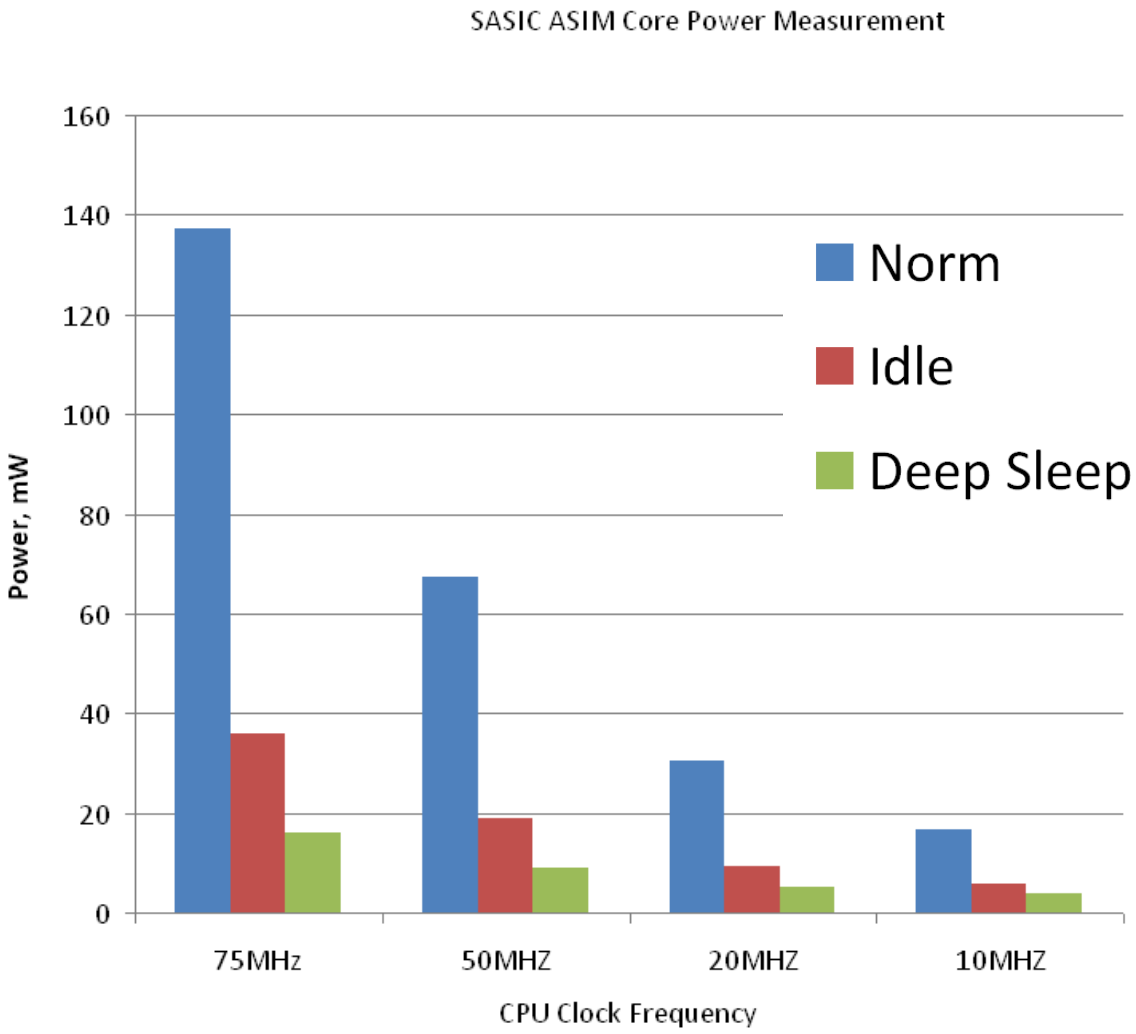
```
ASIM Plug and Play Satellite
MICRO-RDC, Albuquerque, NM
1 XTEDS= x
2 SPI,MFG ID = A
3 S_0 RS232 = B
4 WB_UART = D
5 SPW = S
6 WDT = W
7 Timer_0 = T
8 PMU_IDLE = J
9 PMU_DEEP_SLEEP = K
10 Self Test = L
BS_0_RS232

Press any key to be repeated on terminal
Enter '%' to escape test
This is an entry from Serial port 0%
Test is Done
Press any key to continue
```

SASIC ASIM Evaluation Board Clock Input



Measured Power Consumption Taped Out Silicon SASIC ASIM Idle and Deep Sleep Modes Core Power (1.2V)




```
Core Vdd=1.2V
IO   Vdd=3.3V
```

SASIC ASIM Post Silicon Functional Verification Tests

- Functional Unit Tests
- Wishbone Cross Bar Switch Cores
- SpaceWire CODEC Tests
- Complex Flows Tests

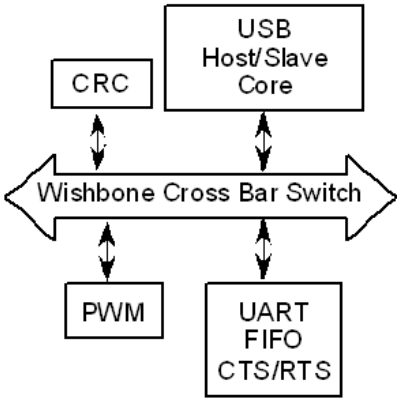
Functional Unit Tests

No.	Test Name	Block Tested	Function	Pass
1	s0_serial_work	Serial IO 0	Serial IO 0 send out and receive data	Pass
2	s1_serial_work	Serial IO 1	Serial IO 1 send out and receive data	Pass
3	s2_serial_work	Serial IO 2	Serial IO 2 send out and receive data	Pass
4	s3_serial_work	Serial IO 3	Serial IO 3 send out and receive data	Pass
5	chipram	On chip ram	On Chip Register File 256x8	Pass
6	test_xc	8051 core	The Keil R8051xc test code for extended 8051 functionality	Pass
7	ext_data_mem	External data memory	Write to a group of external data memory and read back. (12K)	Pass

Functional Test Continued

No.	Test Name	Block Tested	Function	Pass
8	I2C Master	I2C Core	Verify with I2C Master controlling external ADC and DAC I2C devices	Pass
9	I2C Slave	I2C Core	Setup Core as I2C slave	
10	SPI Master	SPI Core	SPI Master reads XTEDS from external NVM.	Pass
11	SPI Slave	SPI Core	SPI Slave communicating with Diolan I2C/USB Bridge	
12	Watch Dog Timer	WDT	Verify WDT reset.	Pass
13	Timers	Timer 0, 1 and 2	Verify CAST Core Timers	Pass
14	LVDS Lane	Adsantec SERDES MACRO LVDS	Verify LVDS Lane. CMOS Tx LVDS Tx, LVDS Rx, CMOS Rx	Pass

Wishbone Cross Bar Switch Cores



No.	Test Name	Block Tested	Function	Pass
1	wb_uart	UART	OpenCores 16550 UART Wishbone Bus	Pass
2	USB Host	USB Host Slave	Wishbone and OpenCores USB Host/Slave	Pass
3	crc	CRC	Check the CRC out after feeding certain values. Test Wishbone Bus	Pass
4	pwm	PWM	Setup PWM to toggle the PWM output pin Wishbone Bus	Pass

SpaceWire CODEC Tests

No.	Test Name	Block Tested	Function	Pass
1	Spacewire Transmit at 5,10, 25 Mbps	Spacewire Codec	Cross verify Spacewire with 4Links test equipment	Tx Pass
2	SpaceWire Loop Back @ 10 Mbps External LVDS	Spacewire Codec	Loop Back Test. Check if Run State achieved.	Pass
3	SpaceWire Loop Back @ 10 Mbps On-Chip LVDS	Spacewire Codec	Loop Back Test. Check if Run State achieved.	Pass
4	Space Receive at 5, 10, 25, and 50 Mbps	Spacewire Codec	Cross verify Spacewire with 4Links test equipment	Rx Pass

Complex Flows Tests

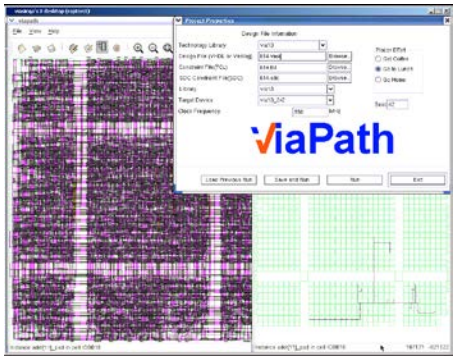
No.	Flow Name	BlockTested	Function	Pass
1	SPI Download PRGM_RAM EXECUTION WRITE	SPI Slave Block SRAM	Download code through SPI Slave, Execute from Block SRAM, do a Write and Read from Program SRAM	Pass
2	EEPROM Boot-up	SPI EEPROM Master, Muxes to SRAM, Block SRAM, Bypass Mode, Manual Load and Reset	Copy code from EEPROM into Block SRAM with SPI Master, Execute and test SRAM Program Memory Write/Read	Pass
3	Automatic Reload EEPROM	SPI EEPROM Master, Muxes to SRAM, Block SRAM, Bypass Mode, Reload and Automatic Reset, RAM Select, Soft Reset Interrupt 3	Copy code from EEPROM into Block SRAM with SPI Master, Execute and test SRAM Program Memory Write/Read. Test automatic boot-up sequence.	Pass
4	PMU	PMU and Clock Generation	Idle Mode and Sleep Mode	Pass

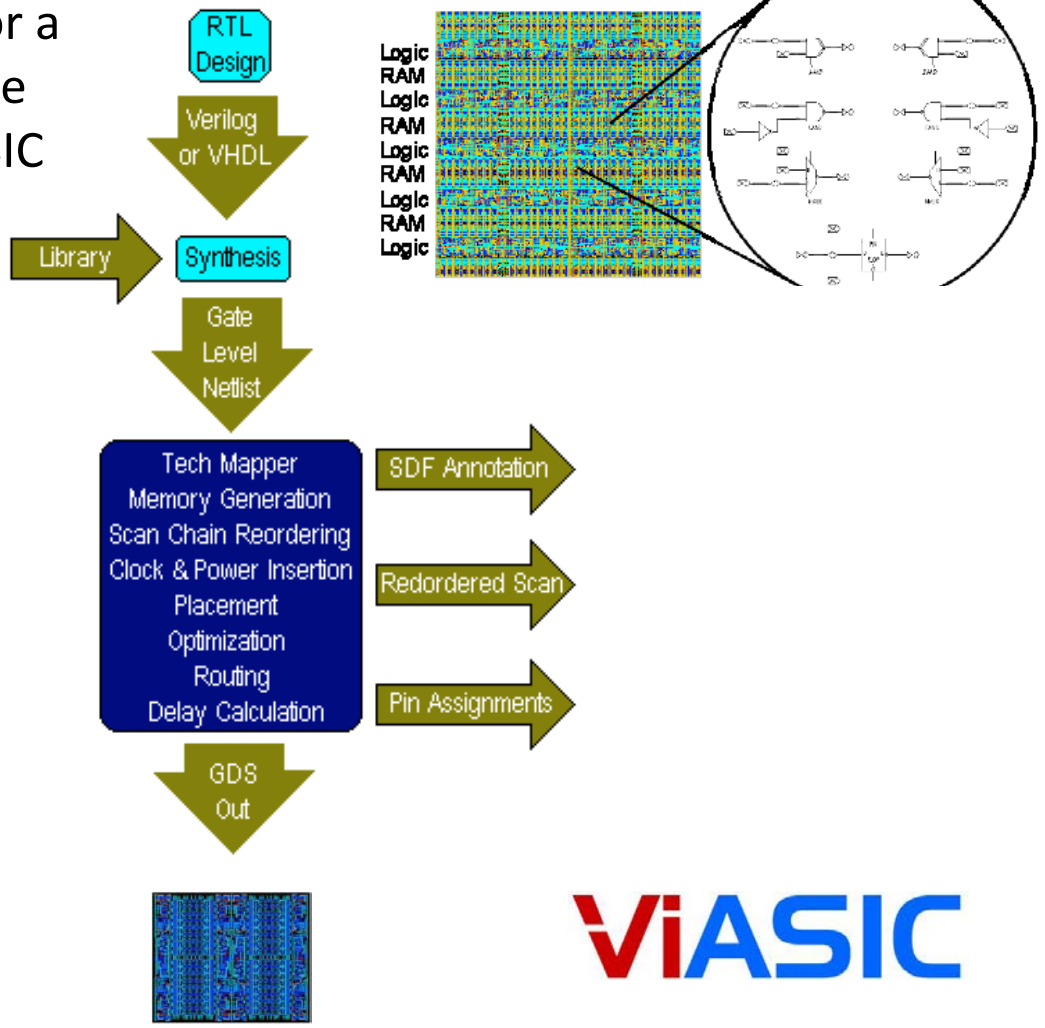
Structured ASIC Verification

- Verification of SASIC Logic Fabric running at 75 MHz Clock with 40% utilization
- Verification of Block SRAM Read and Write (64Kx8) at 75 MHz Clock
- Verification of Dual Port Distributed RAM at 75 MHz Clock
  - Configured as 12Kx8 RAM
  - Configured as 2048x9 Dual Port RAM for SpaceWire FIFO
- Verification of Adsantec LVDS Transmit and Receive

ViASIC ViaPath
Structured ASIC Place and Route Tool Verified

- **ViaPath** Place and Route Tool for a One-Mask (Via-3) programmable Design-Hardened Structured ASIC





ViASIC

Conclusions

- SASIC ASIM Taped Out on IBM 90nm 9LP CMOS Process.
- ASIM Chip uses RHBD techniques including Temporal Latches for SEU immunity.
- ASIM Chip achieves very low power consumption by implementing Idle and Deep Sleep modes.
- Power reduction through Clock Scaling verified.
- Evaluation Board fabricated and built for Post Silicon Verification Tests of all functional units, complex flows and all interfaces.
- All functional tests pass in Post Silicon Verification.
- All Cores interfaced to 8051XC CPU using Wishbone Crossbar Switch pass Post Silicon Verification tests.
- EEPROM Bootup and on demand on-line scrubbing pass in taped out Silicon.
- Built in ROM and SPI Firmware download capability allow all functional units and complex flows to be tested in Silicon.
- LGA 484 Package and Evaluation Board with LGA 484 Socket allow for full hardware integration evaluation in spaceborne systems with complete software/hardware development support.
- Support for SPA-S, SPA-U and SPA-1 Space Avionics Plug and Play Systems.

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