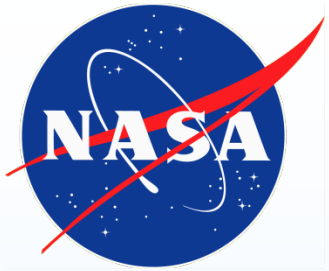

Introduction and NASA Electronic Parts and Packaging (NEPP) Program Overview

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To be presented by Kenneth A. LaBel at the Electrical, Electronic, and Electromechanical (EEE) Parts for Small Missions, Greenbelt, MD, September 10-11, 2014.

Acronyms

3D	Three Dimensional
ADC	Analog to Digital Converter
Aero	Aerospace
ARC	Ames Research Center
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off The Shelf
CSLI	CubeSat Launch initiative
DIP	Dual Inline Package
DNL	Differential Non-Linearity
DSP	Digital Signal Processor
EDAC	Error Detection and Correction
EEE	Electrical, Electronic, and Electromechanical
ENOB	Effective Number of Bits
EPI	Epitaxial
ESSP	Earth System Science Pathfinder
FCBGA	Flip Chip Ball Grid Array
FPGA	Field Programmable Gate Array
GAS can	GetAway Special can
Gb	Gigabit
Gbps	Gigbits per Second
GHz	Gigaherz
GSFC	Goddard Space Flight Center
HST	Hubble Space Telescope
IC	Integrated Circuit
INL	Integral Non-Linearity
IO	Input Output
ISS	International Space Station
JIMO	Jupiter Icy Moons Orbiter
JPL	Jet Propulsion Laboratories
JWST	James Webb Space Telescope
k	Kilo
kb	Kilobit
LCC	Leadless Chip Carrier
M	Meg

MER	Mars Exploration Rover
MHz	Megaherz
MIDEX	Medium-Class Explorer
MIL	Military
MIPS	Millions of Instruction per Second
MP3	Moving Picture Experts Group-I or II Audio Layer III
MRO	Mars Reconnaissance Orbiter
Msps	Megasamples per second
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts and Packaging
NID	NASA Interim Directive
nm	nanometer
NMOS	N-type Metal Oxide Semiconductor
NPR	NASA Procedural Requirements
NPSL	NASA Parts Selection List
NRE	Non-Recurring Engineering
PCB	Printed Circuit Board
POF	Physics of Failure
RF	Radio Frequency
SAA	South Atlantic Anomaly
SCD	Source Control Drawing
SDRAM	Synchronous Dynamic Random Access Memory
SEE	Single Event Effect
SERDED	Serializer Deserializer
SEU	Single Event Upset
Si	Silicon
SMA	Safety and Mission Assurance
SME	Subject Matter Expert
SMEX	Small Explorer
SOC	Systems on a Chip
SOI	Silicon on Insulator
SWaP	Size, Weight, and Power
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
um	micron

Why are we here?

- As a follow-on to an internal NASA EEE parts workshop held in 2013, the NEPP Program will be hosting an open workshop entitled
  - "EEE Parts for Small Missions".
- Small Missions are loosely defined as those under 500 kg, but the emphasis here is on under 100 kg.
- The workshop focus will discuss tailoring EEE parts approaches based on mission risk and expectations.
- This includes "traditional" (science) and "non-traditional" (demonstration) missions with CubeSat electronics a prime discussion area.
- ***The real purpose is to aid the community in understanding risks with EEE parts and open a forum for discussion both now and in the future.***

Agenda – Day 1

		Wed Sep 10 2014
	Session	
8:00 AM		Coffee and registration check-in
9:00 AM	*Introduction and Government Agency Presentations*	*Introduction and NASA Electronic Parts and Packaging Overview - Ken LaBel*
9:20 AM		*European Space Agency: CubeSat Overview - Roger Walker, ESA*
10:00 AM		Break (20 min)
10:20 AM		*Small Spacecraft Technology at NASA - Andrew Petro, NASA*
11:00 AM		*NASA CubeSat Launch Initiative - Carol Galica or Garrett Skrobot, NASA*
11:30 AM		*Small Satellite Parts On Orbit Now (SPOON) - Charlene Jacka, AFRL*
12:00 PM		Lunch (60min)
1:00 PM	*Basic Concepts*	*Why Space is Unique? The Basic Environment Challenges for EEE Parts - Ken LaBel*
1:30 PM		*Traditional EEE Part Testing versus "Higher Assembly" Validation Tests - Is Better the Enemy of Good Enough? - Henning Leidecker*
2:00 PM		*Panel: Fault Tolerance: Does It Cure All Ills? - led by Jesse Leitner, NASA*
2:30 PM		Break (30 min)
3:00 PM	*COTS and Risk*	*Is It Wise to Fly Automotive Electronics - Michael Sampson, NASA*
3:30 PM		*The Challenges of PEMs Packaging - S. Ali Lilani, Integra Technologies*
3:50 PM		*Relative Radiation Risk Reduction for Small Spacecraft and New Designers - Michael Campola, NASA*
4:20 PM		*Using Modeling to Provide Realistic Radiation Requirements - Thomas Jordan, EMPC*
4:45 PM		End of Day 1

Agenda – Day 2

		Thurs Sep 11 2014
	Session	
8:00 AM		Coffee and registration check-in
9:00 AM	*Approaches to Small Missions*	*Cygnss: Lessons Learned from a Class D Mission - Jessica Stack Tumlinson, SwRI*
9:30 AM		*RadFx: Cube-Sat Based Payload to Study Radiation Effects in Advanced Electronics - Robert Reed, Vanderbilt*
9:50 AM		*Small Satellites Hardened by Design Using Non-space Qualified EEE Parts - Roberto Ciblis, INVAP*
10:10 AM		Break (20 min)
10:30 AM	*EEE Parts Qualification*	*Tailoring Traditional Parts Qualification - Pat Dugan, NASA*
11:00 AM		*Tailoring TOR for Class D Missions - Charles Hymnowitz, AEi Systems*
11:30 AM		*Alternative Methods to Qualify EEE parts for Small Missions - Craig Hillman, DFR Solutions*
12:00 PM		Lunch (60min)
1:00 PM	**Invited**	*The First 200 CubeSats - Prof. Michael Swartwout, Saint Louis University*
1:30 PM	*NEPP Tasks*	*CubeSat Parts Database: NASA Usage and Kit Manufacturers - Doug Sheldon, JPL*
1:50 PM		*Candidate CubeSat Processors - Steve Guertin, JPL*
2:10 PM		*Candidate CubeSat Power Devices - Leif Scheick, JPL*
2:30 PM		*Arduino/Raspberry Pi: Hobbyist Hardware and Radiation Total Dose Degradation - Daniel Violette, Uconn/NASA*
2:50 PM		Break (25 min)
3:15 PM		*Burn-In of Complex Commercial Parts - Marti McCurdy - Silicon 360*
4:00 PM	*Panel and Concepts*	*Panel: The "Right" Power Architecture for CubeSats - led by John Shue, NASA*
4:30 PM		*Wrapup Discussion*
		End of Day 2

NEPP Overview

***NEPP provides the Agency infrastructure for assurance of EEE parts for space usage*.**

Qualification guidance
To flight projects on how to qualify

Technology Evaluation
Determine new technology applicability and qualification guidance

Standards
Ensures NASA needs are represented

Test/Qualification Methods
Evaluate improved or more cost-effective concepts

Manufacturer Qualification
Support of audits and review of qualification plans/data

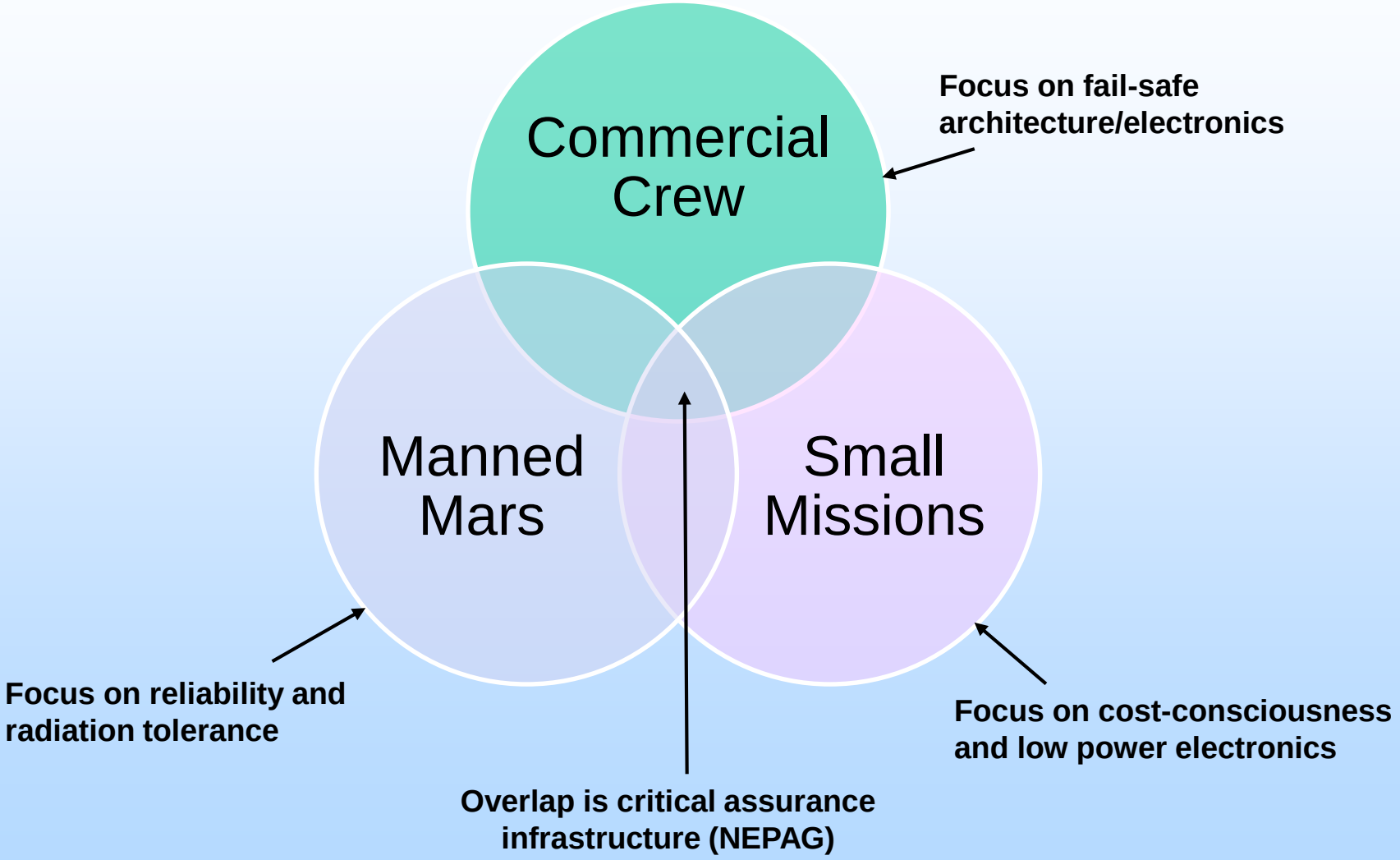
Risk Analysis
For all grades of EEE parts (commercial, automotive, military/aerospace, …)

Information Sharing
Lessons learned, working groups, website, weekly telecons

Subject Matter Expertise
SMEs for NASA programs, other agencies, industry

NEPP and its subset (NASA Electronic Parts Assurance Group – NEPAG) are the Agency's POCs for reliability and radiation tolerance of EEE parts and their packages.

Notional NEPP View of EEE Parts Needs Diversity



FY14 NEPP Core –
Automotive/Commercial Electronics (Small Missions)

Core Areas are Bubbles;
Boxes underneath are variable tasks in each core

Legend
- NEPP Ongoing Task
- FY14 New Start

NEPP Research Category – Automotive/Commercial Electronics

Automotive Electronics
- Body of Knowledge on specs, standards, and vendor approaches
- Reliability evaluation of ceramic capacitors, discrete transistors, and microcircuits

Work performed by NAVSEA Crane in collaboration

Alternate Test Approaches
- Effectiveness of Board Level Testing for Piecepart Qualification (will utilize boards with processors and microcontrollers)

Mobile Processors
- Intel Atom, Qualcomm Snapdragon Processors (radiation only)

Microcontrollers
- Freescale Automotive Microcontroller (+ board)
- Cubesat vendor Microcontrollers: Tyvak (TI microcontroller), Pumpkin (Atmel microcontroller) (radiation only)

Advanced Processors
- Freescale P5040 Network Processor (+board) (IP for next generation BAE Systems Rad Hard Processor)

Requires collaboration with Freescale

Guidance, Documents
- Rule of thumb documents
- Policy, Guidelines
- Microcontroller recommendations
- CubeSat Parts Database
- COP

FY14 NEPP Core - Complex Devices

Core Areas are Bubbles;
Boxes underneath are variable tasks in each core

Legend
- NEPP Ongoing Task
- FY14 New Start

NEPP Research Category – Complex Devices

FPGAs – Radiation
- Xilinx Virtex 5QV
- Commercial Xilinx 28nm Virtex-7, Kintex-7
- FPGA SOCs Xilinx Zynq, Microsemi SmartFusion 2
- New Microsemi and ATMEL
- Embedded Coldfire™

FPGAs – Reliability
- Xilinx Virtex 5QV Daisy Chain Package Evaluation
- FPGA SOCs Xilinx Zynq, Microsemi SmartFusion 2

Area Array Packages
- Class Y QML
- Class Y and IPC
- HALT for PBGA
- Thermal Interface Materials
- Solder Bump Comparison
- Flip Chip Interconnect

Memory Devices
- Resistive Memory (RERAM, CBRAM) Radiation, Reliability
- 3D Structure FLASH Memory Samsung VNAND Radiation, Reliability
- DDR3 Memory Radiation, Reliability

Advanced CMOS
- IBM trusted foundry 14-32 nm Radiation
- Intel 14 nm Radiation
- DARPA LEAP Program (32 nm) Radiation

Assurance
- Memory Fault Coverage
- SOC Radiation
- Synopsys TMR Tool Evaluation

FY14 NEPP Core - Power Devices

Core Areas are Bubbles;
Boxes underneath are variable tasks in each core

Legend
- NEPP Ongoing Task
- FY14 New Start

NEPP Research Category – Power Devices

- **Power Converters**
  - DC-DC Converter Working Group
  - POL SEU Susceptibility
- **Power MOSFETS – Silicon**
  - New Mil/Aero Product Evaluation (Radiation)
  - (Cubesat) Commercial Power MOSFET Evaluation (Radiation)
- **Widebandgap Power and RF**
  - Widebandgap Working Group
  - GaN Radiation Test
  - SiC Radiation Test
  - Combined Effects Reliability
- **Assurance**
  - Standards Support

FY14 NEPP Core - Assurance

Core Areas are Bubbles;
Boxes underneath are variable tasks in each core

Legend
- NEPP Ongoing Task
- FY14 New Start

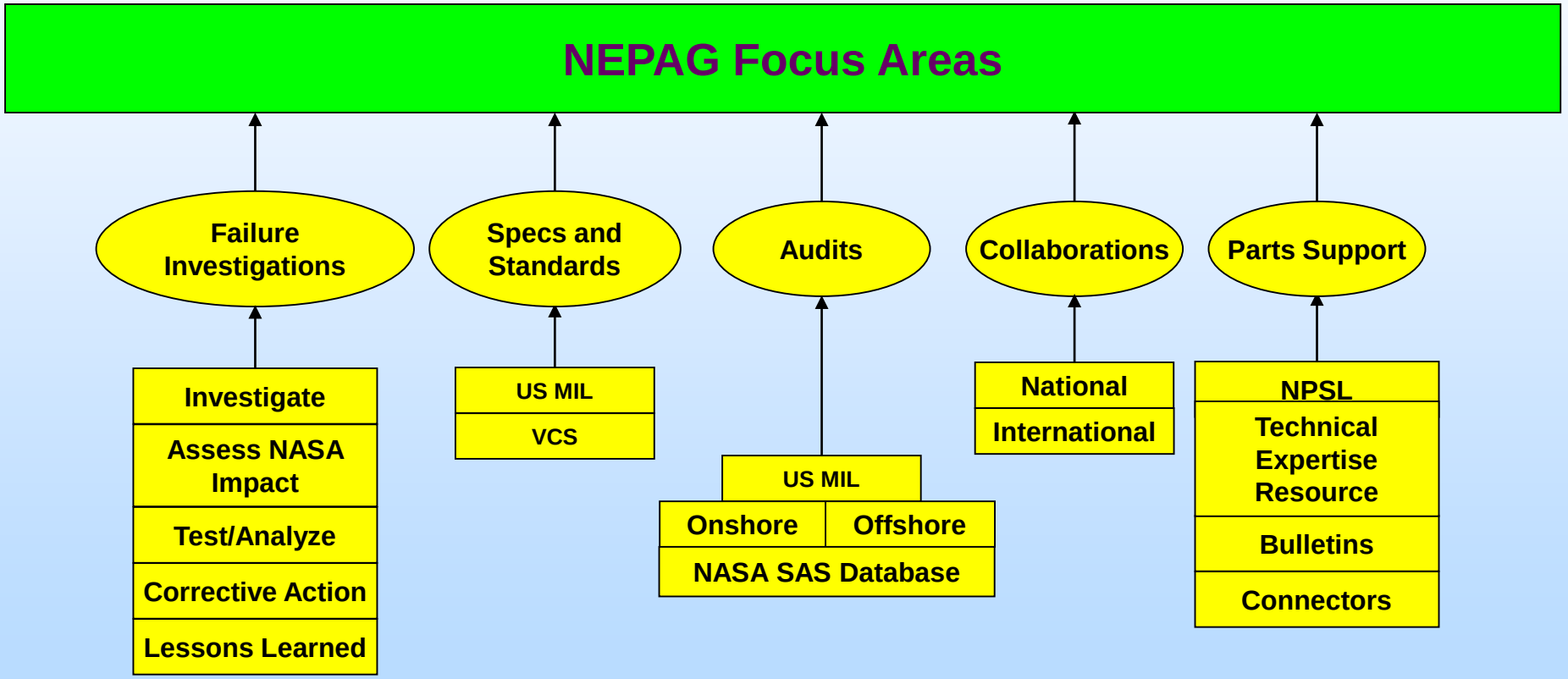
NEPP Research Category – Assurance

- **Radiation**
  - Hydrogen Effects
  - Ultra-ELDRS
  - Board level proton testing BOK
- **Parts**
  - Hermeticity
  - BME Capacitors
  - Ceramic Capacitors
  - Tantalum Capacitors
- **Packaging**
  - NEPP Roadmap Update
  - Leadless Package Trends
- **Assurance**
  - Connector Working Group
  - Low Proton Energy Test Guideline
  - NASA Parts Policy Update
  - Radiation Assurance Policy/Guidance
  - Long term Storage BOK

NASA Electronic Parts Assurance Group (NEPAG)

Core Areas are Bubbles;
Boxes underneath are elements in each core

Legend
- NEPP Ongoing Task
- FY14 New Start



Outline

- **Assurance for Electronics**
- **Commercial Off The Shelf (COTS) Usage**
- **Testing at Board/Box Level?**
- **Summary and Discussion**

Hubble Space Telescope courtesy NASA

Assurance for Electronic Devices

- ***Assurance*** **is**
  - **Knowledge of**
    - **The supply chain and manufacturer of the product,**
    - **The manufacturing process and its controls, and,**
    - **The physics of failure (POF) related to the technology.**
  - **Statistical process and inspection via**
    - **Testing, inspection, physical analyses and modeling.**
  - **Understanding the application and environmental conditions for device usage.**
    - **This includes:**
      - **Radiation,**
      - **Lifetime,**
      - **Temperature,**
      - **Vacuum, etc., as well as,**
      - **Device application and appropriate derating criteria.**

Reliability and Availability

- **Reliability (Wikipedia)**
  - **The ability of a system or component to perform its required functions under stated conditions for a specified period of time.**
- **Availability (Wikipedia)**
  - **The degree to which a system, subsystem, or equipment is in a specified operable and committable state at the start of a mission, when the mission is called for at an unknown, *i.e.,* a random, time. Simply put, availability is the proportion of time a system is in a functioning condition. This is often described as a *mission capable rate*.**
- **The question is:**
  - **Does it *HAVE* to work? Or**
  - **Do you just *WANT* it to work?**

What does this mean for EEE parts?

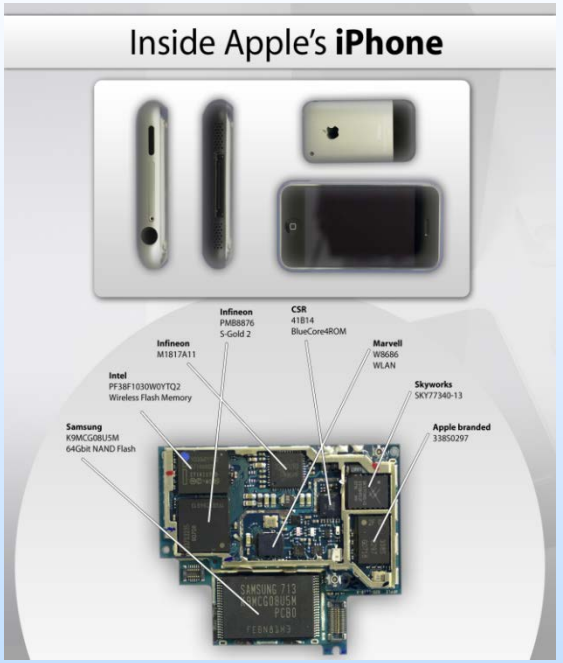
- **The more *understanding* you have of a device's failure modes and causes, the higher the *confidence* level that it will perform under mission environments and lifetime**
  - ***High confidence* = "have to work"**
    - **The key is operating without a problem when you need it to (appropriate availability over the mission lifetime)**
  - ***Less confidence* = "want to work"**
    - ***This is not saying that it won't work, just that our confidence to be available isn't as high (or even unknown)***
- **Standard Way of Doing Business**
  - **Qualification processes are statistical beasts designed to understand/remove known reliability risks and uncover unknown risks inherent in a part.**
    - **Requires significant sample size and comprehensive suite of piecepart testing (insight) – high confidence method**

Screening <> Qualification

- **Electronic component screening uses environmental stressing and electrical testing to identify marginal and defective components within a "lot" of devices.**
  - **This is opposed to *qualification* which is usually a suite of harsher tests (and often destructive) intended to fully determine reliability characteristics of the device over a standard environment/application range**
- ***Diatribe*: what is a "lot"?**
  - **For the Mil/Aero system, it is devices that come from the same wafer diffusion (i.e., silicon lot from the same wafer)**
  - **For all others, it is usually the same "packaging" date**
    - **I.e., silicon may or may not be the same, but the devices were packaged at the same time. This raises a concern often known as "die traceability".**
  - ***Device failure modes often have variance from silicon lot to silicon lot.***

The Trade Space Involved With Part Selection

- **Evolution of IC space procurement philosophy**
  - **OLD: Buy Mil/Aero Radiation Hardened Devices Only**
  - **NEW: Develop Fault /Radiation Tolerant Systems**
- **This is now systems design that involves a risk management approach that is often quite complex.**
- **For the purposes of this discussion, we shall define ICs into two basic categories**
  - ***Space-qualified – which may or may not be radiation hardened, and,***
  - ***Commercial (includes automotive)***
- **Understanding Risk and the Trade Space involved with these devices is the new key to mission success**
  - **Think size, weight, and power (SWaP), for instance**



Performance *Inside a Apple iPhone™*

Courtesy EE Times Magazine

The Challenge for Selecting ICs for Space

- **Considerations since the "old days"**
  - **High reliability (and radiation tolerant) devices**
    - **Now a *very* small market percentage**
  - **Commercial "upscreening*"**
    - **Increasing in importance**
    - **Assesses reliability, does not enhance**
  - **System level performance and risk**
    - **Hardened or fault tolerant "systems" not devices**

ADCs?
SerDes?
SDRAM?
Processor?
ASICs?
DSPs
Flash?
FPGAs?

System Designer
Trying to meet high-resolution instrument requirements AND long-life

***upscreening – performing tests/analysis on electronic parts for environments outside the intended/guaranteed range of a device**

ADC: analog-to-digital converter
SDRAM: synchronous dynamic random access memory
SerDes: serializer-deserializer
ASIC: application-specific integrated circuit
DSP: digital signal processor

Understanding Risk

- **The risk management requirements may be broken into three considerations**
  - **Technical/Design – "The Good"**
    - **Relate to the circuit designs not being able to meet mission criteria such as jitter related to a long dwell time of a telescope on an object**
  - **Programmatic – "The Bad"**
    - **Relate to a mission missing a launch window or exceeding a budgetary cost cap which can lead to mission cancellation**
  - **Radiation/Reliability – "The Ugly"**
    - **Relate to mission meeting its lifetime and performance goals without premature failures or unexpected anomalies**
- ***Each mission must determine its priorities among the three risk types***

The Risk Trade Space –
Considerations for Device Selection (Incomplete)

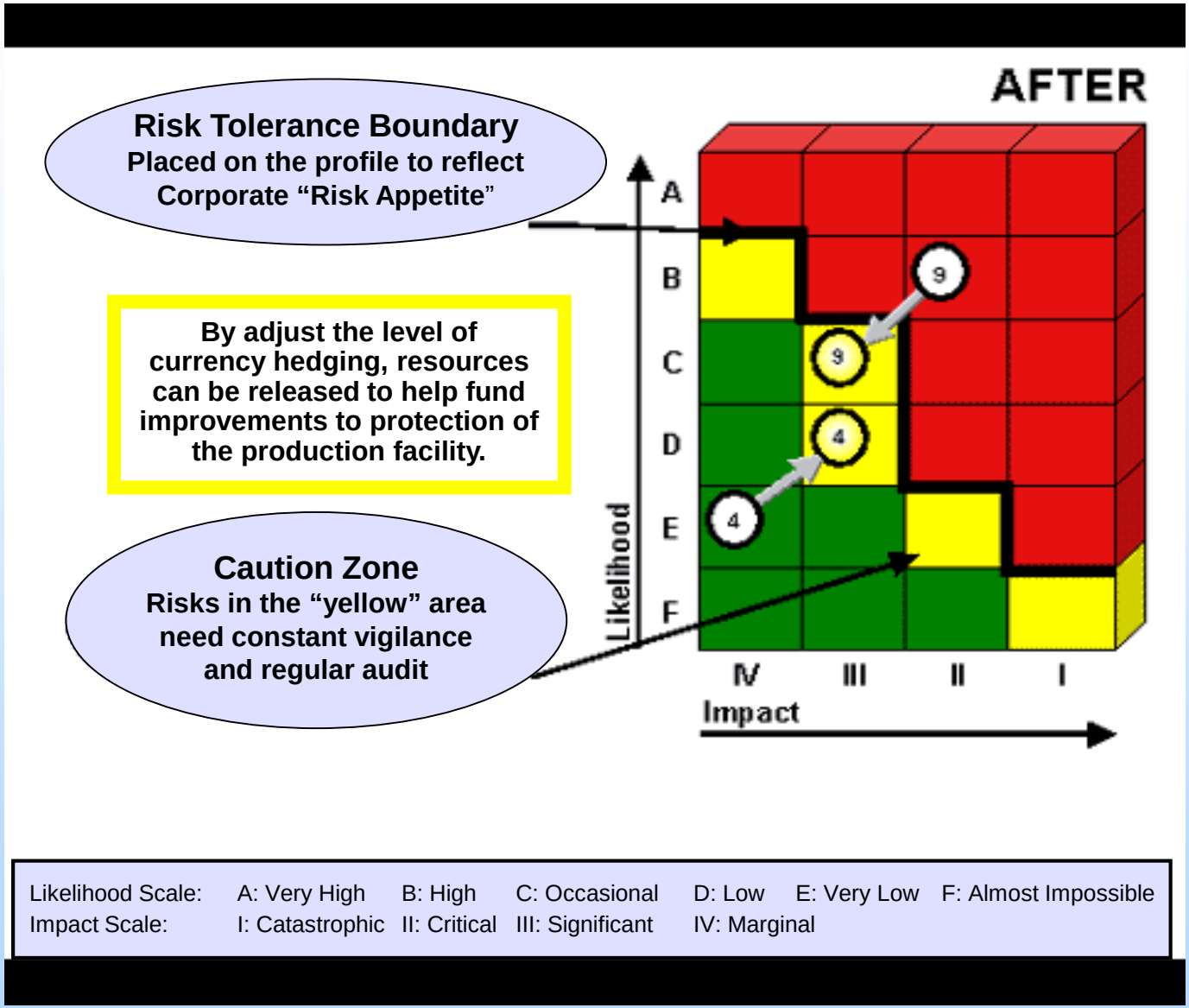
- **Cost and Schedule**
  - Procurement
  - NRE
  - Maintenance
  - Qualification and test
- **Performance**
  - Bandwidth/density
  - SWaP
  - System function and criticality
  - Other mission constraints (*e.g.*, reconfigurability)
- **System Complexity**
  - Secondary ICs (and all their associated challenges)
  - Software, etc…
- **Design Environment and Tools**
  - Existing infrastructure and heritage
  - Simulation tools
- **System operating factors**
  - Operate-through for single events
  - Survival-through for portions of the natural environment
  - Data operation (example, 95% data coverage)
- **Radiation and Reliability**
  - SEE rates
  - Lifetime (TID, thermal, reliability,…)
  - "Upscreening"
- **System Validation and Verification**

NRE: non-recurring engineering
IC: integrated circuit
SEE: single-event effect
TID: total ionizing dose

Systems Engineering and Risk

- **The determination of acceptability for device usage is a complex trade space**
  - **Every engineer will "solve" a problem differently**
    - **Ex., approaches such as synchronous digital circuit design may be the same, but the implementations are not**
- **A more omnidirectional approach is taken weighing the various risks**
  - **Each of the three factors may be assigned weighted priorities**
    - **The systems engineer is often the "person in the middle" evaluating the technical/reliability risks and working with management to determine acceptable risk levels**

Traditional Risk Matrix



NASA and COTS

- **NASA has been a user of COTS electronics for decades, *typically* when**
  - **Mil/Aero alternatives are not available (performance or function or procurement schedule),**
  - **A system can assume possible unknown risks, and,**
  - **A mission has a relatively short lifetime or benign space environment exposure.**
- **In most cases, some form of "upscreening" has occurred.**
  - **A means of assessing a portion of the inherent reliability of a device.**
  - **Discovering that a COTS device fails during upscreening has occurred in almost every flight program.**
- ***Note: CubeSats may NOT necessarily use this model.***

Notional EEE Parts Usage Factors

Environment/Lifetime

Criticality

	Low	Medium	High
Low	COTS upscreening/ testing optional; do no harm (to others)	COTS upscreening/ testing recommended; fault-tolerance suggested; do no harm (to others)	Rad hard suggested. COTS upscreening/ testing recommended; fault tolerance recommended
Medium	COTS upscreening/ testing recommended; fault-tolerance suggested	COTS upscreening/ testing recommended; fault-tolerance recommended	Level 1 or 2, rad hard suggested. Full upscreening for COTS. Fault tolerant designs for COTS.
High	Level 1 or 2 suggested. COTS upscreening/ testing recommended. Fault tolerant designs for COTS.	Level 1 or 2, rad hard suggested. Full upscreening for COTS. Fault tolerant designs for COTS.	Level 1 or 2, rad hard recommended. Full upscreening for COTS. Fault tolerant designs for COTS.

Comments on the "Matrix" Wording

- **"Optional" – implies that you might get away without this, but there's risk involved.**
- **"Suggested" – implies that it is good idea to do this.**
- **"Recommended" – implies that this really should be done.**
- **Where just the item is listed (like "full upscreening on COTS") – this should be done to meet the criticality and environment/lifetime concerns.**

Good mission planning identifies where on the matrix it lies.

"How to Save on EEE Parts for a Payload on a Budget and Be Reliable"

- **First and foremost: *SCROUNGE***
  - **Are there spare devices available at either your Center or elsewhere at the Agency?**
    - **NASA has already bought devices ranging from passives to FPGAs.**
  - **Some may be fully screened and even be radiation hardened/tested.**
    - **You may still have to perform some additional tests, but it's cheaper than doing them all!**
- **Engage parts/radiation engineers early to help find and evaluate designers "choices".**
  - **Use their added value to help with the choices and even on fault tolerance approaches – you'll need them to "sign off" eventually.**
- **If you can't find spares, try to use parts with a "history".**
  - **At a minimum, the hope is that your lot will perform similarly to the "history" lot – not guaranteed.**
  - **Even riskier, choose devices built on the same design rules by the same company (i.e., different part, but on the same process/design as a part with "history").**
- **If you absolutely need something new, you will pay for the qualification or take the risk.**

Brief Diatribe:
Add Fault Tolerance or Radiation Hardening?

- **Means of making a system more "reliable/available" can occur at many levels**
  - **Operational**
    - **Ex., no operation in the South Atlantic Anomaly (proton hazard)**
  - **System**
    - **Ex., redundant boxes/busses or swarms of nanosats**
  - **Circuit/software**
    - **Ex., error detection and correction (EDAC) scrubbing of memory devices by an external device or processor**
  - **Device (part)**
    - **Ex., triple-modular redundancy (TMR) of internal logic within the device**
  - **Transistor**
    - **Ex., use of annular transistors for TID improvement**
  - **Material**
    - **Ex., addition of an epi substrate to reduce SEE charge collection (or other substrate engineering)**

Good engineers can invent infinite solutions,
but the solution used must be adequately validated

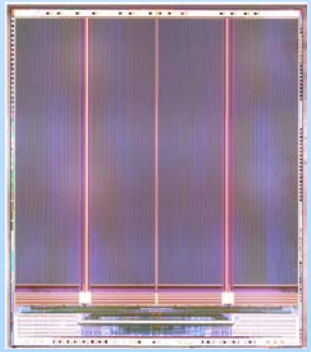
Discussion: Is knowledge of EEE Parts Failure Modes Required To Build a Fault Tolerant System?

- **This is NOT to say that the system won't work without the knowledge, but do we have adequate confidence in the system to work when we need it to?**
  - **What are the "unknown unknowns"? Can we account for them?**
  - **How do you calculate risk with unscreened/untested EEE parts?**
  - **Do you have common mode failure potential in your design? (i.e., a identical redundant string rather than having independent redundant strings)**
  - **How do you adequately validate a fault tolerant system for space?**
- **If we go back to the "Matrix", how critical is your function and harsh your environment/lifetime? This will likely drive your implementation "answers".**

Example:
Is Radiation Testing Always Required for COTS?

- **Exceptions for testing may include**
  - **Operational**
    - **Ex., The device is only powered on once per orbit and the sensitive time window for a single event effect is minimal**
  - **Acceptable data loss**
    - **Ex., System level error rate may be set such that data is gathered 95% of the time. This is data availability. Given physical device volume and assuming every ion causes an upset, this worst-case rate may be tractable.**
  - **Negligible effect**
    - **Ex., A 2 week mission on a shuttle may have a very low Total Ionizing Dose (TID) requirement. TID testing could be waived.**

Memory picture courtesy
NASA, Code 561



A flash memory may be acceptable without testing if a low TID requirement exists or not powered on for the large majority of time.

Summary

- **In this talk, we have presented:**
  - **An overview of NEPP as well as considerations for selection of ICs focusing on COTS for space systems.**
    - **Technical, programmatic, and risk-oriented**
      - **As noted, every mission may view the relative priorities between the considerations differently.**
- **As seen below, every decision type may have a process.**
  - **It's all in developing an appropriate one for your application and avoiding "buyer's remorse"!**

Five stages of Consumer Behavior

http://www-rohan.sdsu.edu/~renglish/370/notes/chapt05/

Backup Slides

IC Selection Requirements

- **To begin the discussion, we shall review IC selection from three distinct and often contrary perspectives**
  - **Performance,**
  - **Programmatic, and,**
  - **Reliability.**
- **Each of these will be considered in turn, however, one must ponder all aspects as part of the *process***

Graphic courtesy
http://www.shareworld.co/

Performance Requirements

- **Rationale**
  - **Trying to meet science, surveillance, or other performance requirements**
- **Personnel involved**
  - **Electrical designer, systems engineer, other engineers**
- **Usual method of requirements**
  - **Flowdown from science or similar requirements to implementation**
    - **i.e., ADC resolution or speed, data storage size, etc…**
- **Buzzwords**
  - **MIPS/watt, Gbytes/cm^3, resolution, MHz/GHz, reprogrammable**
- **Limiting technical factors beyond electrical**
  - **Size, weight, and power (SWaP)**

Race Car courtesy
http://wot.motortrend.com/

MIPS: millions of instructions per second

Programmatic Requirements and Considerations

- **Rationale**
  - **Trying to keep a program on schedule and within budget**
- **Personnel involved**
  - **Project manager, resource analyst, system scheduler**
- **Usual method of requirements**
  - **Flowdown from parent organization or mission goals for budget/schedule**
    - **I.e., Launch date**
- **Buzzwords**
  - **Cost cap, schedule, critical path, risk matrix, contingency**
- **Limiting factors**
  - **Parent organization makes final decision**

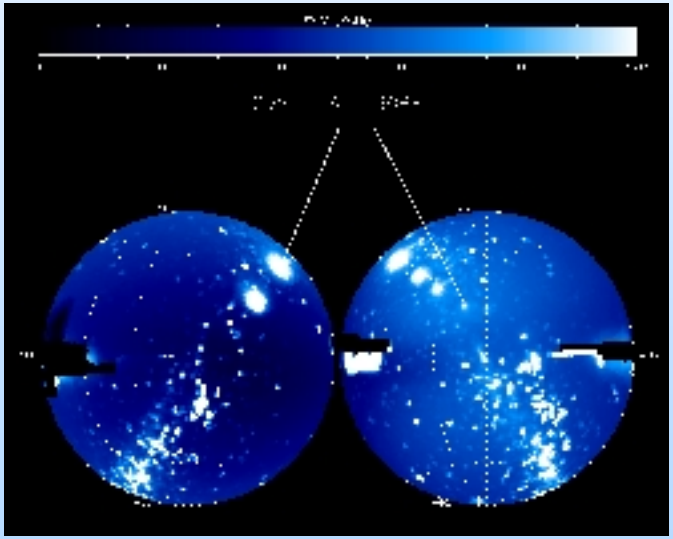
Burroughs Accounting Machine courtesy
http://www.piercefuller.com/collect/before.html

Programmatics

A numbers game

Risk Requirements

- **Rationale**
  - **Trying to ensure mission parameters such as reliability, availability, operate-through, and lifetime are met**
- **Personnel involved**
  - **Radiation engineer, reliability engineer, parts engineer**
- **Usual method of requirements**
  - **Flowdown from mission requirements for parameter space**
    - **I.e., SEU rate for system derived from system availability specification**
- **Buzzwords**
  - **Lifetime, total dose, single events, device screening, “waivers”**
- **Limiting factors**
  - **Management normally makes “acceptable” risk decision**



SOHO/SWAN Ultraviolet Image courtesy
http://sohowww.nascom.nasa.gov/gallery/Particle/swa008.html

An Example “Ad hoc” Battle

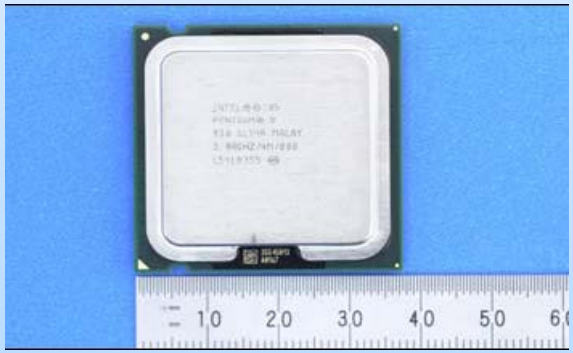
- **Mission requirement: High resolution image**
  - **Flowdown requirement: 14-bit 100 Msps ADC**
    - **Usually more detailed requirements are used such as Effective Number of Bits (ENOB) or Integral Non-Lineariy (INL) or Differential Non-Linearity (DNL) as well**
  - **Designer**
    - **Searches for available radiation hardened ADCs that meet the requirement**
    - **Searches for commercial alternatives that could be upscreened**
    - **Looks at fault tolerant architecture options**
  - **Manager**
    - **Trades the cost of buying Mil-Aero part requiring less aftermarket testing than a purely commercial IC**
    - **Worries over delivery and test schedule of the candidate devices**
  - **Radiation/Parts Engineer**
    - **Evaluates existing device data (if any) to determine reliability performance and additional test cost and schedule**
- **The best device? Depends on mission priorities**

Why COTS?
The Growth in Integrated Circuit Availability

- **The semiconductor industry has seen an explosion in the types and complexity of devices that are available over the last several decades**
  - **The commercial market drives features**
    - **High density (memories)**
    - **High performance (processors)**
    - **Upgrade capability and time-to-market**
      - **Field Programmable Gate Arrays (FPGAs)**
    - **Wireless (Radio Frequency (RF) and mixed signal)**
    - **Long battery life (Low-power Complementary Metal Oxide Semiconductors (CMOS))**

Integrated Cycling Bib and MP3

Zilog Z80 Processor
circa 1978
8-bit processor



Intel 65nm Dual Core Pentium D Processor
circa 2007
Dual 64-bit processors

Processor pictures courtesy NASA, Code 561

FPGA: field programmable gate array
RF: radio frequency
CMOS: complementary metal oxide semiconductor

The Changes in Device Technology

- **Besides increased availability, many changes have taken place in**
  - **Base technology,**
  - **Device features, and,**
  - **Packaging**
- **The table below highlights a few selected changes**

DIP: dual in-line package
LCC: leaded chip carrier
FCBGA: flip chip ball grid array
SOI: silicon on insulator

Feature	circa 1990	circa 2007
Base technology	bulk CMOS/NMOS	CMOS with strained Si or SOI
Feature size	> 2.0 um	65 nm
Memory size - volatile (device)	256 kb	1 Gb
Processor speed	64 MHz	> 3 GHz
FPGA Gates	2k	> 1M
Package	DIP or LCC - 40 pins	FCBGA - 1500 balls
Advanced system on a chip (SOC) features	Cache memory	>Gbps Serial Link, Serdes, embedded processors, embedded memory

- ***Now commercial technology is pushing towards 14nm, 3D transistors, and substrates, etc…***

Evaluation Method of Commercial Off-the-Shelf (COTS) Electronic Printed Circuit Boards (PCBs) or Assemblies

CompactPCI™

ZIATECH CORPORATION

We can test devices,

but how do we test systems?

Or better yet, systems of systems on a chip (SOC)?

Sample Challenges for the Use and Testing of COTS PCBs:

- **Limited parts list information**
  - **Bill-of-materials often does NOT include lot date codes or manufacturer of device information**
  - **Die or in some cases lack of information on "datasheets"**
  - **Full PCB datasheet may not have sufficient information on individual device usage**
  - **The possibility of IC variances for "copies" of the "same" PCBs:**
    - **Form, fit, and function doesn't equal same device from same manufacturer**
    - **Lot-to-lot, device-to-device variance**
- **The limited testability of boards due to complex circuitry, limited IO, and packaging issues ("*visibility*" issues) as well as achieving full-range thermal/voltage acceleration. This includes "fault coverage".**
- **The issue of piecepart versus board level tests**
  - **Board performance being monitored, not device**
  - **Error/fault propagation often time and application dependent**
- **The inability to simulate the space radiation environment with a single particle test**
  - **Potential masking of faults during radiation exposure (too high a particle rate or too many devices being exposed simultaneously)**
- **Statistics are often limited due to sample size**