Ultra-Scaled CMOS
Radiation Performance


Radiation Effects and Analysis Group
NASA Goddard Space Flight Center
Greenbelt, MD 20771 USA
Introduction

- Ultra-scaled CMOS includes commercial foundry capabilities at and below the 90 nm technology node
- Evaluations take place using standard products and test characterization vehicles (memories, logic/latch chains, etc.)
- NEPP focus is two-fold:
  - Conduct early radiation evaluations to ascertain viability for future NASA missions – leverage commercial technology development
  - Uncover gaps in current testing methodologies and mechanism comprehension – early risk mitigation
Introduction

- Large source of collaboration with external partners:
  - Corporate
    - Cypress Semiconductor
    - IBM Corporation
    - Intel Corporation
    - Texas Instruments
    - STMicroelectronics
  - Government
    - Naval Research Laboratory
    - Sandia National Laboratories
  - University
    - Vanderbilt University
    - The Georgia Institute of Technology
    - Auburn University
    - Arizona State University
Introduction

Cypress
- 90 nm CMOS
- 65 nm CMOS

IBM
- 65 nm SOI
- 45 nm SOI
- 32 nm SOI

IBM
- 65 nm SOI
- 45 nm SOI
- 32 nm SOI

Texas Instruments
- 65 nm CMOS
- 45 nm CMOS

STMicroelectronics
- 65 nm CMOS

Intel
- 65 nm CMOS
- 45 nm CMOS
- 32 nm CMOS

NASA/GSFC REAG
Scaled CMOS

Description:

- Continue task to evaluate scaled CMOS technologies (< 100 nm) from Cypress Semiconductor, IBM, Intel, Texas Instruments, and STMicroelectronics using state-of-the-art test vehicles and products, and
- Determine inherent single-event effects (SEE) tolerance of Trusted Access Program Office (TAPO) product flows, and
- Identify challenges for future SEE hardening efforts
- Investigate new SEE failure mechanisms and effects, and
- Provide data to NASA/DTRA modeling programs.
- Testing covers both destructive and non-destructive SEE using heavy ion and protons
- Recent emphasis has been on low-energy proton soft errors induced by direct ionization

FY10 Plans:

- Cypress: evaluate heavy ion data from 65 nm quad data rate SRAM; conduct heavy ion and possible pulsed laser evaluation of 90 nm non-volatile SRAM.
- IBM: continue analysis of FY09 45 nm SOI SRAM data to assess role of proton direct ionization soft errors (both single and multi-bit); extend accelerated ground tests to 45 nm SOI latches; employ cold laser ablation and XeF₂ to yield advanced flip-chip sample preparation for low-energy protons and pulsed laser testing; extend studies to 32 nm SOI when available.
- Intel: continue evaluation of test articles as available
- TI: continue comparison of 65 and 45 nm data; support Vanderbilt efforts to gather SEL and exotic particle SEU data; support modeling efforts.
- STMicro: develop test set for 65 nm test characterization vehicle.

Schedule:

- All tasks are currently ongoing
- Diamonds indicate completed or scheduled tests

Deliverables:

- Quarterly status reports to NEPP/DTRA
- Test reports
- Updates to lessons learned
- Presentations at leading technical conferences
- Publications in refereed journals
Goals

• Cypress Semiconductor
  – Complete design of 90 nm CMOS non-volatile SRAM test sets
  – Collect initial SEE data sets – heavy ion and pulsed laser

• IBM Corporation
  – Gather first heavy ion and proton data sets on 45 nm SOI latches
  – Analyze low-energy proton and alpha particle data for latches and SRAM

• Texas Instruments
  – Continue investigation of layout dependence on heavy ion SEL in 45 nm CMOS
  – Support additional accelerated tests to aid modeling efforts
Goals

- **Intel Corporation**
  - Work with vendor to develop and perform radiation tests for 32 nm CMOS technology

- **STMicroelectronics**
  - Develop test set for 65 nm CMOS test vehicle
  - Identify appropriate tests for provided hardware
Expected Impact to Community

• Encourage early-adoption of advanced technologies
  – Promote technology development and leverage non-recurring engineering

• Identify new failure mechanisms
  – Reduce risk
  – Refine test methodologies and standards

• Strengthen existing and foster new relationships with industry
  – Maintain proactive (not reactive) stance for the radiation community
Status/Schedule

- **Cypress Semiconductor**
  - Completed data analysis of 90 nm, 4 Mbit asynchronous SRAM (FY09 TAMU data)
  - Completed initial heavy ion test of 4 Mbit non-volatile SRAM (FY10 LBNL data)
- **IBM Corporation**
  - Completed 45 nm SOI latch test set design
  - Completed initial 45 nm SOI latch heavy ion test (FY10 TAMU)
  - Completed initial 45 nm SOI proton test (FY10 IUCF)
  - Completed follow-up heavy ion testing of 45 nm SOI latches, including RHBD variant (FY10 LBNL)
- **Texas Instruments**
  - Completed initial heavy ion SEL analysis (FY09 TAMU & LBNL) on 45 nm CMOS
  - Supported initial tests at TRIUMF (FY10) on 45 nm CMOS
Status/Schedule

• Intel Corporation
  – Continuing discussions with Intel to gain access to 32 nm hardware
  – Radiation testing looks likely for FY10Q4

• STMicroelectronics
  – Completed initial conversations regarding 65 nm CMOS hardware test articles
Technical Highlights
45 and 65 nm Texas Instruments CMOS

- Proton single-event effects cover energies over several orders of magnitude; need to use multiple facilities
- Additional testing complications at low-energy


Traditional models fail to predict scaled device response – need detailed radiation transport and updated hardness assurance guidelines
Technical Highlights
45 and 65 nm IBM SOI CMOS SRAM

• Completed initial heavy ion and proton characterization


Demonstrated similarity between 65 and 45 nm SOI and confirmed low-energy proton direct ionization effects in both technologies.
Technical Highlights

*Direct Ionization* Rates for Scaled CMOS

- Upset model based on a 45 nm SOI SRAM
- Rates calculated based on direct ionization
- Detailed radiation transport with accurate physics
- Several types of space radiation environments are dominated by proton effects

Accurate radiation transport captures low-energy proton soft errors – can dominate rates in some environments

M. A. Xapsos et al., 2010 SEE Symposium, San Diego, CA.
Technical Highlights

45 nm IBM SOI CMOS Latches

- Five latch chains of varying length
- Three of the five chains are SEE-hardened designs
- Irradiation is topside, through the back end of line
- Tests able to reuse 65 nm IBM SOI SRAM test board

Logical progression from SRAM testing – make use of dynamic testing, which is critical for application evaluation
Technical Highlights
90 nm Cypress CMOS

- Heavy ion testing at LBNL
- Good flow of data and information between Cypress and GSFC
- Data analysis shared between GSFC and Cypress

90 nm CMOS non-volatile SRAM

Evaluating unique commercial products for possible NASA use
FY10 Publications

Single-Event Upsets and Multiple-Bit Upsets on a 45 nm SOI SRAM

David F. Heidel, Senior Member, IEEE, Paul W. Marshall, Member, IEEE, Jonathan A. Pellish, Member, IEEE, Kenneth P. Rodbell, Senior Member, IEEE, Kenneth A. LaBel, Member, IEEE, James R. Schwank, Fellow, IEEE, Stewart E. Rauch, Senior Member, IEEE, Mark C. Hakey, Melanie D. Berg, Member, IEEE, Carlos M. Castaneda, Member, IEEE, Paul E. Dodd, Senior Member, IEEE, Mark R. Friendlich, Anthony D. Phan, Christina M. Seidleck, Marty R. Shaneyfelt, Fellow, IEEE, and Michael A. Xapsos, Senior Member, IEEE

Impact of Low-Energy Proton Induced Upsets on Test Methods and Rate Predictions

Brian D. Sierawski, Member, IEEE, Jonathan A. Pellish, Member, IEEE, Robert A. Reed, Senior Member, IEEE, Ronald D. Schrimpf, Fellow, IEEE, Kevin M. Warren, Member, IEEE, Robert A. Weller, Senior Member, IEEE, Marcus H. Mendenhall, Member, IEEE, Jeffrey D. Black, Member, IEEE, Alan D. Tipton, Member, IEEE, Michael A. Xapsos, Member, IEEE, Robert C. Baumann, Member, IEEE, Xiaowei Deng, Member, IEEE, Michael J. Campola, Member, IEEE, Mark R. Friendlich, Hak S. Kim, Anthony M. Phan, and Christina M. Seidleck

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Significant published work on low-energy proton effects presented at the 2009 Nuclear and Space Radiation Effects Conference
Heavy Ion Testing with Iron at 1 GeV/amu

Jonathan A. Pellish, Member, IEEE, Michael A. Xapsos, Senior Member, IEEE, Kenneth A. LaBel, Member, IEEE, Paul W. Marshall, Member, IEEE, David F. Heidel, Senior Member, IEEE, Kenneth P. Rodbell, Senior Member, IEEE, Mark C. Hakey, Paul E. Dodd, Senior Member, IEEE, Marty R. Shaneyfelt, Fellow, IEEE, James R. Schwank, Fellow, IEEE, Robert C. Baumann, Member, IEEE, Xiaowei Deng, Member, IEEE, Andrew Marshall, Member, IEEE, Brian D. Sierawski, Member, IEEE, Jeffrey D. Black, Member, IEEE, Robert A. Reed, Senior Member, IEEE, Ronald D. Schrimpf, Fellow, IEEE, Hak S. Kim, Member, IEEE, Melanie D. Berg, Member, IEEE, Michael J. Campola, Member, IEEE, Mark R. Friendlich, Christopher E. Perez, Member, IEEE, Anthony M. Phan, and Christina M. Seidlek

Submitted for publication in IEEE Transactions on Nuclear Science

First use of the NASA Space Radiation Laboratory at Brookhaven National Lab for ultra-scaled CMOS
FY10 Presentations

  – Presented by M. A. Xapsos et al. at the 2010 SEE Symp., La Jolla, CA.


FY10 Presentations


Plans (FY10/FY11)

- Cypress Semiconductor
  - Continue analysis of 65 nm QDR SRAM data (FY10Q3-Q4)
    - Possible proton testing in FY10Q4
  - Continue dialog with Cypress to obtain new hardware (FY10Q3-Q4, FY11)
  - Begin analysis of 90 nm non-volatile SRAM data (FY10Q3-Q4)

- IBM Corporation
  - Continue SRAM and latch data analysis (FY10Q3-Q4, FY11)
  - Perform low-energy proton and $^4$He tests at UC Davis on latches and SRAM (FY10Q3)
  - Perform additional heavy ion tests at TAMU on latches (FY10Q4)

- Intel Corporation
  - Obtain 32 nm hardware and begin development of test sets for TID, dose rate, and proton evaluation (FY10Q3-Q4)
  - Perform radiation testing (FY10Q3-Q4, FY11)
Plans (FY10/FY11)

• **STMicroelectronics**
  - Obtain 65 nm CMOS test characterization vehicle (FY10Q3-Q4)
  - Begin identification of test sites and development of test sets for TID and SEE evaluation (FY10Q3-Q4)
  - Perform radiation tests (FY10Q4, FY11)

• **Texas Instruments**
  - Continue to support analysis of TAMU and LBNL SEL data (FY10Q3-Q4)
  - Support additional testing and modeling efforts as necessary (FY10Q3-Q4, FY11)