FPGA - Overview of JPL Efforts under NEPP

Dr. Douglas Sheldon
Jet Propulsion Laboratory
California Institute of Technology

Overview

• Introduction
• Technology
• Radiation
• Packaging
• Applications
• Software
• Future
Introduction

- JPL/NEPP FPGA efforts are focused on:
  - Technology qualification
  - Risk management
  - Packaging qualification and development
  - Guideline development
  - Agency wide support for community development
FPGAs at NASA

• FPGAs represent the main VLSI technology driving force for all NASA missions.

• All current generation and future generation spacecraft will have literally dozens of FPGAs on board doing a wide variety of tasks.
  – MSL – 60+ FPGAs
    • Bus control, telemetry, encoders, telecom, NVM, algorithms

• Concerns/opportunities:
  – New materials qualification and reliability
  – Power management
  – High bandwidth communication related issues
  – Single event/soft error mitigation schemes
  – Programming vulnerabilities
Worldwide Semiconductor Market 2011

Total Semiconductors $325.2B

Integrated Circuits $269.6B
- Memory $68.8B
- Micro $65.8B
- Logic $82.9B
- Standard Logic & Display Drivers $8.0B
- PLD $5.1B

Discrete, Sensors & Optoelectronic $55.6B
- ASIC $11.8B
- ASSP $58.0B

Source: iSuppli, March 2011

PLD = Programmable Logic Devices/FPGAs
Technology
Technology Node vs. Year of Introduction

- Space users are many generations behind in FPGA technology
- New technology issues for space community are ‘old’ for commercial community
Space FPGA Technology

• Currently RTAX is latest generation in flight
  – 150nm/7 layer AlCu:TiN/~3nm tox/antifuse
  – Custom designs for life test/burn evaluation and antifuse qualification
What’s next for Space FPGA Technology?

<table>
<thead>
<tr>
<th>Technology node</th>
<th>Name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>130nm</td>
<td>RTP3</td>
<td>Flash</td>
</tr>
<tr>
<td>90nm</td>
<td>Virtex 4</td>
<td>SRAM</td>
</tr>
<tr>
<td>65nm</td>
<td>Virtex 5</td>
<td>SRAM</td>
</tr>
<tr>
<td>65nm</td>
<td>RTP4</td>
<td>Flash</td>
</tr>
</tbody>
</table>

- Use of flash and 90nm and below technologies introduce significant new qualification and reliability issues.
- What’s the methodology to do this...?
FPGA Technology Qualification Methodology

Three main areas for emphasis

**Technology**
- Wafer Level Reliability
- Intrinsic Life
- Parametric
- Radiation Tolerance

**Design**
- Performance
- Screening
- Extrinsic Defect Control
- Radiation Mitigation

**Package**
- Materials
- Screening
- Manufacturability
FPGA Technology Qualification Methodology

- Fabless FPGA companies and wafer fabs have a unique relationship for technology qualification*.
- Each has responsibilities and both must share at the same time.
- Space community is additional partner in the qualification relationship.
  - *We can’t do most of these tasks, yet we must understand them and influence them where we need to.*

<table>
<thead>
<tr>
<th></th>
<th>Infant Mortality - Extrinsic Failures</th>
<th>Long Term Life - Intrinsic Failures</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Wafer Fab</strong></td>
<td>• Defect Reduction</td>
<td>• Wear out data/models</td>
</tr>
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<td></td>
<td>• Excursion Prevention</td>
<td>• WLR testing</td>
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<td></td>
<td>• Outlier elimination</td>
<td>• Process standardization</td>
</tr>
<tr>
<td><strong>Joint Fab-Fabless</strong></td>
<td>• Wafer parametric limits</td>
<td>• Wafer failure criterion</td>
</tr>
<tr>
<td></td>
<td>• Yield acceptance limits</td>
<td>• Process customization</td>
</tr>
<tr>
<td><strong>Fabless Design</strong></td>
<td>• Defect Isolation</td>
<td>• Use conditions &amp; wear out rules</td>
</tr>
<tr>
<td></td>
<td>• Product level screening/BI</td>
<td>• Design for reliability</td>
</tr>
<tr>
<td><strong>Space community</strong></td>
<td>• Custom BI/screening</td>
<td>• Product reliability characterization</td>
</tr>
<tr>
<td></td>
<td>• Custom designs for reliability/radiation evaluation</td>
<td>• Derating</td>
</tr>
<tr>
<td></td>
<td>• Custom designs for reliability/radiation evaluation</td>
<td>• Mission specific requirements</td>
</tr>
<tr>
<td></td>
<td>• Additional reliability/radiation testing</td>
<td>• Additional reliability/radiation testing</td>
</tr>
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</table>

*S. Y. Pai, ‘Reliability Framework in a Fabless-Foundry Environment”, IRPS 2009*
FPGA Technology Reliability Issues

http://stanford-online.stanford.edu/sesi04moore/docs/LowKDielectics4.pdf
Technology qualification highlights:
- Lot requirements
- Derating
- Mission definition of failure
- Test structures and analysis

UMC 90nm PMOS NBTI Lifetime
6-8MV/cm @ 125C

UMC 90nm EM Lifetime
20% delta R

“Virtex-4, Aerospace and Defense UMC-12A
90 nm” - Xilinx

<10yrs life at high Tj
Foundry Differences – Virtex 5

Intermetal Dielectric Differences

- CVD vs. Spin-On ILD/ UMC vs. Toshiba
- UMC - CVD carbon-doped oxide (SiOC) in M1-M6
- Toshiba - SiLK is used at the M1 – M6 levels
- SiLk $k \approx 2.65$ vs. CVD $k \approx 2.8-3.0$
- Subtle foundry differences can have possible significant impact on long duration, high reliability missions – particularly packaging

Flash Based FPGA

- Non-volatile and reprogrammable/Low power/Rad tolerant
- Flash based interconnection is new to space applications
- Two transistor (2-T) cell with common floating gate between two devices
- The “Switch” device is used as the configuration switch in the FPGA fabric.
- The “Sense” device is used to program the cell as well as for sensing the threshold voltage of the switch.
Flash FPGA Technology Qualification

- Flash cell reliability driven by electric field and temperature.
- Flash devices have data retention and endurance as new failure mechanisms that need to be included into overall FPGA qualification plan.
  - 50% P/E cycle limit + 1,000 HTOL?
  - Flash memory devices require error correction and wear leveling to ensure reliability as densities have scaled. Same concerns here?
  - Temperature dependence of program/erase operation?
  - The behavior of individual bits can dominate reliability.
New Technology Development Issues are just getting started

- FPGAs are now technology drivers for top tier commercial foundries.
- We have many exciting new technologies to look forward to!
Recent Radiation Results
FPGA Technology

Greg Allen - JPL
Introduction

• Historically, reconfigurable FPGAs have had relatively sensitive radiation responses
  – Altera (SEL)
  – Actel (TID/SEU)
  – Xilinx (SEU/SEFI)

• The aerospace community has traditionally used one time programmable FPGAs (e.g. antifuse) due to relative SEE/TID robustness
  – Increasing interest in recent years to implement reconfigurable devices (Xilinx QR in particular)
  – Lead to challenges in mitigation, verification, and system error rate calculations
Goals

• Full static radiation characterization of the Xilinx XQR5VFX130 SIRF device in conjunction with the Xilinx Radiation Test Consortium
  – Provide a methodology for NASA missions to determine error rates and mitigation methodologies (as necessary)

• Evaluate other reconfigurable FPGA vendors for SEE/TID
  – SiliconBlue iCE65
  – Altera Stratix IV/Stratix V

• Evaluate non-volatile memory products as available
  – SONOS devices
  – Mitigated flash
SEE Mitigation—TMR and RHBD

- **EDAC (Virtex-4)**
  - TMR and scrubbing
    - Complicated implementation
    - Increased engineering cost
    - Complicated verification and error rate calculation

- **RHBD (Virtex-5)**
  - Transparent implementation from the designer perspective
  - Complex radiation response requires new flight qualification methodologies
General FPGA Radiation Effects Evaluation Path

- Single-Event Latchup
- Static Characterization (Heavy Ion/Proton)
  - Configuration Elements, RAM, Registers, and Device-Level Single-Event Functional Interrupt
- Total Ionizing Dose Susceptibility
- IP Block Characterization (Dynamic Testing)
  - Clock Management, I/O, Processors, Multipliers, etc.
Moving from Virtex-II/Virtex-4 SEE Verification to Virtex-5

• Previous Virtex devices’ error rate was dominated by static elements (namely configuration and BRAM cells).

• A general outline for developing a mitigation scheme is outlined below:
  – What is the underlying, unmitigated system error rate?
    • Fault injection, accelerator testing, or software estimation
  – What is the probability of observing an error?
    • Error rate and operating period
  – What is the level of mitigation that is going to be required?
    • Engineering vs. reliability
  – What level of configuration correction is going to be required?
    • Level of error persistence
  – How will this mitigation scheme be verified?
    • Fault injection or accelerator testing

Enabling, yet SEU sensitive devices, require complex upset mitigation to use in most cases
Moving from Virtex-II/Virtex-4 SEE Verification to Virtex-5

- Virtex-5 RHBD has virtually removed the static elements from the error model. Now dominated by SETs.

New methodology developed for characterizing dual-node configuration cells. The focus is now shifted to embedded IP elements.
Technical Highlights

- CMT testing almost completed

**DCM**

Pattern = 0, 0 Hz, Type = 0

Average of Bank 1 and 2 Upsets that Caused Multiple Switches, Creme: 8.42e-6
Average of Bank 1 and 2 Upsets that Caused Single Switches, Creme: 1.08e-5
Upsets that Caused Both Banks to Switch Multiple Times, Creme: 2.56e-5
Upsets that Caused Unique Single-Switch Events, Creme: 1.32e-5

**PLL**

Pattern = 1, 0 Hz, Type = 0

Average of Bank 1 and 2 Upsets that Caused Multiple Switches, Creme: 1.14e-5
Average of Bank 1 and 2 Upsets that Caused Single Switches, Creme: 5.50e-6
Upsets that Caused Both Banks to Switch Multiple Times, Creme: 3.51e-5
Upsets that Caused Unique Single-Switch Events, Creme: 2.39e-6
Technical Highlights

- BRAM and embedded BRAM EDAC evaluated for SEE
Technical Highlights

- SET testing on CLB
  - Frequency dependence evaluation

![Graphs showing cross-section vs. effective LET for different frequencies and patterns.](image-url)
Technical Highlights

• SET testing on CLB
  – SET Filter and Logic configuration (parallel vs. serial)
Going Forward

- System fault characterization methodology for XQR5VX130
  - Accelerator testing of SEFIs is complicated: cross-section dependence on LET, flux, rotation/tilt, and configuration monitor implementation
  - System-level qualification is convoluted:
    * Beam testing won’t express error rate from configuration bit upsets
  - FY11 Product will be a complete XQR5VFX130 static/pseudo-static characterization report
  - FY12 Product will be recommendations to estimate system error rates for various XQR5VFX130 designs.

- Unhardened IP characterization qualification
- Continued SEE testing of SiliconBlue and Altera FPGA

Complex SEE response will require flight qualification guidelines to be updated for this device
Packaging
FPGA Packaging

- The non-hermetic package is the beginning of a new era in packaging technology qualification - High density, high power VLSI devices
- Important implications for space applications
- What is required for risk management?
  - Failure classification standards
  - Identification of failure mechanisms
  - Improved failure analysis techniques
  - Electrical/thermal/mechanical simulation
  - Lifetime models with defined acceleration factor
  - Test vehicles for specific reliability characterization
  - Early warning structures
  - Space Quality Manufacturing guidelines
Xilinx V4/V5 Ceramic Package

- Each one of the highlighted areas is a qualification concern:
  - Underfill/Chip Capacitors/SiC Lid/Adhesive/Solder columns/Substrate

- Main stress tools are:
  - Temperature cycle
  - Temperature + humidity stress
  - Mechanical bond stress

- Evaluation tools:
  - C-SAM
  - Electrical test (custom and product)
FPGA Packaging – Xilinx V4 Nonhermetic

- Review and critique
- Integrate in mission requirements

- NEPAG
- Support documentation

- Additional testing
- Overall integration and risk management
Testing on Xilinx V4/V5 Non-hermetic Package

<table>
<thead>
<tr>
<th>Qualification Test</th>
<th>Test Method</th>
<th>Sample Size</th>
<th>Device</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group A testing</td>
<td>Mil Std 883, TM5005</td>
<td>100%</td>
<td>All 4 V4 XQR CF's</td>
<td>Pass</td>
</tr>
<tr>
<td>Modified* Group B Testing</td>
<td>Mil Std 883</td>
<td>per Mil Std 883</td>
<td>All 4 V4 XQR CF's</td>
<td>Pass, see Section 1</td>
</tr>
<tr>
<td>Group C testing</td>
<td>Mil Std 883, TM1005</td>
<td>15 units per device</td>
<td>XQR4VFX60, XQR4VLX200 &amp; XQR4VSX55</td>
<td>Pass, see Section 2</td>
</tr>
<tr>
<td>Group D testing</td>
<td>Mil Std 883</td>
<td>per Mil Std 883</td>
<td>XQR4VLX200 &amp; XQR4VSX55</td>
<td>Pass, see Section 1</td>
</tr>
<tr>
<td>Group E testing</td>
<td>Mil Std 883</td>
<td>per Mil Std 883</td>
<td>All 4 V4 XQR CF's</td>
<td>Pass</td>
</tr>
<tr>
<td>BLR Temperature Cycle Testing</td>
<td>IPC 9701</td>
<td>per IPC 9701</td>
<td>XQR4VLX200-CF1509</td>
<td>Pass, see Section 3</td>
</tr>
<tr>
<td>MLS 1 testing + CSAM</td>
<td>JEDEC Std 020A</td>
<td>15 units</td>
<td>XQR4VLX200-CF1509</td>
<td>Pass, see Section 4</td>
</tr>
<tr>
<td>Package Temperature Cycle Condition B Testing + CSAM</td>
<td>JEDEC &amp; Xilinx Std</td>
<td>14 units</td>
<td>XQR4VLX200-CF1509</td>
<td>Pass, see Section 4</td>
</tr>
<tr>
<td>Outgassing Testing</td>
<td>ASTM E-595</td>
<td>3 units</td>
<td>CF Underfill and Lid Adhesive</td>
<td>Pass, see Section 5</td>
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<tr>
<td>Wear Out Tests</td>
<td>Xilinx Std</td>
<td>Xilinx Std</td>
<td>V4</td>
<td>Pass, see Section 6</td>
</tr>
<tr>
<td>Mask Qualification (Latch Up and ESD)</td>
<td>Xilinx Std</td>
<td>Xilinx Std</td>
<td>All 4 V4 XQR CF's</td>
<td>Pass, see Section 6</td>
</tr>
</tbody>
</table>

* Some tests do not apply to ceramic flip chip


- Additional testing
  - Joint Xilinx/Customer Daisy Chain CF1752 qual
  - NEPP
    - CF1509 based board tests
    - PEM upscreening comparison of COTS FF series devices
    - Underlayer LP2 underfill – (Jong-ok Suh)
      - Thermal effects, outgassing, ageing due to plasma/radiation, vacuum, absorption.
V4 Daisy Chain – DPA
Cross Section of V4
COTS Flash FPGA DPA
Temp Cycle Qualification –
Manage Requirements with Different Packages

Bigger die and bigger packages have less capability in terms of total number of temp cycles

A Review of the CF Package & the Implications of addendum Y – J. Fabula MRQW 2010
• High performance FPGA to FPGA connection challenge amount of available I/O and signal latency.
• Multiple FPGA die to be combined into single package with Through-Silicon Via technology
• Provides 100x improvement/increase in inter-die bandwidth per watt over conventional approaches
Applications
NEPP Focused FPGA Application Assurance Support for Flight Projects

• “I did ______ to the FPGA. Is it going to be ok?”

• Provide NEPP generated engineering resource database of tests, measurements, and guidelines to support analysis:
  – Lifetime calculations based on physics of failure
  – Accelerated life test
  – Materials analysis and DPA
  – Risk management using guidelines and procedures

• Help to define next generation NEPP tasks that have broad agency relevance.
  – Materials degradations
  – SW/HW interactions
  – Technology characterization
  – Radiation Issues
Example Technology-Application Interaction: ESD influence on High Speed Designs

- Data Rates are influenced by the ESD loading capacitance
- The requirement of low capacitance in turn degrades ESD levels
- At 100 fF and below, 2kV HBM cannot be achieved

D. Sheldon
Continued technology scaling results in both metal current density and oxide breakdown voltage reduction.

Result is to close the ESD Window (Vbd – Vop) for High Speed Designs making it difficult to maintain 2kV HBM.

Protection versus Signal Integrity.
Methodology for Derating VLSI Devices

- Historically space community derated 40°C from (usually assumed) maximum of 150°C, or 110°C derated.
- Assuming 0.7eV activation energy, the 40°C from 150°C to 110°C gives an acceleration factor of 7.43.
  - This factor can be viewed as “margin” for long life reliability.
- Modern FPGAs have Tj_max = 125°C.
- Now we need to find what temperature gives same margin value using 125°C as the new derated maximum temperature.
Software
• ~50% of FPGA companies resources are in software development.
• The software environment and its interaction with the hardware determine the reliability and radiation performance of the FPGA.
• The tradeoffs, options and behaviors represent future areas for NEPP guidelines and recommendations
Design Abstraction

• To take advantage of ever increasingly sophisticated vendor supplied IP, software tools are at higher levels of abstraction than traditional HDL.
• Risk vs. Opportunity
Model based SW development

- Variety of new tools to support design validation and verification.
- DO-254 Tools and requirements – Future requirement for NASA?
- The interaction of HW and SW – Can FPGAs solve historical SW problems?
Explore Project Quality Management
S/W – Satin Technologies

- Ability to read and analyze a wide variety of files (csv, xls, SQL, DFT and STA reports, etc.)
- JavaScript based decision and parsing (arithmetic/natural language/etc.) formulism.
- Next generation tools to help manage complex projects.
The Future...
The future of commercial FPGA applications

- Intel Stellarton = Atom processor SoC + Altera FPGA
  - Emphasis on re-programmability, HW acceleration and customization
  - Xilinx V7 = FPGA + ARM microcontroller/processor
  - Actel Fusion = FPGA + ARM Cortex microprocessor
- In the future, SoC made up of processors and FPGA fabric could be standard high performance solution.
Future NEPP + FPGA Directions

• FPGA use will continue to grow in all aspects of spacecraft electronics.
• Power management will drive FPGA reliability.
• Transition to reprogrammable FPGAs as the norm.
• Guidelines for single event mitigation (SRAM and Flash)
• Technology reliability will require more details from foundries.
  – Independent life test experiments are becoming too expensive.
• Application support and IP verification may be new NEPP product.
  – Formal centers of FPGA test (HW and SW) may be required
• FPGA packaging will continue to challenge historical specifications and processes