Taming the SEU Beast - Approaches and Results for FPGA Devices and How To Apply Them

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Introduction

• Field Programmable Gate Array (FPGA) Single Event Effect (SEE) Models have been developed by NASA/GSFC Radiation Effects and Analysis Group (REAG)
  – Compartmentalize SEEs to enhance analysis
  – Uses a top-down approach
• Details of SEE generation and other electrical properties are part of ongoing development
• Presented models are only expected to fit synchronous designs as per NASA design guidelines.
Goal:

• Application of the NASA REAG FPGA Single Event Upset (SEU) Cross Section ($\sigma_{SEU}$) Model to a variety of FPGA types

Top Level Model has 3 major categories of $\sigma_{SEU}$:

\[
P_{\text{error}}(fs) \propto P_{\text{Configuration}} + P_{\text{Functional Logic}} + P_{\text{SEFI}}
\]

- Probability for Design Specific system SEE
- Probability for Configuration SEE
- Probability for Functional logic SEE
- Probability for Single Event functional Interrupt
Impact to Community

• Provides a standard method for comparing various types of FPGAs
• Enhances analysis by providing a means for evaluating Single Event Upsets (SEUs) and Single Event Transients (SETs):
  – Generation
  – System Propagation
  – Evaluate effectiveness of mitigation strategies
  – Determine dominant SEE components
  – Eases the overall analysis process
• Analysis provides designers with dominant or insignificant susceptible components... enhanced design for radiation strategies
Technical Highlights

• This presentation will focus on:
  – Configuration: $P_{configuration}$
  – Data Path functional logic: $P_{functional Logic}$

• Model Derivation is presented

• Model application to Microsemi FPGAs:
  – RTAXs: Embedded Radiation Hardened by Design (RHBD)
  – ProASIC3: No embedded mitigation

\[ P(f_s)_{error} \propto P_{Configuration} + P(f_s)_{functional Logic} + P_{SEFI} \]
Configuration

\[ P_{\text{Configuration}} \]
Place, Route, and Gate Utilization are Stored in the FPGA Configuration

- **Configuration Defines:**
  Arrangement of pre-existing logic via programmable switches
  - Functionality (logic cluster)
  - Connectivity (routes)
  - Placement

- **Programming Switch Types:**
  - **Antifuse:** One time Programmable (OTP)
  - **SRAM:** Reprogrammable (RP)
  - **Flash:** Reprogrammable (RP)

To be presented by Melanie Berg at the NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop, Greenbelt, Maryland, June 28-30, 2011, and published on nepp.nasa.gov.
Programmable Switch Implementation and Single Event Upset (SEU) Susceptibility

ANTIFUSE (OTP)

SRAM (RP)

Configuration: SEU IMMUNE

Configuration: SEU SUSCEPTIBLE
## Configuration Test and Analysis

- Configuration is static during operation... hence we test and evaluate it statically

<table>
<thead>
<tr>
<th></th>
<th>Antifuse</th>
<th>SRAM</th>
<th>FLASH</th>
<th>SEU Hardened SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>Microsemi</td>
<td>Xilinx</td>
<td>Microsemi</td>
<td>Xilinx, Achronix, Atmel</td>
</tr>
<tr>
<td></td>
<td>Aeroflex</td>
<td>Achronix</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Upset Signature</td>
<td>Fuse</td>
<td>Bit State</td>
<td>Bit State or resistivity</td>
<td>Bit State</td>
</tr>
<tr>
<td></td>
<td>Resistivity</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Configuration Test</td>
<td>Non-Specific</td>
<td>Read-back post-irradiation</td>
<td>Verify Post-irradiation</td>
<td>Read-back post-irradiation</td>
</tr>
<tr>
<td>Information from Configuration Test</td>
<td>N/A</td>
<td>Upset configuration bits</td>
<td>Pass/Fail</td>
<td>Upset configuration bits</td>
</tr>
<tr>
<td>Results</td>
<td>No upsets observed</td>
<td>Dominant upsets</td>
<td>Insignificant</td>
<td>Low significance</td>
</tr>
<tr>
<td>REAG Tested</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Atmel, Achronix, Yes/Xilinx No</td>
</tr>
</tbody>
</table>
### Impact of Configuration Testing and Analysis to the REAG Model

<table>
<thead>
<tr>
<th>Component</th>
<th>Equation Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Antifuse</td>
<td>[ P(f_s)<em>{\text{error}} \propto P</em>{\text{functional Logic}}(f_s) + P_{\text{SEFI}} ]</td>
</tr>
<tr>
<td>SRAM (non-mitigated)</td>
<td>[ P(f_s)<em>{\text{error}} \propto P</em>{\text{Configuration}} ]</td>
</tr>
<tr>
<td>Flash</td>
<td>[ P(f_s)<em>{\text{error}} \propto P</em>{\text{functional Logic}}(f_s) + P_{\text{SEFI}} ]</td>
</tr>
<tr>
<td>Hardened SRAM</td>
<td>[ P(f_s)<em>{\text{error}} \propto P</em>{\text{Configuration}} + P_{\text{functional Logic}}(f_s) + P_{\text{SEFI}} ]</td>
</tr>
</tbody>
</table>
Data Path Functional Logic and Concepts of Synchronous Design
Synchronous Design Basic Building Blocks: Combinatorial Logic and Flip-Flops (DFF’s)

**Combinatorial Logic:** Output is a function of the inputs after some delay ($\tau_{dly}$)

Output = $f$ (input, $\tau_{dly}$)

**DFF:** Captures data input at clock edge and is a function of the clock period ($\tau_{clk}$)

$Q = f(D, \tau_{clk})$
Component Libraries: Basic Designer Building Blocks

- Combinatorial logic blocks
  - Vary in complexity
  - Vary in I/O

- Sequential Memory blocks (Flip-flops or DFFs)
  - Uses global Clocks
  - Uses global Resets
  - May have mitigation
DFF’s in a Synchronous Design

- All DFFs are connected to a clock
- Clock period: $\tau_{clk}$
- Clock frequency: $f_s$

\[
\tau_{clk} = \frac{1}{f_s}
\]

DFFs are BOUNDARY POINTs in a synchronous design
Deterministic Data Capture...Adhering to Setup and Hold Time for a DFF

Data Launch from StartPoint

DFF1

Hold:

StartPoint

DFF1

EndPoint

DFF2

Setup:

\[ \tau_{\text{dly}} < \tau_{\text{clk}} - (\tau_{\text{su}} + \tau_{\text{skew}} + \tau_{\text{jitter}}) \]

Data Capture is Deterministic when:

\[ \tau_{\text{dly}} \]: Data Delay through combinatorial logic and routes

\[ \tau_{\text{su}} \]: Setup time
Making Setup Time: Static Timing Analysis (STA)

DFFs are boundary points
- Timing is performed from one DFF to the next DFF
- For each DFF, data paths are traced backwards to their start-points
- Combinatorial logic and routes are part of the delay
Start Point DFFs → End Point DFFs

\[ \tau_{dly} \text{ and the "Cone of Logic"} \]

EndDFF(\( T \)) = f(StartDFFs(\( T - 1 \)))

Signal will arrive at destination by \( \tau_{dly} \) ... but it will not be captured until the next clock edge.

Referred to as the "Cone of Logic"
System States

- System state is defined by the logic values within all DFFs
- In between clock edges (intermediate points)
  - Computations are occurring (combinatorial logic)
  - SETs or SEUs can occur
- System state is captured at each rising clock edge... after clock cycle computations are completed

Note: Upsets occur at intermediate points. They become part of the system state if they are captured into the next state
Synchronous Design Take Away Points

• Basic Blocks: DFFs and Combinatorial logic
• DFFs are boundary points
  – For each DFF (end point) there is a backwards trace to start point DFFs
  – There is delay between start point DFFs and endpoint DFFs
    • Combinatorial logic
    • Routes
• SEE analysis is based on utilized DFFs in a design because an upset is not an upset unless it is captured by a DFF

The question is... If an upset occurs will it reach an endpoint DFF?
Data Path Functional Logic

\[ P_{\text{functionalLogic}} \]
Configuration versus Data Path (Functional Logic) SEE

- Configuration and Functional logic are separate logic
- Can be implemented with different technologies within one device (e.g. antifuse versus CMOS)
- Configuration is static and data paths are not. Requires a different test and analysis approach

This explains why there are separate categories of error:

\[ P_{\text{configuration}} \text{ vs. } P_{\text{functional Logic}} \]
## SEU and SET Background

Primary functional logic components can be classified into:

<table>
<thead>
<tr>
<th>Combinatorial</th>
<th>Sequential</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Logic function generation</strong> (computation)</td>
<td><strong>Captures and holds state of combinatorial Logic</strong></td>
</tr>
<tr>
<td>SET</td>
<td>SEU</td>
</tr>
</tbody>
</table>

**SET: Glitch in the combinatorial logic: Capture is frequency dependent**

**SEU: State changes until next cycle of enabled input: Next state capture can be frequency dependent**

*SET effects are nonlinear and are heavily design and state dependent.*

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Data Path Model and DFF Logic Cones

\[ P(fs)_{\text{functional Logic}} \]

Evaluate for Each DFF

\[ \exists_{DFF} \left( \sum_{j=1}^{\#\text{Start Point DFFs}} P(fs)_{\text{DFFSEU\rightarrow SEU}(j)} + \sum_{i=1}^{\#\text{Combinatorial Cells}} P(fs)_{\text{SET\rightarrow SEU}(i)} \right) \]

Probability for Captured DFF Events

Probability for Captured Combinatorial logic

DFF\(_k\) Cone of Logic

*All Start Point DFFs and Combinatorial Logic gates that feed into End Point DFF under Evaluation (DFF\(_k\))*:

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Combinatorial Logic Contribution to System Error in a Synchronous System: Capturing a SET

\[ P_{SET \rightarrow SEU} \]
SETs and a Synchronous System

- Generation ($P_{gen}$)
- Propagation ($P_{prop}$)
- Logic Masking ($P_{logic}$)
- Capture

All Components comprise:

$P_{SET\rightarrow SEU}$
SET Generation: $P_{\text{gen}}$

- SET generation occurs due to an “off” gate turning “on”.
- A transient in a CMOS circuit will be generated with an amplitude and width ($\tau_{\text{width}}$) based on:
  - Amount of deposited charge (i.e. small Linear Energy Transfer (LET) values produce small transients)
  - The strength of the gate’s load
  - The strength of its complimentary “ON” gate
  - The dissipation strength of the process.

$$Q_{\text{coll}} > Q_{\text{crit}}$$

$$Q_{\text{crit}} = C_{\text{node}} * V_{\text{node}}$$

Collected Charge > Critical Charge

Node Capacitance

Node Voltage
SET Propagation to an EndPoint DFF: $P_{prop}$

- In order for the data path SET to become an upset, it must propagate and be captured by its endpoint DFF.
- $P_{prop}$ only pertains to electrical medium (capacitance of path… combinatorial logic and routing)
  - Capacitive SET amplitude reshaping
  - Capacitive SET width reshaping
  - Small SETs or paths with high capacitance have low $P_{prop}$
- $P_{prop}$ heavily contributes to the non-linearity of $P_{SET\rightarrow SEU}$ because of the variation in path capacitance.
SET Logic Masking: $P_{\text{logic}}$

- $P_{\text{logic}}$: Probability that a SET can logically propagate through a cone of logic. Based on state of the combinatorial logic gates and their potential masking.

“AND” gate reduces probability that SET will logically propagate

$0 < P_{\text{logic}} < 1$

Determining $P_{\text{logic}}$ for a complex system can be very difficult
SET Capture at Destination DFF

Each combinatorial element can generate a transient. The transient width will be a fraction of the clock period for a synchronous design in a CMOS process.

\[ P(\tau_{\text{clk}})_{\text{SET} \rightarrow \text{SEU}} \propto \frac{\tau_{\text{width}}}{\tau_{\text{clk}}} \]

\[ P(f_s)_{\text{SET} \rightarrow \text{SEU}} \propto \tau_{\text{width}} f_s \]

Probability of capture is proportional to the width of the transient as seen from the destination DFF.
Data Path Model and Combinatorial Logic SETs

\[ P(fs)_{\text{functionalLogic}} = \exists_{DFF} \left( \sum_{j=1}^{\#\text{StartPointDFFs}} P(fs)_{DFFSEU \rightarrow SEU(j)} + \sum_{i=1}^{\#\text{CombinatorialCells}} P(fs)_{SET \rightarrow SEU(i)} \right) \]

\[ = \exists_{DFF} \sum_{i=1}^{\#\text{CombinatorialCells}} P_{\text{gen}(i)} P_{\text{prop}(i)} P_{\text{logic}(i)} \tau_{\text{width}(i)} fS \]

\[ \text{Upper Bound SET } P_{\text{logic}} = 1 \]
DFF Contribution to System Error in a Synchronous System

\[ P_{\text{DFFSEU} \rightarrow \text{SEU}} \]
Conventional Theory: System Upsets Have a Static Component + Dynamic Component

\[ \sigma_{DFFerror} = P_{DFFSEU} + P_{(fs)}_{SET \rightarrow SEU} \]

**Composite Cross Section**

Does not fully characterize DFF upsets as they pertain to a synchronous system.

Takes into account upsets from combinatorial logic in DFF data path and the DFF potential for flipping its state.
SEUs and a Synchronous System: New Stuff

- Generation \( P_{DFFSEU} \)
- \( P_{prop} = 1 \) for hard state switch
- Logic Masking \( P_{logic} \)
- Capture

All Components comprise:

\[ P_{DFFSEU→SEU} \]
Generation of DFF Upsets: $P_{DFFSEU}$

- Probability that a DFF will flip its state
- Can be a hard flip:
  - Will not change until the next clock cycle
  - Amplitude and width are not affected as with a SET
- Can be a metastable flip
  - No real defined state
  - Otherwise known as a “weak” state
  - Can cause oscillations in the data path
### Generation $P_{DFFSEU}$ versus $P(fs)_{DFFSEU\rightarrow SEU}$

<table>
<thead>
<tr>
<th>$P_{DFFSEU}$</th>
<th>$P(fs)_{DFFSEU\rightarrow SEU}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Probability a Startpoint DFF becomes upset</td>
<td>Probability that the Startpoint upset is captured by the endpoint DFF</td>
</tr>
<tr>
<td>Occurs at some point in time within a clock period</td>
<td>Occurs at a clock edge (capture)</td>
</tr>
<tr>
<td>Not frequency dependent</td>
<td>Frequency dependent</td>
</tr>
</tbody>
</table>
Logic Masking DFFs… $P_{\text{logic}}$

- Logic masking for DFF start points is similar to logic masking of combinatorial logic.
- DFF logic masking is generally the point where Triple Modular Redundancy (TMR) is inserted.

$P_{\text{logic}} > 0$
for Voter… its upsets are not masked

$P_{\text{logic}} = 0$
for DFFs… their upsets are masked
DFF Upsets (SEUs) and Next State Capture: $P_{\text{DFFSEU}}$ and $P_{\text{DFFSEU} \rightarrow \text{SEU}}$

- If a DFF is affected by an SEU it will change its state somewhere within a clock cycle at time $\tau$

$$0 < \tau < \tau_{\text{clk}} \quad \tau \text{ is defined to be within 1 clock period (} \tau_{\text{clk}} \text{)}$$

Will the endpoint DFF capture the upset?  
Will the endpoint DFF capture the correct value?  
OR…

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SEU Capture Example: Assume $\tau_{clk} = 15$ns

If DFF_D flips its state...

$0 < \tau < (5.5)$ns

The upset will get caught...

otherwise it’s as if the event never occurred
Percentage of Clock Cycle for SEU Capture:

\[ \tau < \tau_{clk} - \tau_{dly} \quad \text{Upset is caught within this timeframe} \]

\[ \frac{\tau}{\tau_{clk}} < \frac{\tau_{clk} - \tau_{dly}}{\tau_{clk}} \quad \text{Fraction of clock period for upset capture} \]

\[ \frac{\tau}{\tau_{clk}} < 1 - \frac{\tau_{dly}}{\tau_{clk}} \]

\[ \tau f_S < 1 - \tau_{dly} f_S \quad \text{Fraction of clock period for upset capture wrt to frequency} \]
Data Path Upsets and Start Point DFFs

\[ P(fs)_{\text{functionalLogic}} \]

\[ \sum_{DFF} \left( \sum_{j=1}^{\#\text{StartPointDFFs}} P(fs)_{\text{DFFSEU}\rightarrow SEU(j)} + \sum_{i=1}^{\#\text{CombinatorialCells}} P(fs)_{\text{SET}\rightarrow SEU(i)} \right) \]

\[ \sum_{j=1}^{\#\text{StartPointDFFs}} P_{\text{DFFSEU}(j)} P_{\text{logic}(j)} (1 - \tau_{\text{dly}(j)} fs) \]
Putting it all together:

\[ P(fs)_{\text{functional Logic}} = P(fs)_{\text{DFF SEU \rightarrow SEU}} + P(fs)_{\text{SET \rightarrow SEU}} \]

DFF SEU capture  DFF SEU capture  Combinatorial Logic SET capture
NASA REAG FPGA Data Path Functional Logic Susceptibility Model

\[
P(f_s)_{\text{functionaLogic}}
\]

\[
\exists_{DFF} \left( P(f_s)_{DFFSEU\rightarrow SEU} + P(f_s)_{SET\rightarrow SEU} \right)
\]

\[
\exists_{DFF} \left( \sum_{j=1}^{\#\text{StartPointDFFs}} P_{DFFSEU(j)} \left( 1 - \tau_{dly(j)} f_s \right) P_{\text{logic}(j)} \right) + \sum_{i=1}^{\#\text{CombinatorialCells}} \left( P_{\text{gen}(i)} P_{\text{prop}(i)} P_{\text{logic}} \tau_{\text{width}(i)} f_s \right)
\]
NASA REAG FPGA Upper Bound Susceptibility Model

\[
\exists_{DFF}\left(\sum_{j=1}^{\text{StartPointDFFs}} P_{DFFSEU(j)}(1 - \tau_{dly(j)}fs)P_{\text{logic}(j)}) + \sum_{i=1}^{\text{CombinatorialCells}} (P_{\text{gen}(i)}P_{\text{prop}(i)}P_{\text{logic}}\tau_{\text{width}(i)}fs)\right)
\]

Upper-bound assumes \(P_{\text{logic}}=1\) (no mitigation) and NO DFF frequency (fs) dependency
NASA REAG Models + Heavy Ion Data: RTAXs
RTAXs FPGA Core Logic: Basic Building Blocks are R-CELLs and C-CELLs

R-CELL: Sequential + Combinatorial

C-CELL: Combinatorial

Combinatorial Logic is susceptible to Single Event Transients (SETs) (RCELLs, CCELLs, and buffers are susceptible to SETs)

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Model Application to RTAXs: Embedded Localized Triple Modular Redundancy (LTMR)

\[ P(f_s)_{error} \propto P_{Configuration \ SEE \ upset \ rate} + P(f_s)_{Functional \ logic \ SEE \ upset \ rate} + P_{SEFI \ Interrupt} \]

Design Specific SEE upset rate

Configuration SEE upset rate

Functional logic SEE upset rate

Single Event functional Interrupt

Combinatorial logic cells

(LTMR): DFF
Testing Combinatorial Logic Contributions to SEU Cross-Sections: WSRs with Inverters

Combinatorial Logic

N levels of Inverters between DFF stages: N = 0, 8, and 18

Shift Register Chain

4-bit Window Output

Windowed Shift Register (WSR)

WSR₀: N=0 Chain … Only DFFs
WSR₈: N=8 Chain… 8 Inverters per 1 DFF
WSR₁₆: N=16 Chain… 16 Inverters per 1 DFF

Think of DFFs as your boundary points… They capture SETs

∃ \left( \sum_{j=1}^{1} (P_{gen(i)} P_{prop(i)} \tau_{width(i)} f_s) \right) + \sum_{i=1}^{\#CombinatorialCells} (P_{gen(i)} P_{prop(i)} \tau_{width(i)} f_s)

RCELL: Combinatorial
CCELL: Combinatorial

CCELLs: Inverters

CCELLs: Inverters
RTAXs: SET Capture across LET affects WSR SEU Cross Sections

\[ \sigma_{SEU}(\text{cm}^2/\text{bit}) = \left( \sum_{i=1}^{#\text{CombinatorialCells}} \left( P_{\text{gen}(i)} P_{\text{prop}(i)} \tau_{\text{width}(i)} f s \right) \right) + \sum_{i=1}^{#\text{CombinatorialCells}} \left( P_{\text{gen}(i)} P_{\text{prop}(i)} \tau_{\text{width}(i)} f s \right) \]

Per WSR stage

Increase Frequency → Increase Cross section

Increase Combinatorial Logic → Increase Cross section

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RTAXs: SET Capture across LET affects SEU Cross Sections (Non-Linearity)

Non-Linear Effects:
- WSR₀ has the lowest $\sigma_{\text{SEU}}$ at High LETs
- $\omega WSR₀ \sigma_{\text{SEU}} > WSR₈ \sigma_{\text{SEU}}$ at Low LETs

Low LETs: attenuation of Single Event Transients (SETs) at low LET values
Why is $\text{WSR}_0 > \text{WSR}_8$ for Low LET?

\[
(P(f_s)_{SET\rightarrow SEU})|_{\text{WSR}_0} > (P(f_s)_{SET\rightarrow SEU})|_{\text{WSR}_8}
\]

RCELL

Additional buffer after LTMR DFFs

Can’t make it to end point ($P_{prop}$ is low)

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Why is $WSR_0 > WSR_8$ for Low LET? Proof using the REAG Model

$WSR_8\ CCELL\ P_{prop\ is\ low}$

$\sum_{j=1}^{1} P_{gen(j)} P_{prop(j)} \tau_{\text{width}(j)} f_S + \sum_{i=1}^{1} P_{gen(i)} P_{prop(i)} \tau_{\text{width}(i)} f_S < \sum_{j=1}^{1} P_{gen(j)} P_{prop(j)} \tau_{\text{width}(j)} f_S$

$WSR_8\ RCELL\ CCELL\ P_{prop\ is\ low}$

$\sum_{j=1}^{1} P_{gen(j)} P_{prop(j)} \tau_{\text{width}(j)} f_S < \sum_{j=1}^{1} P_{gen(j)} P_{prop(j)} \tau_{\text{width}(j)} f_S$

$WSR_8\ RCELL\ P_{prop\ is\ low}$

$RCELL\ P_{prop\ is\ low} < RCELL\ P_{prop\ is\ low}$

Can’t make it to end point ($P_{prop\ is\ low}$)

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NASA REAG Models + Heavy Ion Data: ProASIC
Background: Micro-Semi (Actel) ProASIC3 Flash Based FPGA

- Originally a commercial device
- Configuration is flash based and has proven to be almost immune to SEUs
- No embedded mitigation in device
- Evaluation of user mitigation insertion has been performed
Actel ProASIC3 Shift Register Study

- Shift Register Functional Logic Designs Under Test:
  - Six WSR strings with various levels of combinatorial logic

\[
P(f_s)_{\text{error}} \propto P_{\text{Configuration}} + P(f_s)_{\text{functional Logic}} + P_{\text{SEFI}}
\]

\[
\exists_{DFF} \left( P(f_s)_{DFF\,SEU \rightarrow SEU} + \sum_{i=0}^{\#\text{Inverters}} P(f_s)_{SET \rightarrow SEU(i)} \right)
\]
**σ_{SEU} Test Results: Windowed Shift Registers (WSRs) No-TMR**

- **N=0**: WSR with only DFFs
- **N=8**: WSR with 8 inverters between each DFF stage
- **No Mitigation**: \( σ_{SEU} WSR_0 > σ_{SEU} WSR_8 \) For every LET

---

**No-TMR 100MHz Checkerboard LET Versus SEU Cross Section**

- \( WSR \ N=8 \)
- \( WSR \ N=0 \)
Why is WSR0 > WSR8 for Non-Mitigated ProASIC: $\tau_{dly}$

For a clock period = $\tau_{clk}$, if DFFa flips @ time $\tau > (\tau_{clk} - \tau_{dly})$ then DFFb will never capture the upset.

Startpoint

For a clock period = $\tau_{clk}$, if DFFa flips @ time $\tau > (\tau_{clk} - \tau_{dly})$ then DFFb will never capture the upset.

Endpoint

$W SR_0 \quad \tau_{dly} \ll W SR_8 \quad \tau_{dly}$

Combinatorial Logic: Inverters
Why is $WSR_0 \sigma_{SEU} > WSR_8 \sigma_{SEU}$ for The Non-Mitigated ProASIC3 Design?

New Research!

\[
(P(fs)_{DFFSEU\rightarrow SEU}|_{WSR_0} > (P(fs)_{DFFSEU\rightarrow SEU} + P(fs)_{SET\rightarrow SEU})|_{WSR_8}
\]

**DFF Capture** \((P(fs)_{DFFSEU\rightarrow SEU})\) for \(WSR_0\) is not the same as \(WSR_8\) because of \(\tau_{dly}\)

\[
P_{DFFSEU}(1 - \frac{\tau_{dly}|_{WSR_0}}{\tau_{clk}}) > P_{DFFSEU}(1 - \frac{\tau_{dly}|_{WSR_8}}{\tau_{clk}}) + \sum_{i=1}^{8} P(fs)_{SET\rightarrow SEU(i)}
\]

\(\tau_{dly}|_{WSR_0} < \tau_{dly}|_{WSR_8} < \tau_{clk}\)

\[
P_{DFFSEU} > \frac{\tau_{clk}}{\tau_{dly}|_{WSR_8} - \tau_{dly}|_{WSR_0}} \sum_{i=1}^{8} P(fs)_{SET\rightarrow SEU(i)}
\]

**DFF \(\sigma_{SEU} > \) combinatorial logic \(\sigma_{SET}\)**

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**Comparison of $P_{DF{}FSEU\rightarrow SEU}$ and $P_{SET\rightarrow SEU}$ ... How it Impacts System Susceptibility**

<table>
<thead>
<tr>
<th>Logic</th>
<th>$P_{DF{}FSEU\rightarrow SEU}$</th>
<th>$P_{SET\rightarrow SEU}$</th>
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</thead>
<tbody>
<tr>
<td>Startpoint DFF Capture by Endpoint DFF</td>
<td>Combinatorial SET Capture by Endpoint DFF</td>
<td></td>
</tr>
</tbody>
</table>

Capture percentage of clock period ($\tau_{clk}$)

\[
(1 - \frac{\tau_{dly}}{\tau_{clk}}) = (1 - \tau_{dly} \cdot f_S) \quad \frac{\tau_{width}}{\tau_{clk}} = \tau_{width} f_S
\]

Frequency Dependency

As frequency **increases**, $P_{DF{}FSEU\rightarrow SEU}$ **decreases**  
As frequency **increases**, $P_{SET\rightarrow SEU}$ **increases**

Combinatorial Logic Effects

Increase Combinatorial logic increases $\tau_{dly}$ and decreases $P_{DF{}FSEU\rightarrow SEU}$  
Increase in combinatorial logic increases $P_{gen}$ and increases $P_{DF{}FSEU\rightarrow SEU}$

To be presented by Melanie Berg at the NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop, Greenbelt, Maryland, June 28-30, 2011, and published on nepp.nasa.gov.
Another Application of the $P(fs)_{\text{functionalLogic}}$ Model Components

- If the DFFs are mitigated and the $\sigma_{\text{SEU}}$ is decreasing over frequency, how do you analyze this?
  - Combinatorial logic effects are directly proportional to system frequency
    \[ P_{\text{gen}(j)} P_{\text{prop}(j)} \tau_{\text{width}(j)} f_s \]
  - Hence, most likely not due to combinatorial logic… i.e. not $P_{\text{SET}} \rightarrow \text{SEU}$.
- More than likely, the DFFs are not as mitigated as you expected them to be
  - As system frequency increases cross section decreases
    \[ (1 - \tau_{\text{dly}} f_s) \]
  - $P_{\text{logic}} \neq 0$
Local Triple Modular Redundancy (LTMR): Triple DFFs Only

• Triple Each DFF + Vote+ Feedback Correct at DFF
• Unprotected:
  – Clocks and Resets… SEFI
  – Transients (SET->SEU)
  – Internal/hidden device logic: SEFI

\[ P(fs)_{error} \propto P_{Configuration} + P(fs)_{DFF \rightarrow SEU} + P(fs)_{SET \rightarrow SEU} + P_{SEFI} \]
ProASIC LTMR Shift Register Data Path Model

Evaluate for Each DFF

\[
\exists_{DFF} \left( \sum_{j=1}^{\#Start\text{DFFs}} P(f_s)_{DFF\rightarrow SEU(j)} + \sum_{i=1}^{\#\text{Combinatorial Logic Gates}} P(f_s)_{SET\rightarrow SEU(i)} \right)
\]

LTMR: \( P_{logic} = 0 \)

\[
\exists_{DFF} \left( P(f_s)_{DFF\rightarrow SEU} + \sum_{i=1}^{\#\text{Combinatorial Logic Gates}} P(f_s)_{SET\rightarrow SEU(i)} \right)
\]

\[
\exists_{DFF} \left( \sum_{i=1}^{\#\text{Combinatorial Logic Gates}} P(f_s)_{SET\rightarrow SEU(i)} \right)
\]

As we increase \#combinatorial logic gates we increase \( \sigma_{SEU} \)
\( \sigma_{SEU} \) Test Results: Windowed Shift Registers (WSRs) No-TMR versus TMR

- LTMR is effective and has reduced \( P_{DFFSEU} \)
- **LTMR: SEU cross Sections** \( WSR_0 < WSR_8 \) For every LET
Deliverables

• Further develop components of model for all FPGAs of concern
• Apply the model to an Application Specific Integrated Circuit (ASIC) Design
• Utilize the models to develop:
  – Develop design guidelines for radiation effects per FPGA
  – Evaluate strength of a variety of mitigation strategies per FPGA type
Summary

- REAG has developed a FPGA SEE model:
  - Specifically for Synchronous designs
  - Categorizes SEE upsets to assist analysis and test structure development
  - Successfully applied across a variety of FPGA types
  - Great method for comparing different device types
  - Upper-bound version is mostly utilized

\[
P(f_s)_{\text{error}} \propto P(f_s)_{\text{Configuration}} + P(f_s)_{\text{functional Logic}} + P(f_s)_{\text{SEFI}}
\]

\[
\exists_{\text{DFF}} \left( P(f_s)_{\text{DFFSEU} \rightarrow \text{SEU}} + P(f_s)_{\text{SET} \rightarrow \text{SEU}} \right)
\]

\[
\exists_{\text{DFF}} \left( \sum_{j=1}^{\#\text{StartP}\text{aintDFFs}} P_{\text{DFFSEU}(j)} (1 - \tau_{\text{dly}(j)} f_s) P_{\text{logic}(j)} \right) + \sum_{i=1}^{\#\text{Combinatorial Logic Gates}} (P_{\text{gen}(i)} P_{\text{prop}(i)} P_{\text{logic}(i)} \tau_{\text{width}(i)} f_s)
\]

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