Outline

• Background
• HiREV Leadership
• High Level Description
• Activities
• Accomplishments
Background

• 1997- AFRL stood up and the Reliability Assessment Center (Rome Lab) was stood down – Reliability Information Analysis Center (RiAC) maintained

• Early 2000s – Electronics parts anomalies

• 2003-2004: National community formed tiger teams to assess causes of increase in parts anomalies

• One common conclusion was that a “Physics of Failure” Center of Excellence was missing and was needed for Mission Success

• 1 Feb 2010: AFRL and NRO stood up HiREV and provided long-term leadership, advocacy, and resources – Space and Missiles Systems Center joined
HiREV Leadership Team

Systems Engineering
Tom Burns / Byron Knight

Space and Missile Systems Center
Dave Davis

Space Vehicles
Andy Motes / Ken Hunt

Materials and Manufacturing
Don Dorsey

Sensors
Chris Bozada

National Systems Group
Rich Haas / Dave Eccles

Physical Sciences Laboratories
Jon Osborn

Electronics and Sensors Division
Larry Harzstark

Defense Microelectronics Activity
Dan Marrujo
Goal: develop and maintain a govt led center
- Not compete with existing activities or groups
- A group of experts, tools, and contract vehicles with resources that are ready and capable
- Provide support to Tech Maturation / Insertion, Acquisition and R&D communities

Not just
- a program or program portfolio
- independent technology assessment
- prequalification activities
- Information sharing/data repository
- Contributor to MIL SPEC/STD/HDBK/PRF updates

Long term commitment to “Stake holders”
What HiREV is Not

- Productization and Qualification
- Technology Maturation
- Root Cause Investigation
- Reliability Improvement
- Underwriter’s Laboratory

Confusing, because some of the “team” does do these activities
**Prequalification**

Addressing TRL 3 to TRL 6

Determine whether a technology is qualifiable or not for a given application
Refined ConOps

- Technology Forecast
  Poll acquisition, prime and manufacturer communities

- Reliability Science
  Physics and chemistry based models, tools and techniques

- Prequalification
  Lit Reviews, test chip design and fab, testing, analysis, etc

- Information Sharing
  Data, measurements, techniques, models, standards, guidelines, etc
HiREV Reliability Science Focus

• Improved Models of Device Operation and Degradation
  • Complex physical and chemical interactions
  • Get the stressor distribution right
  • Predict behavior in areas inaccessible to measurements
  • Interpret stress test and characterization results
  • Ultimately, provide higher fidelity lifetime estimates

• Improved Characterization Techniques
  • Improved sample prep (spatial specificity & sample quality)
  • Drive spatial resolution to the nanoscale
  • Evolution of charge, point defect populations
  • Thermal, Electrical and Mechanical Behavior
HiREV Prequalification Model

- Existing knowledge/data review
- Characterization of operational conditions
- Lifetest planning/execution/analysis
- Parts (unstressed, partially stressed, failed)
- Stress Testing
- Non-destructive analysis (pre and post test)
- Destructive Physical Analysis (pre and post test)
- Modeling/Simulation
- Technology Assessment (Qualification Guidelines)

Technology Qualifiable and a Path to Qualification Developed
Draft Prequalification Workflow

A) Technology node literature search and assessment — Effort to determine what is known (what needs to be independently validated) and what is not known (but should be known) to assess the applicability of a given technology node.

Ideal set of information:
1) Technology capability and projected use
   a) What are the targeted applications?
   b) What are the technology limits?
   c) What type of parts will be built?
      i) Operational environment
      ii) Operational waveforms
      iii) Thermal analysis

2) Manufacturer’s prowess/technology node maturity (ability to manufacture and control process)
   a) Variability (within part, within wafer, within lot, lot-to-lot)
   b) SPC controls and spec limits
      i) Spec limits derived from instrument limits, performance, yield and/or reliability
      ii) Throughput (actual and full)
      iii) Process and performance margins and their sensitivities
      iv) Process/test optimization

3) Reliability Assessment
   a) Failure modes and effects analysis
   b) Waveform analysis
   c) Step stress tests
   d) Accelerated life testing
      i) Parts sampled

   ii) Type of accelerants
   iii) Long term > 6000 hours
   iv) Degradation data
      A. Lifetime projection analysis and confidence
      B. Multi-mode analysis

   v) Failure mechanism identification
   vi) Pre, during and post stress characterization
      A) Non-destructive
      B) Destructive

   vii) Degradation models
      A. Empirical
      B. Physics and Chemistry
      C. Operational at IC level

   d) Operational life tests (longest lived parts)
   e) Field returns/data (especially on similar and the same parts in the desired environment)

4) Radiation and synergistic effects/characterization/modeling

B) Develop and cost work plan to fill missing information and/or validate results/analysis
   1) Part availability (test structures, transistors, integrated circuits: unstressed, partially stressed and failed)
   2) Artwork/foundry availability
   3) Stress stands
   4) Etc

C) Develop qualification guides
Selected Achievements

- Developed new laboratory analysis and 3D visualization techniques – high fidelity atomic analysis
- Explained radiation failure mechanism (particle spallation) in 90 nm CMOS – explained premature degradation
- Characterized impact of “cracks” in GaN devices – critical new semiconductor device degradation
- Completed early pre-qualification experiments and analysis for wide bandgap semiconductors and advanced CMOS – impact on insertion decisions
- Expanded government and industry participation – team is gaining capability
- Discussions underway with Community of Practice – assure minimal duplication of effort
- Brought HiREV Information Architecture (HIA) prototype on-line – information sharing is a key capability
Trusted Foundry 90 nm process destructive physical analysis

- Provided by Boeing under DARPA Rad-Hard By Design (RHBD) program
- Destructive physical analysis used to characterize technology
- Resulting products shared between HiREV partners to further understanding of device reliability
Die Top View
Minimum Geometry Device #4

- Mask layout images are not necessarily representative of true shape of device
- FIB nanotomography
DualBeam-FIB Sample Prep for TEM

The sample was extracted and mounted upside-down to prevent curtaining in substrate silicon.
The shallow trench isolation (STI) has a double-layer liner.
Transistor and STI details

Bright contrast observed in the ADF image (but not in the HAADF), at the STI edge, is likely related to lattice strain in this region.
Details at the Edge of the Transistor Gate

Dark regions in the HAADF image in the source/drain regions could be related to defects associated with dopant levels.
Electron Energy Loss Spectral (EELS) Mapping
Lattice Resolution at the Gate Oxide

Lattice resolution HAADF-STEM allowed gate oxide thickness measurement.

Lattice resolution imaging: gate oxide thickness = 2 nm
Next Steps (6 months)

- Formalize virtual center with multi-party non-disclosure agreement (Aerospace / Industry / Academia)
- Complete draft of electronic technology forecast
- Continue reliability science activities
- Test information sharing proof of concept
- Refine prequalification guide – use industry to assess
Questions?