National Aeronautics and Space Administration

NASA Electronic Parts and Packaging (NEPP) Program

3rd Electronics Technology Workshop (ETW)

NEPAG Update

Shri Agarwal
NASA/JPL

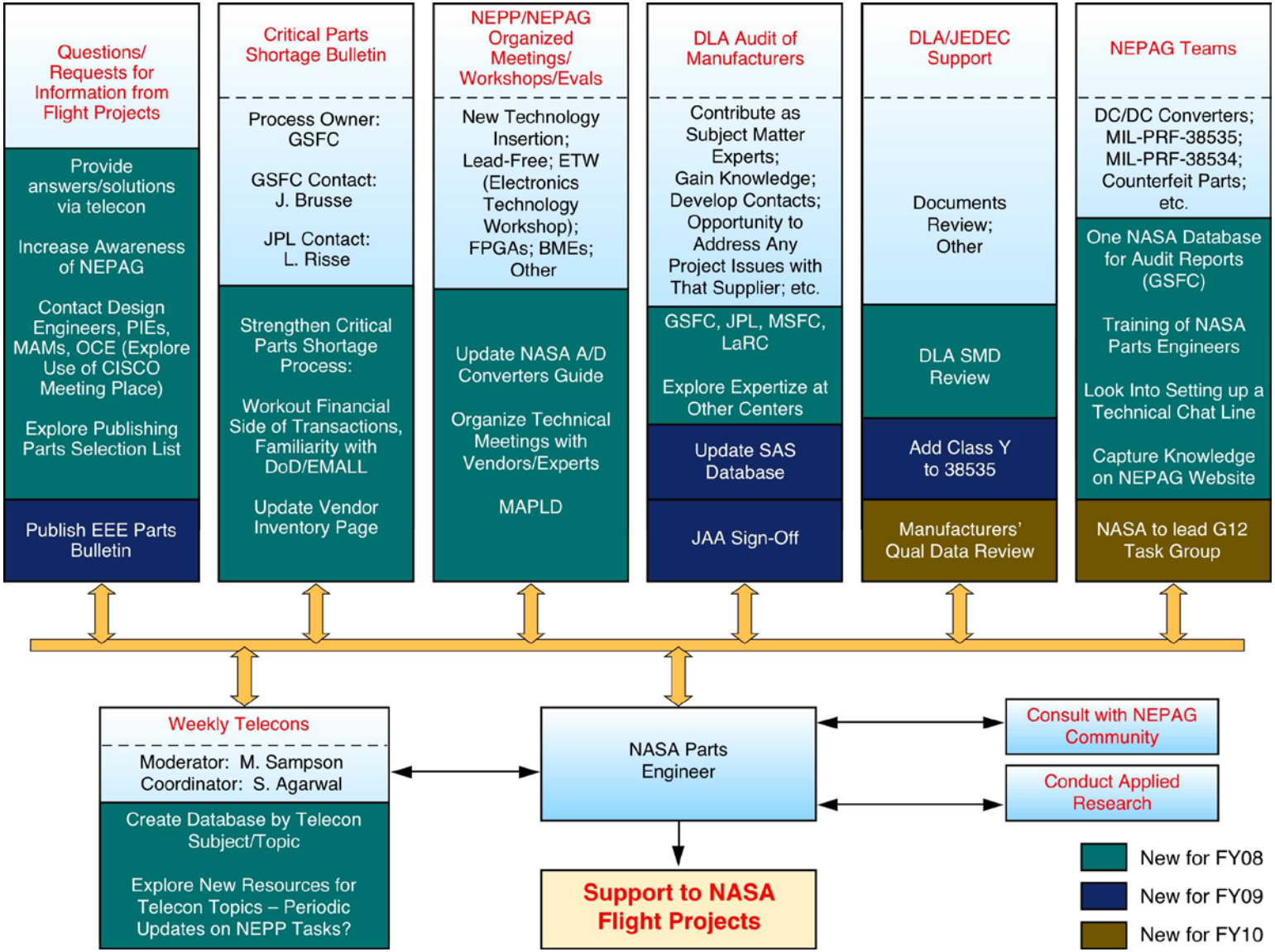
June 11-13, 2012

Mars Science Laboratory (Curiosity rover)
Launched: Nov. 26, 2011
Landing: Aug. 5, 2012

Space Parts World
A Vanishingly Small Part of the Commercial Parts World

NEPAG is actively involved with the procurement process - parts users and standards organizations join hands to ensure timely delivery of reliable parts from suppliers.

NEPAG ACTIVITIES



NEPAG
TELECONS

- **Telecons**
  - Held weekly
  - Participation
    - Domestic telecons: ~45
    - International telecons (held once a month): ~35
  - The telecons drive other NEPAG activities
  - Runs like a weekly production
  - NEPAG develops action items to follow
  - Point of contact: Roger Carlson

NEPAG
SMD REVIEWS

- **NASA Review of Pre-released SMDs for Space Products**
  - Understanding between NASA and DLA Land and Maritime-VA: NASA to provide comments within 10 days.
  - Increased co-operation from DLA Land and Maritime and the manufacturers. NASA comments are viewed by DLA Land and Maritime as essential comments.
  - The in-house experts (Parts specialists, radiation specialists, packaging specialists, reliability engineering, and others) are called upon to support this effort.
  - New technology data review
    - Suppliers using MIL-PRF-38535, Appendix H for dual use technology
    - Commercial parts developed for space customers
    - An early NASA and space community involvement in new product definition, SMD development
  - No. of SMDs reviewed in FY12: 10 (20 including new technology SMDs)
  - Total No. of SMDs reviewed in FY11: 33 (40 w/new tech SMDs).
  - Total No. of SMDs reviewed in FY10: 80; Reviewed 41 in FY09.

NEPAG
SUPPLIER AUDITS

- **DLA Audits Support**
  - DLA Land and Maritime-VQ (formerly DSCC) is the designated DoD entity that has **authority to approve or disapprove suppliers**. There are two parts to an audit: certification (capability demonstration) and qualification (successfully building product).
  - What the Agencies like NASA, Air Force, NRO bring to the audits is their **technical expertise**.
  - Audits to be supported by the space community are **decided on the NEPAG telecons**. We support them as subject matter experts, gain personal knowledge, make contacts**, resolve any flight project issues.**
  - The audit team spends a vast portion of the audit time to go on the production floor, test floor, etc. to talk to the operators, engineers, physically witness the operation or test being performed. Review supplier chain management.
  - The audit findings are reported on the NEPAG telecons. A high level summary of the audits supported by NASA is entered into the NASA **SAS** (supplier assessment system) database.
  - Only a small portion of the audits conducted by DLA are supported. **In FY11, NASA supported 39 of the 180 DLA audits** (all commodities).

NEPAG Update

- **Microcircuits**
  - Recent Findings from Audits, New Technology Data Reviews
    - **Disabled Chip Burn-ins** A recent audit for a QML device discovered that the chip was disabled during the static burn-in, thus it was not drawing any current.
      Recommendation: For new SMDs add a statement within the burn-in paragraphs stating that the parts shall be kept in their enabled state during the burn-in.
    - **Class Q 160-hr/125ºC Burn-in** This is being interpreted as a static burn-in (even for CMOS technology).
      Recommendation: Provide clarification in MIL-STD-883, Test Method 5004.
    - **At Frequency (Dynamic) Burn-ins** Test equipment limitation is being cited for not doing burn-ins at the application frequency.
      Recommendation: The burn-in task group to discuss and provide guidance. When the SMD says that the part can be used at 200 MHz, then doing burn-in at 6 MHz (cited as burn-in equipment limitation frequency) is not going to be meaningful!
    - **Two Static Burn-ins** Some manufacturers are doing electrical testing between the two static burn-ins, whereas others do electricals after completing both static burn-ins.
      Recommendation: Provide clarification in MIL-STD-883, Test Method 5004.
    - **Thermal Imaging** For a device with hot spots, the thermal resistance, junction-to-case, would be much higher than the guidelines given in MIL-STD-1835. One of the suppliers used thermal imaging to find hot spots on the die.
      Recommendation: Assign a task group to evaluate the effectiveness of thermal imaging at the product development stage.

NEPAG Update (Contd.)

– Class M

- **Removal of Class M** We have been told that class M parts with Q marking are equivalent to class Q parts. However, most SMDs from QML suppliers have both classes M and Q shown In table II of the SMDs. Is one part, one part number still a requirement?
  Recommendation: keep class Q and remove class M from the new SMDs.

5962-11203 (Draft)

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 2/ 9,10,11	1,2,3,4, 1/ 2/ 5,6,9,10,11	1,2,3, 2/ 3/ 4,5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 2/ 9,10,11	1,2,3,4,5,6, 2/ 9,10,11	1,2,3,4,5,6, 2/ 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6, 2/ 9,10,11	1,2,3,4,5,6, 2/ 9,10,11	1,2,3,4,5,6, 2/ 9,10,11
Group D end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6
Group E end-point electrical parameters (see 4.4)	1,4	1,4	1,4

1/ PDA applies to subgroup 1.
2/ See Table I for parameters tested or characterized for subgroups 1,2,3, 9, 10, and 11. Characterization is repeated after receipt of subsequent wafer lots, major design or process changes.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table I).

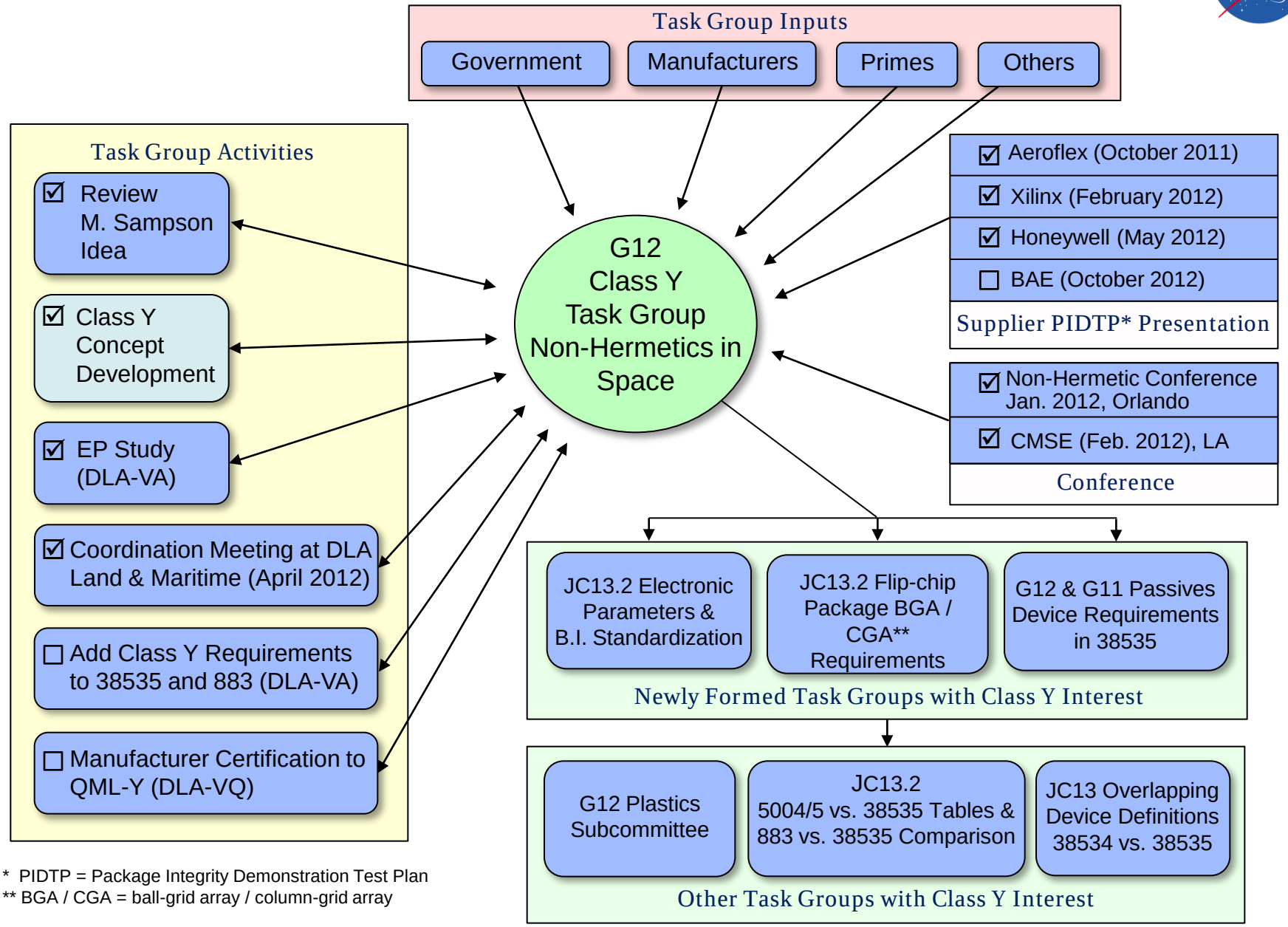
Communication with one of the suppliers (June 1, 2012)

- NASA Comment: Table IIA shows electricals for three classes: M, Q and V. Since, this is a brand new QML part and ADI will be the only supplier, you should consider offering it as Class V and Class Q. Remove Class M from the table to avoid confusion.
- Supplier's response: ADI agrees that the Class M information is unnecessary and that ADI will NOT be offering a Class M version of this part now or in the future. If Charles Saffle's group want to remove it, then ADI is fine with it. (Adding Charles and Rick Officer for their information… Rick do you want to go ahead & remove the Class M references now before we release this draft?)

MIL-PRF-38535J, Para 6.4.27 Class M.

- Items which have been subjected to and passed all applicable requirements of appendix A herein and are documented on an SMD. This product is intended for military applications.

Infusion of New Technology into the QML System
G12 Class Y Effort at a Glance



* PIDTP = Package Integrity Demonstration Test Plan
** BGA / CGA = ball-grid array / column-grid array

The Team

The **Team members** are:

- Muhammad Akbar, DLA-VA
- Larry Harzstark, Aerospace
- David Sunderland, Boeing
- Shri Agarwal, NASA/JPL
- Roger Carlson, NASA/JPL

Team resources include:

- Mike Sampson, NASA/GSFC
- Mark Porter, G12
- Brent Rhoton, JC13
- Anduin Touw, G12
- Mike Adams, DLA-VQ
- Rob Heber, DLA-VA
- Tom Hess, DLA-VA
- Charles Saffle, DLA-VA

CLASS Y - Package Integrity Demonstration Test Plan (Class Y - PIDTP) Data Sharing with the Space Community

- Presentations by Major Suppliers:
  - ☑ Aeroflex (Presented at the Class Y TG meeting in October 2011)
  - ☑ Xilinx (Presented at the TG meeting in February 2012)
  - ☑ Honeywell (Presented at the TG meeting in May 2012)
  - ☐ BAE (Scheduled for October 2012 TG meeting)
  - ☐ Other (TBD)

Class Y Team Notes from Columbus Meeting

1. Lesson learned: 1 hour at JEDEC/TechAmerica meetings is too limited for this topic.
2. We walked through the entire EP Study report, achieving consensus on most comments that should allow an update soon after April 24 (when all comments are due).
3. Post-column electrical test remains a stumbling block. Proposed that either 1-temp post-column test or 3-temp LGA test following thermal simulation of column attach process be accepted. Also discussed sample post-column testing instead of 100% screen.
4. Various mechanical and radiation tests should have the option of being performed without balls or columns, as long as a failure mode due to balls or columns is not what is being tested.
5. All tables (screening, TCI and qualification) should have side-by-side columns for Class V and Y, differing in text and format only where hermeticity issues require it. Flip-chip and solder termination issues should apply to both columns.
6. Moisture resistance test: Consensus was that Class Y should see HAST instead of TM 1004 for V, but conditions (biased or unbiased) remain open.

Notes (Contd)

7. We need a definition of package integrity demonstration plan (PIDTP), clear indication of when one is needed, and list of what one should include. Consensus was that this should go into MIL-PRF-38535 Appendix H (Qualification), and a PIDTP would be required if any of the following technologies was used: a) non-hermetic package, b) flip-chip, or c) solder terminations. PIDTP requirements would be different for each case.

8. Use of ancillary passives not compliant with MIL-PRF-123 remains a stumbling block. Most believe that specific applications (such as power supply decoupling for low-voltage FPGAs) could be approved on the basis of: a) low stress, and b) low parametric sensitivity, and that language saying so might be useful. More generally, a lot-specific qualification program seems required, and Aerospace plans to convene a group to define what that will be. Suppliers seem resistant to creating a new military specification for BME capacitors. Limitation to only capacitors could be “at this time” to facilitate including other types in product roadmaps.

9. The exercise revealed a number of issues with MIL-PRF-38535 that have nothing to do with Class Y, flip-chip, or solder terminations. Recommendations to study the relevant passages should be made to relevant subcommittees or task groups.

38535 QML Space – Current Status

		Class V (Existing)	Class Y (In Development)	Comment
QML	Need class specific PIDTP	No	Yes	
CGA**	Offered as QML	Yes	Yes	
CGA*	Need CGA specific PIDTP	Yes	Yes	same for both classes
Flip-chip*	Need Flip-chip specific PIDTP	Yes	Yes	same for both classes
Passives*	38535 Para 3.15	applies	applies	same for both classes
Passives*	Any updates for BME	would apply	would apply	same for both classes

- **Observations**
  - * represents an issue which is common to both classes
  - ** highlights the fact that CGA devices are currently offered as QMLV.
  - Despite limited resources in working this task, a meaningful QML Y product must be delivered to the flight projects in a timely manner. While the common issues are being worked, we should be able to update MIL-PRF-38535 to include Class Y requirements. This would enable the manufacturers and DLA-VQ to gear up for Class Y audits, an activity that can start now and continue in parallel with resolution of common issues, thus saving time.
- **Recommendations**
  - Upon completion of the Class Y specific actions from the coordination meeting in Columbus (PIDTP, tables and any others), DLA-VA to update 38535 with Class Y requirements and release it (keeping the requirements for common issues the same as they exist today for QMLV).
  - Keep working the common issues as quickly as possible. Continue to update the MIL documents as conclusions are reached on these issues.

PIDTP = Package Integrity Demonstration Test Plan
CGA = column-grid array BME = base metal electrode

NEPAG
EEE PARTS BULLETINS

- EEE Parts Bulletins
  - A periodic newsletter – joint effort of ATPO/NEPAG/514
  - Distribution
    - JPL/NASA centers/NEPAG: ~2000
    - QLF through Diana Shellman: ~3000
  - Approvals
    - Template has NASA approval – obtained yearly
    - Bulletin is cleared for unlimited distribution by JPL URS – each issue
  - Support
    - Assigned support: Lori Risse (514), Roger Carlson (274), Jim Okuno (FA photo)
    - Other support: Articles from NASA and JPL experts
    - Final version is approved by S. Agarwal, R. Menke, C. Barnes, M. Sampson
  - New for FY11
    - Add MDA advisories – B. Hughitt's suggestion
    - Solicit more articles from specialists across the Agency – M. Sampson's suggestion
  - Accomplishment last quarter:
    - Released March/April 2012 edition.

NEPAG
EEE PARTS BULLETINS

Draft Version

National Aeronautics and Space Administration

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the JPL/OSMS Assurance Technology Program Office (ATPO), NASA EEE Parts Assurance Group (NEPAG), and Section 514, of the Jet Propulsion Laboratory.

May/June 2012 • Volume 4 • Issue 2

Gallium Nitride – Worth the Hype

Gallium nitride (GaN) is a wide band gap (WBG) semiconductor with properties well ahead of silicon for applications where speed and power are desired. A cursory review of Table I reveals that GaN has a numerical advantage in both managing electric fields (due to the higher band gap energy and critical electric field) and device speed (due to higher drift velocity). A typical polytype of silicon carbide (SiC), the other contender for power management and distribution (PMAD), is shown for comparison. The salmon cells in Table I highlight each technology's strong points.

Table I. Comparison of power semiconductor material properties. Numbers in the table are approximate.

Property	Si	GaN	3C-SiC
Bandgap, Eg (eV at 300 K)	1.12	3.4	2.4
Critical electric field, Ec (V/cm)	2.5×10^5	3×10^6	2×10^6
Thermal conductivity, (W/cmK at 300 K)	1.5	1.3	3–4
Saturated electron drift velocity, vsat (cm/s)	1×10^7	2.5×10^7	2.5×10^7
Electron Mobility, in (cm^2/Vs)	1350	1000	1000
Hole Mobility, ip (cm^2/Vs)	480	30	40
Dielectric constant	11.9	9.5	9.7

The advantage of GaN is more readily shown in a figure of merit (FOM) graph (Figure 1). An ideal device for PMAD applications would be at the highest frequency, the right side of the graph, and the lowest FOM, which is the product of resistance of the device when on and the charge needed to invert the gate or base of the device. The theoretical limit of GaN resides significantly closer to the optimal application area. Despite these encouraging numbers, GaN does lag behind silicon in the area of thermal conductivity. This aspect of GaN will present a design challenge to any device architecture.

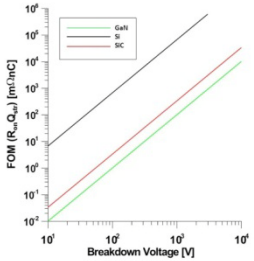


Figure 1. Theoretical limiting FOM of various PMAD technologies. Commercial silicon devices operate at their respective limit, while first-generation GaN devices are surpassing silicon.

So far, however, GaN transistors have been harder to productize into a workable alternative to silicon PMAD solutions. This lag has been due to the challenges in producing high quality GaN substrates. These challenges have recently been overcome, and devices are now becoming industrially available. Cree, EPC, RFMD, and Sumitomo are some of the manufacturers providing commercially available GaN transistors. In all of the options from the aforementioned manufacturers, the architecture is a lateral high electron mobility transistor (HEMT). Figure 2 presents a typical HEMT structure in a field-effect transistor (FET) where the conduction between the source and drain of the device occurs in a two-dimensional gas electron (2dg) and is controlled by the gate bias. This design is easier to fabricate using a silicon substrate to reduce cost and manage heat. This GaN HEMT can be very small to counter thermal issues, will be very fast, and can support current of the same magnitude as silicon power devices of comparable specification. However, some drawbacks have become evident. The nature of the HEMT structure results in a "normally on" operation, which is atypical for PMAD applications, but EPC has developed a "normally off" version of the HEMT called eGaN. Also, the gate junction in the HEMT device is very sensitive to breakdown, and therefore, voltage overstress of the gate is a serious reliability consideration. The failure in time (FIT) estimates of GaN devices are only starting to be studied, as well as the thermal and wear-out effects on

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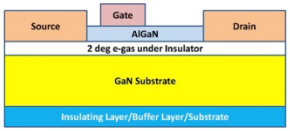

Figure 2. HEMT structure typical of a GaN FET

To fully realize the switching power of GaN, a vertical device architecture would be a considerable step forward. These would be smaller, and they would have lower parasitic inductance, higher blocking voltage, and better thermal properties. These devices would be necessarily more complex than lateral devices; however prototypical devices have been demonstrated. Further advancement to GaN FETs would be realized if gate isolation could be introduced commercially. The high gate leakage and low gate overstress bias, which are impediments to designing PMAD applications with GaN, would be removed. This advancement to GaN has been a challenge because the lattice mismatch between GaN and SiO_2 has been prohibitive to commercialization.

Because of the mass, power, and speed advantages of GaN technologies, there is increasing interest in using GaN for designing high-efficiency, low-mass power supplies for space missions. Current GaN devices have shown promising radiation hardness, and future designs should have at least the hardening potential of silicon. The aforementioned reliability issues have been assessed as presenting a diminishing risk to most space applications.

For further information, contact: **Leif Scheick (818) 354-3272**

GIDEP Alerts/Advisories

Contact your GIDEP Representative for a copy of:

Suspect Counterfeit	Exceeds 20. Contact GIDEP Rep.
Misc.	QQ8-P-12-01 Semiconductors, FSC 5961; IBZ-P-12-01 Semiconductor Device, Over-bonding, wire bond; GB4-P-12-01 Microcircuit, Memory, Digital, CMOS, Radiation Hardened Low Voltage SRAM; Y7-P-12-01 ESD Protective Packaging Materials: BRH-A-12-01 Microcircuits, Side Lobe Ringing Testing; RM-A-12-01 Leak Testing, Process

NASA parts specialists recently supported DLA Land and Maritime Audits of:

Natel Engineering Co., CA; DPA Components Int'l, CA; Maxwell Technologies, CA; Aeroflex Circuit Technology, NY; Valley Labs, CA; Preferred Testing Lab, CA; Accurate Circuit Eng., CA; BAE Systems, VA

Upcoming Meetings

- NEPP Workshop (ETW) http://www.nepp.nasa.gov/workshops/etw2012; NASA/GSFC June 11–13, 2012
- Nuclear and Space Radiation Effects Conference (NSREC) http://www.nsrec.com; Miami, FL, July 16–20, 2012

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NEPAG

NEPAG PARTICIPANTS

Backup Information

NEPAG
CRITICAL PARTS SHORTAGES

- **Critical Parts Shortages**
  - Support flight projects with their critical parts needs
  - Point of contact: Lori Risse (514)
  - Additional support
    - JPL 514 Parts Support group
  - Four Prong Approach
    - Space community wide announcement through J. Brusse (GSFC)
    - Contact manufacturers
    - Contact franchized distributors
    - Contact defense contractors through JAPC (T. Gutierrez)
  - Chance of Success
    - The above approach pretty much guarantees finding parts if they are out there and available
    - Best case example: Took only two days to find FPGAs for MIRI
  - Accomplishment this quarter: Worked with manufacturers to find parts for MARS-TGO, NASA/MSFC, NASA/GSFC.

Class Y

DLA-VA's Engineering Practice (EP) Study for Class Y is **complete**

DLA-VA hosted a coordination meeting regarding Class Y on April 12 & 13, 2012

Background

Back in 2009, there was a big push to bring the Xilinx Viirtex-4 (a non-hermetic part) into the QML system as Class V device. NASA and others were not in favor as it would have created massive confusion. Mike Sampson conceived the idea of a new Class Y for non-hermetic space parts to provide QML coverage for Xilinx Virtex-4 and similar devices.

A new G-12 Task Group, TG 2010-01, was formed in early 2010 to address non-hermetic devices for space. Shri Agarwal was asked to lead the effort.

This task was challenging because it:
- Was far more involved than typical G12 tasks,
- Required development of a brand new concept,
- Used system-on-a-chip (SoC) — one of the most complicated devices,
- Needed to be simple and easily understood,
- Possessed sketchy testing and board assembly boundaries, and
- Was needed to procure a standard QML product as quickly as possible.

Why “Class Y”?

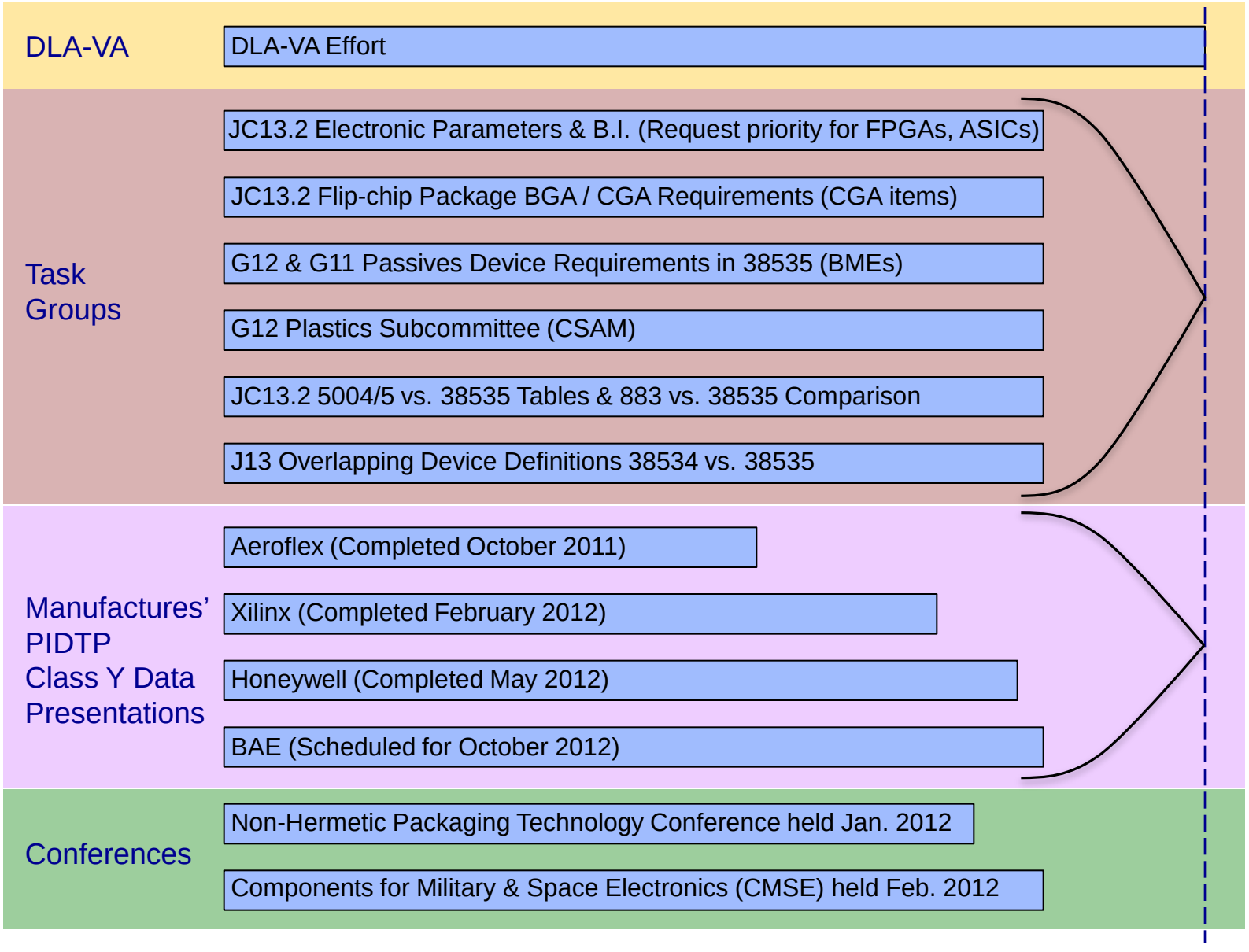
- This effort is an attempt to bring advancements in packaging technology into the QML system.
- Advancements in packaging technology, increasing functional density and increasing operating frequency have resulted in single die SoCs with non-hermetic flip-chip construction, in high-pin-count ceramic column grid array packages
  - “Poster Child” example: Virtex-4 (V-4) FPGAs from Xilinx
  - Such products were evaluated for radiation and reliability and have drawn the attention of the space user community
- Question: How do we bring V-4 and similar microcircuits into the QML system as space products?
  - It can’t be Class V because those are hermetic devices
  - Our intent is to put V-4 like products for space users in a new category: “Class Y”.
  - A year ago, G-12 opened a Task Group to develop Class Y
- What if we dropped the Class Y effort?
  - It would be a major loss for the space community and the QML program at large because the industry would be limited to ordering via Source Control Drawings (SCDs), which is counterproductive to Mission Assurance, prevents standardization, and is expensive.

G12 Class Y Task Group Summary

- The Team requested G12 approval for DLA - VA to conduct an Engineering Practice (EP) study using the detailed requirement input the Task Group has developed. This request was approved by G12.
- The Team's request for clear approval of the Task Group charter was also approved by G12. The charter statement reads:

  "This task group will develop requirements, including qualification and screening standards, for non-hermetic, ceramic-based microcircuits suitable for space applications. Initial effort will be focused on support for devices using flip-chip ceramic column grid array packaging, with resulting requirements to be submitted as a proposal for consideration to DLA Land and Maritime."
- So far 10 manufacturers have expressed interest in offering Class Y products (Xilinx, Actel, Intersil, Aeroflex, BAE, Honeywell, TI, e2v, 3D Plus, and Cypress).

Closure of QML-Y (and related) Activities



A New Trend – Supply Chain Management

Die design and fabrication	Cypress Semiconductor, San Jose, CA Cypress Semiconductor, Plymouth, Minnesota
Package design Package manufacturing	Kyocera Corporation, San Diego, CA
Wafer lap and dice	Corwil, Milpitas, CA
Assembly	DPA Components International, Simi Valley, CA
CGA column attach Solderability	Six Sigma, Milpitas, CA
Screening/electrical/package tests	DPA Components International, Simi Valley, CA
Complete electricals per SMD	Presto Engineering, San Jose, CA
Internal water vapor content	Oneida Research Services, Whitesboro, NY Pernicka Corp., Fort Collins, CO Seal Labs, El Segundo, CA
Radiation testing	J D Instruments, Albuquerque, NM

Operating Temperature Ranges, Use Caution (Not all parts guaranteed over mil temp range)

Aeroflex Memories (DLA SMD 5962-99607):

Device type	Generic number	Circuit function	Access time
01	8Q512	512K X 8-bit rad-hard low voltage SRAM (MIL Temp)	25 ns
02	8Q512	512K X 8-bit rad-hard low voltage SRAM (Extended Temp)	25 ns
03	8Q512	512K X 8-bit rad-hard low voltage SRAM (MIL Temp)	20 ns
04	8Q512	512K X 8-bit rad-hard low voltage SRAM (Extended Temp)	20 ns
05	8Q512E	512K X 8-bit rad-hard low voltage SRAM (MIL Temp)	20 ns
06	8Q512E	512K X 8-bit rad-hard low voltage SRAM (Extended Temp)	20nS

Operating case temperature, (TC) (Device 01, 03, and 05) ..... -55°C to +125°C
Operating case temperature, (TC) (Device 02, 04, and 06) ..... -40°C to +125°C

(Bottom line: This SMD is implying that there may be a yield issue at low temperatures. Use caution for operation at low temperatures. Work with the manufacturer, get product test/characterization data.)

Some other Aeroflex Memories, 5962-01533 and 5962-01511 are specified as follows: Device type 01, -40C to +125C; Device types 02 and 03, -40C to +105C. These may have yield problems at both low and high ends.