Updated Solid State Recorder (SSR) Radiation Guidelines

Ray Ladbury

Radiation Effects and Analysis Group
NASA Goddard Space Flight Center
Greenbelt, MD 20771 USA
Introduction

• Solid-State Recorder (SSR) timeline
  – 1992—first use of solid state recorder
  – 2002—First radiation guidelines for SSR use (C. Poivey for NEPP)
  – 2012—Update of guidelines

• What’s new in 2012?
  – Synchronous Dynamic Random Access Memories (SDRAMs) have dominated since late ‘90s; current generation uses 512 Mbit die
    • On-orbit data available for 64-Mbit, 256-Mbit and 512-Mbit generations
  – Next-generation will use 2nd generation Double-Data-Rate (DDR2) die
  – Memory organization has gone from x4 to x8
  – Word size increasing—32-bits is norm; some use of 64-bit
  – EDAC still dominant error correction technique
  – Decrease in # of SDRAM suppliers continues—lost Elpida this year
  – First commercial-FLASH SSR now available from Eads-Astrium
SDRAM Subtask

**Description:**
- This is a continuation task for evaluating the effects of scaling (<100nm), new materials, etc. on state-of-the-art (SOTA) mass volatile memory (VM) technologies—mainly SDRAM. The intent is:
  - To determine inherent radiation tolerance and sensitivities,
  - Identify challenges for future radiation hardening efforts,
  - Investigate new failure modes and effects, and
  - Provide data to DTRA/NASA technology modeling programs.
- Testing includes total dose, single event (proton, laser, heavy ion), proton damage (where appropriate) and reliability. Test vehicles will include a variety of volatile memory devices as available, including DDR2 SDRAMs and commercial SRAMs... and DDR3 devices.
- Emphasis for 2012 will be synergistic degradation resulting from aging and total ionizing dose (TID) response, but SEE testing also planned.

**FY12 Plans:**
- TID test structures
  - DDR2 and DDR3 SDRAMs from Samsung and Micron
  - DDR2 SDRAMs from Elpida (courtesy of 3D Plus)
- TID/reliability tests will use the new Triad Memory tester
- Test focuses
  - Evaluate potential synergistic effects of TID and SDRAM aging
    - Use thermal and voltage acceleration methods
    - Evaluate degradation due to aging/stress
    - Compare TID response of stressed to unstressed parts
- SDRAM SEE response for current generation DDR2 and DDR3 SDRAMs if funding, tester capability and time allow.

**Schedule:**

<table>
<thead>
<tr>
<th>SDRAM radiation response</th>
<th>2011</th>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>O</td>
<td>N</td>
</tr>
<tr>
<td>Part Stress Conditioning</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TID testing DDR2 + DDR3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Develop Guidelines for TID + Stress/Aging testing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delivery of final reports and Guidelines</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEE testing of DDR2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEE testing of DDR3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SDRAM Radiation Response**
- Part Stress Conditioning
- TID testing DDR2 + DDR3
- Develop Guidelines for TID + Stress/Aging testing
- Delivery of final reports and Guidelines
- SEE testing of DDR2
- SEE testing of DDR3

**Deliverables:**
- Updated SSR Radiation Guidelines
- Updated guidelines for TID testing of SDRAMs taking into account wearout mechanisms
- Test reports
- Publications
- Effects of Bias, Electrical and Thermal Stress on DDR SDRAM Total Ionizing Dose Response

**NASA and Non-NASA Organizations/Procurements:**
- Beam procurements: GSFC/REF, TAMU, LBNL
- Partners: 3D Plus, JPL, Micron, Samsung, BAE Systems

Subtask lead: Ray Ladbury

To be presented by Ray Ladbury at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on nepp.nasa.gov.
Goals

- Assess Current SEE Mitigation Techniques for SSRs
  - Current SSRs use SDRAM parts up to 512 Megabits (Mbits)

- Predict Whether Current Mitigation Techniques Adequate for Future SSR designs
  - Next Generation SSRs will use DDR2 SDRAMs

- Identify Trends and Challenges for Future SSRs
  - Candidate Parts and Vendors
  - Developments in Mitigation Techniques

- Assess Adequacy of Current Rate Estimation Techniques for State-Of-The-Art (SOTA) SDRAMs

- Update is about 90% completed
Expected Impact to Community

- Increase confidence in SSRs
  - Validate test methods of SDRAMs for use in SSRs
  - Validate SEE mitigation Techniques in SSRs
- Identify Trends for SOTA SSRs
  - Anticipate new challenges
- Capture Lessons Learned
# Single-Event Effects by Consequence

<table>
<thead>
<tr>
<th>Radiation Risk</th>
<th>Consequence</th>
<th>Remediation</th>
<th>Impact to design</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Destructive Single-Event Latchup (SEL)</strong></td>
<td>Permanent loss of 1 die in memory array</td>
<td>Redundant die in array such that probability of meeting End-of-Life (EOL) requirements is high</td>
<td>Severe</td>
</tr>
<tr>
<td><strong>Nondestructive SEL</strong></td>
<td>Loss of all data on affected die/stack</td>
<td>Requires power cycle of affected die/stack for recovery</td>
<td>Moderate to severe</td>
</tr>
<tr>
<td><strong>Single-Event Functional Interrupt (SEFI) requiring power cycle</strong></td>
<td>Loss of functionality on affected die; Loss of most or all data on affected die/stacks</td>
<td>Requires power cycle of affected die/stack for recovery; EDAC may</td>
<td>Moderate to severe</td>
</tr>
<tr>
<td><strong>Recoverable SEFI</strong></td>
<td>Temporary loss of functionality; Loss of large amounts up to all data on affected die.</td>
<td>EDAC + Organization of data words across independent die; FPGA programmed w/ ability to refresh mode registers/reset device</td>
<td>Moderate</td>
</tr>
<tr>
<td><strong>Stuck Bits</strong></td>
<td>Uncorrectable loss of data integrity in affected bits/symbols</td>
<td>EDAC can correct incorrect bit, but capability permanently degraded</td>
<td>Minor</td>
</tr>
<tr>
<td><strong>Multi-Bit Single-Event Upset (SEU)</strong></td>
<td>Correctable loss of data for multiple bits in same word</td>
<td>EDAC must have sufficient power to correct w/c MBU (usually no worse than w/c SEFI)</td>
<td>Moderate</td>
</tr>
<tr>
<td><strong>Multi-Cell SEU</strong></td>
<td>Multiple bits upset, but in different words</td>
<td>EDAC</td>
<td>Minor</td>
</tr>
<tr>
<td><strong>SEU</strong></td>
<td>Single-bit upset</td>
<td>EDAC</td>
<td>Minor</td>
</tr>
</tbody>
</table>
Design Considerations

- Data stored in k-bit words, broken into n-bit symbols, 1 per part
- EDAC corrects m symbols
- If total symbol error rate = R, uncorrectable error rate ~ R^{m+1}
- Part with destructive SEL requires more die to meet EOL needs
- If SDRAM die are stacked, treat each stack as a “part”
  - Caveat—die in a stack have a common power supply, making it impossible to monitor overcurrent or cycle power to a single die.

FPGA or ASIC
- Supplies data, clock and control signals to memories
- Corrects errors in data
- Monitors health of array and manages data storage

To be presented by Ray Ladbury at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on nepp.nasa.gov.
SSRs: The Current Generation

Ratio Predicted to Observed SEU Rate

Current Rate Estimation Tools adequate to bound SEU rates

- 64 Mbit Samsung
- 128 Mbit Samsung
- 256 Mbit Elpida
- 512 Mbit Elpida

To be presented by Ray Ladbury at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on nepp.nasa.gov.
On-Orbit Data For LRO SSR

- SSR for Lunar Reconnaissance Orbiter (LRO) provides a check on predicted rates
  - >730000 device-days

- Where statistics are good, observed SEE rate agrees with prediction
  - The more disruptive or rare the event, the worse the statistics are for error prediction
- On-orbit data limits now more stringent on SEFI and stuck bits than those from accelerator data

<table>
<thead>
<tr>
<th>Error Mode</th>
<th>Predicted</th>
<th>Observed</th>
<th>Ratio: Obs/Pred.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEU</td>
<td>0.0154</td>
<td>0.0031</td>
<td>0.2012987</td>
</tr>
<tr>
<td>Logic Errors</td>
<td>0.01</td>
<td>0.00017</td>
<td>0.017</td>
</tr>
<tr>
<td>Block Errors</td>
<td>0.00035</td>
<td>0.000033</td>
<td>0.0942857</td>
</tr>
<tr>
<td>SEFI</td>
<td>&lt;8E-6</td>
<td>&lt;6.5E-6</td>
<td>XXXXXXX</td>
</tr>
<tr>
<td>Stuck Bit</td>
<td>&lt;1E-5</td>
<td>XXXXXXX</td>
<td></td>
</tr>
</tbody>
</table>

![Graph showing SEE cross section vs LET (MeV·cm²/mg)]
More LRO Data Analysis

TAMU Data for Elpida SDRAM

- As in heavy-ion test, majority of errors come in burst/block errors
  - 14 events account for >90% of errors
- No data lost to date using Reed-Solomon 2-nibble correction (x4 configuration)
  - No SEFIs requiring power cycle
SSR Components: Next Generation

- Next-Generation SSRs will use DDR2 and DDR3 components
  - Test data for these parts are sparse
    - 800-1600 GHz speeds make parts a challenge to test as well as to use.
  - Hits to Phase-Lock Loop (PLL) likely cause of Burst Errors seen at low LET
    - Some SRR designs will have PLL disabled
  - Using full speed of DDR2/3 parts will require very fast controllers

---


New Challenges for SSRs

- Most challenges arise due to increased density and Integration
  - Increased density of SDRAM die
    - Progression from 512 Mbit to 4 Gbit means increased correction load for EDAC—increased correction cycles or increased vulnerability
    - $\times 4$ die are now uncommon; $\times 8$, $\times 16$ more readily available
      - Larger data words easier to implement on wider die
      - Common EDACs can correct ~2 nibbles in error—that’s 2 WC SEFIs on $\times 4$, but only 1 on a $\times 8$
      - EDAC that can correct 4 nibbles tends to be complicated
  - Stacked Die
    - Makes it difficult to SEL by overcurrent; SEL protection not possible
    - If SEFI requires power cycle, all data on stack is lost
    - Data not lost if memory is nonvolatile
- Rising rates for Block/Burst Errors means more worst-case errors
  - Increased correction burden
- Fewer vendors means fewer chances of hardness by serendipity
Conclusions

• Current error mitigation approaches yield robust data integrity for SSR designs used to date.

• SEE rate estimation tools are adequate at least to 512 Mbit generation of SDRAMs
  – Poor statistics due to disruptive nature or rarity account for conservative nature of predictions for block data and SEFI modes

• Challenges upcoming
  – DDR2/3 SDRAMs exhibit a broad range of SEFI/block error behavior
  – SEFIs and block errors account for increasing share of bit flips
  – Data words and memory organization increasing in complexity
    • Makes implementing EDAC a challenge
  – Stacking of parts increased data loss during recovery from “unrecoverable SEFI”

• In Passing
  – EADS Astrium has developed a Flash based SSR
    • Nonvolatile nature of storage cells has advantages for error recovery, but FLASH has its own challenges

• Current mitigation strategies likely to persist for foreseeable future