MRAM Technology and Status

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What is an MRAM?

**MRAM = Magnetoresistive RAM**

- WRITE using magnetic hysteresis.
- READ using magnetoresistance.
- Built on CMOS. TSOP packages (or ceramic flat-pack for space)
- Architecture similar to SRAM.
- First memory to use magnetic structures exploiting electron **SPIN** as well as CHARGE.
- Future technologies have potential for very HIGH DENSITIES.
- MEMORY CELLS are nonvolatile (unlimited retention) and immune to radiation-induced upset. Also unlimited endurance.
MRAM: The Ideal Memory?

- DRAM Density
- SRAM Speed
- NAND Nonvolatility
- Rad-Hard Memory Cells

Potential to be first nonvolatile Gb memory with unlimited endurance and 20+ year retention (and SEU immunity bonus)
Spintronics

MRAM, The Spintronic Memory

Traditional Memory

- Bulk Movement/Storage of Electrons

Spintronics

- Exploitation of Electron Spin and Resulting Magnetic Moment

Information is carried by electron spin in addition to, or in place of its charge.

Ref [1]
Read: Magnetoresistance (MR)

Types of magnetoresistance (MR):

<table>
<thead>
<tr>
<th>Name</th>
<th>Increase in Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ordinary (OMR)</td>
<td>2%</td>
</tr>
<tr>
<td>Giant (GMR)</td>
<td>50%</td>
</tr>
<tr>
<td>Colossal (CMR)</td>
<td>99.9%</td>
</tr>
<tr>
<td>Tunnel (TMR)</td>
<td>200%</td>
</tr>
</tbody>
</table>

Modern “MTJ” MRAMs
“Ordinary” Magnetoresistance Effect

Resistance of material changes with applied magnetic field.

Corbino Disc

Magnetic field adds circular current component $I_\theta$ and creates resistance to radial component $I_\rho$.

Increased resistance is due to Lorentz Force:

\[ \mathbf{F} = q(\mathbf{E} + \mathbf{v} \times \mathbf{B}) \]

Also known as “anisotropic magnetoresistance” (AMR) because effect is 0 when current and B are parallel and maximum when perpendicular.

Change in resistance is proportional to $B^2$ (Kohler’s Rule):

\[ \frac{\hat{\partial} \rho}{\rho} \propto a \left[ \frac{H}{\rho} \right]^2 \]

Effect discovered by Lord Kelvin in 1856.

Ref [2]

Ref [3]
“Giant” Magnetoresistance

Birth of “spintronics”

- A much larger magnetoresistance effect (up to 50%) observed in thin-film structures composed of alternating ferromagnetic and non-magnetic layers (e.g. Fe/Cr/Fe). Thicknesses in nm.

- Current passes parallel to layers: current in plane (CIP).

- Resistance of material is affected by alignment of magnetic moments of magnetic materials which creates changes in scattering of spin up or spin down electrons.

- In practical application as memory cell, change in resistance is too small (4-8%). Not good enough for high density memory.

The 2007 Nobel Prize in physics was awarded to Albert Fert and Peter Grünberg for the discovery of GMR, which they did (independently) in the 1980s.

Disc Head Readers

- Using pinning layer also known as “spin valve” structure

- Discussed by IBM and published in 1991. Modern MRAM is derivative of this structure.
“Colossal” Magnetoresistance

- Very large change in resistance under magnetic field observed mostly in certain manganese oxide compounds

- First seen in 1950s by Jonker and Stanten (Philips)

- Effect not well understood

- Materials not to be seen in MRAM (or any other electronics) any time soon

Resistance has recently been discovered in La1-x
Sm. The largest effects have been observed for x=0.1, where the resistance changes by 99.9%. Figure 14 shows that the resistivity of the material undergoes a low temperature behavior. The colossal magnetoresistance effect has been shown that the insulating to metal transition is complete at 95%. This resistance reduction is relative to the field dependence of the resistance. These issues will be the focus of future research.
Magnetic Tunnel Junction (MTJ) Cell Structures

- Two layers of magnetic metal (such as cobalt-iron) separated by a layer of insulator (typically aluminum oxide, ~1 nm)

- Tunneling Magnetoresistance
  - Consequence of spin-dependent tunneling
MTJ Drawbacks

Scaling Issues
- Smaller bits are more susceptible to thermal fluctuations

Complicated Lithography

1st Gen: MTJ Cell

2nd Gen: STT Cell

Ref [9]
MRAM Future: Thermally Assisted Switching (TAS)

• Idea is to heat the cell, which lowers the strength of the required magnetic fields for switching

• Advantages:
  – Eliminates write selectivity problems: write select is temperature driven
  – Lower power: only one magnetic field required for write
  – It is thermally stable due to the exchange bias of the storage layer.

• Main Advocate: Crocus (Spintec spin-off): Just received $300M to build factory in Russia.
MRAM Future: Spin Torque Transfer (STT)

- Advantages:
  - Lower Power Consumption
  - Better Scalability
  - Simpler Cells

Ref [8]
SRAM-like Operation

**MRAM Read**

**MRAM Write**

**SRAM Read**

**SRAM Write**
Device Reliability: 1 Mb Everspin (JPL)

- Unlimited Endurance
- 20+ year Retention
- Low susceptibility to external magnetic fields
- -55 to 125 C operation (E2V upscreen)
  - Sold by Everspin as -45 to 130C

B field measurements at JPL

Bit Errors Vs B Field

~25 mT
Radiation Effects - JPL

A 1 Mbit MRAM die packaged in a 40-pin dual-in-package (DIP) for SEL testing (top) and thin-small-outline-package (TSOP) for TID testing (bottom).

<table>
<thead>
<tr>
<th>Run #</th>
<th>Device</th>
<th>Energy (MeV/AMU)</th>
<th>Energy (MeV)</th>
<th>Ion</th>
<th>Eff. LET</th>
<th>Run Time (s)</th>
<th>Fluence</th>
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<td>1</td>
<td>25</td>
<td>1766</td>
<td>Kr</td>
<td>21</td>
<td>177</td>
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<td>2</td>
<td>1</td>
<td>25</td>
<td>1766</td>
<td>Kr</td>
<td>21</td>
<td>242</td>
<td>3.0E+06</td>
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<tr>
<td>3</td>
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<td>25</td>
<td>1766</td>
<td>Kr</td>
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<td>51</td>
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<td>Xe</td>
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<td>8</td>
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<td>Au</td>
<td>84</td>
<td>54</td>
<td>1.0E+07</td>
</tr>
</tbody>
</table>

Ion beams used for SEL testing. No latchup observed during any testing.

Ref [10]
## Memory Comparison

<table>
<thead>
<tr>
<th></th>
<th>SRAM</th>
<th>DRAM</th>
<th>NOR Flash</th>
<th>NAND Flash</th>
<th>FRAM</th>
<th>PRAM</th>
<th>MTJ MRAM</th>
<th>STT MRAM</th>
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<tbody>
<tr>
<td>Density</td>
<td>144 Mb</td>
<td>8 Gb</td>
<td>1 Gb</td>
<td>64 Gb</td>
<td>4 Mb</td>
<td>512 Mb</td>
<td>16 Mb</td>
<td>Gb?</td>
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<tr>
<td>Access Time</td>
<td>&lt;1 ns</td>
<td>260 ps</td>
<td>25 ns</td>
<td>20 ns</td>
<td>55 ns</td>
<td>16 ns</td>
<td>35 ns</td>
<td>&lt;10?</td>
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<tr>
<td>Standby I (mA)</td>
<td>2</td>
<td>150</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
</tr>
<tr>
<td>Read I (mA)</td>
<td>100</td>
<td>100</td>
<td>20</td>
<td>25</td>
<td>&lt;10</td>
<td>16</td>
<td>30</td>
<td>15?</td>
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<tr>
<td>Write I (mA)</td>
<td>100</td>
<td>100</td>
<td>50</td>
<td>25</td>
<td>&lt;10</td>
<td>20</td>
<td>30</td>
<td>15?</td>
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<tr>
<td>Endurance</td>
<td>Infinite</td>
<td>Infinite</td>
<td>100k</td>
<td>0.5-100k</td>
<td>10^{14}</td>
<td>10^6</td>
<td>Infinite</td>
<td>Infinite</td>
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<tr>
<td>Retention</td>
<td>~0</td>
<td>~0</td>
<td>&gt;10 yrs</td>
<td>&gt;10 yrs</td>
<td>&gt;10 yrs</td>
<td>&gt;10 yrs</td>
<td>&gt;20 yrs</td>
<td>&gt;20 yrs</td>
</tr>
<tr>
<td>Cell Size (F^2)</td>
<td>100</td>
<td>8</td>
<td>6</td>
<td>5</td>
<td>10</td>
<td>6</td>
<td>10</td>
<td>&lt;4?</td>
</tr>
<tr>
<td>Rad-Hard Cell</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✔</td>
<td>✗</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>Cost/ Mb ($)</td>
<td>2</td>
<td>.0004</td>
<td>.01</td>
<td>.0002</td>
<td>10</td>
<td>.05</td>
<td>1.5</td>
<td>?</td>
</tr>
</tbody>
</table>
Applications

Wherever nonvolatility, quick booting, high endurance, and/or radiation-hardness are important.

- **Home Computing**
  - Quick boot discs, similar to Flash

- **Mobile Computing**
  - Nonvolatility

- **Military/Space**
  - Nonvolatile, Rad-Hard

- **RFID**
  - Embedded MRAM
MRAM Players (Past and Present)
MRAM Areas of Focus

Commercial MTJ Vendors
- Everspin
- E2V (Everspin Upscreen)

Commercial Rad-Hard MTJ
- Honeywell
- Aeroflex

MTJ IP
- NVE
- Spintec

Thermally Assisted Technology (TAS) R&D
- Crocus, IBM
- Spintec

Inactive
- Motorola (2005, spun off Freescale)
- Freescale (2008, spun off Everspin)
- Infineon (~2006)
- Cypress (2005)

Spin Transfer Torque (STT) R&D
- IBM
- Samsung
- Hynix-Grandis
- Everspin
- Avalanche Technology (CA start-up)
- Spin Transfer Technologies (NYU start-up)
- Intel
- NEC
- Renesas
- Fujitsu
- Toshiba
- Micron, A*Star (Singapore)
## MRAM Product Roadmap

<table>
<thead>
<tr>
<th>Year</th>
<th>Device</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>2004</td>
<td>4 Mb MTJ</td>
<td>Freescale</td>
</tr>
<tr>
<td>2005</td>
<td>1 Mb MTJ Rad-hard</td>
<td>Honeywell</td>
</tr>
<tr>
<td>2005</td>
<td>STT MRAM Prototype</td>
<td>Sony</td>
</tr>
<tr>
<td>2009</td>
<td>32 Mb STT MRAM Prototype</td>
<td>Hitachi</td>
</tr>
<tr>
<td>2010</td>
<td>4/16 Mb MTJ Rad-hard</td>
<td>Aeroflex</td>
</tr>
<tr>
<td>2012?</td>
<td>16/64 Mb Rad-hard QML Class V</td>
<td>Aeroflex/Honeywell</td>
</tr>
<tr>
<td>2015?</td>
<td>Gb STT</td>
<td>Toshiba</td>
</tr>
</tbody>
</table>
Flight Heritage - SpriteSat

- SpriteSat – Tohoku University, Japan
- Various Payloads/Launches Since 2008
- 4 Mb Freescale devices
- Replacing Flash and SRAM with MRAM

Flight Heritage – CubeSat - COVE (JPL)

- Launch October 2011 (Ref: 11)
- CubeSat On-board Processing Validation Experiment, “COVE”
- Secondary Payload on University of Michigan M-Cubed CubeSat
- Included:
  - Xilinx Virtex-5QV FPGA
  - Everspin MR4A16B MRAM (4 Mb)
  - Numonyx P5QPCM PRAM (128 Mb)
- First attempt: NPOESS Prepatory Project (NPP)
- M-Cubed did not separate from another CubeSat, Explorer 1-Prime
  - Although beacons have been heard, University of Michigan team has been unable to send commands to satellite.
Sources/References


