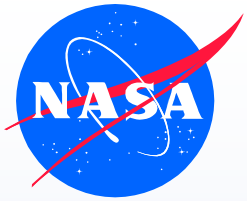
National Aeronautics
and Space Administration



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DDR2 Device Reliability Update

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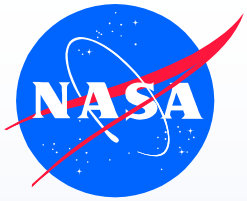
Outline

- Background
- Reliability Qualification Approach
- Test Equipment
- Recap of Last Year's Results
- Initial DIMM Results

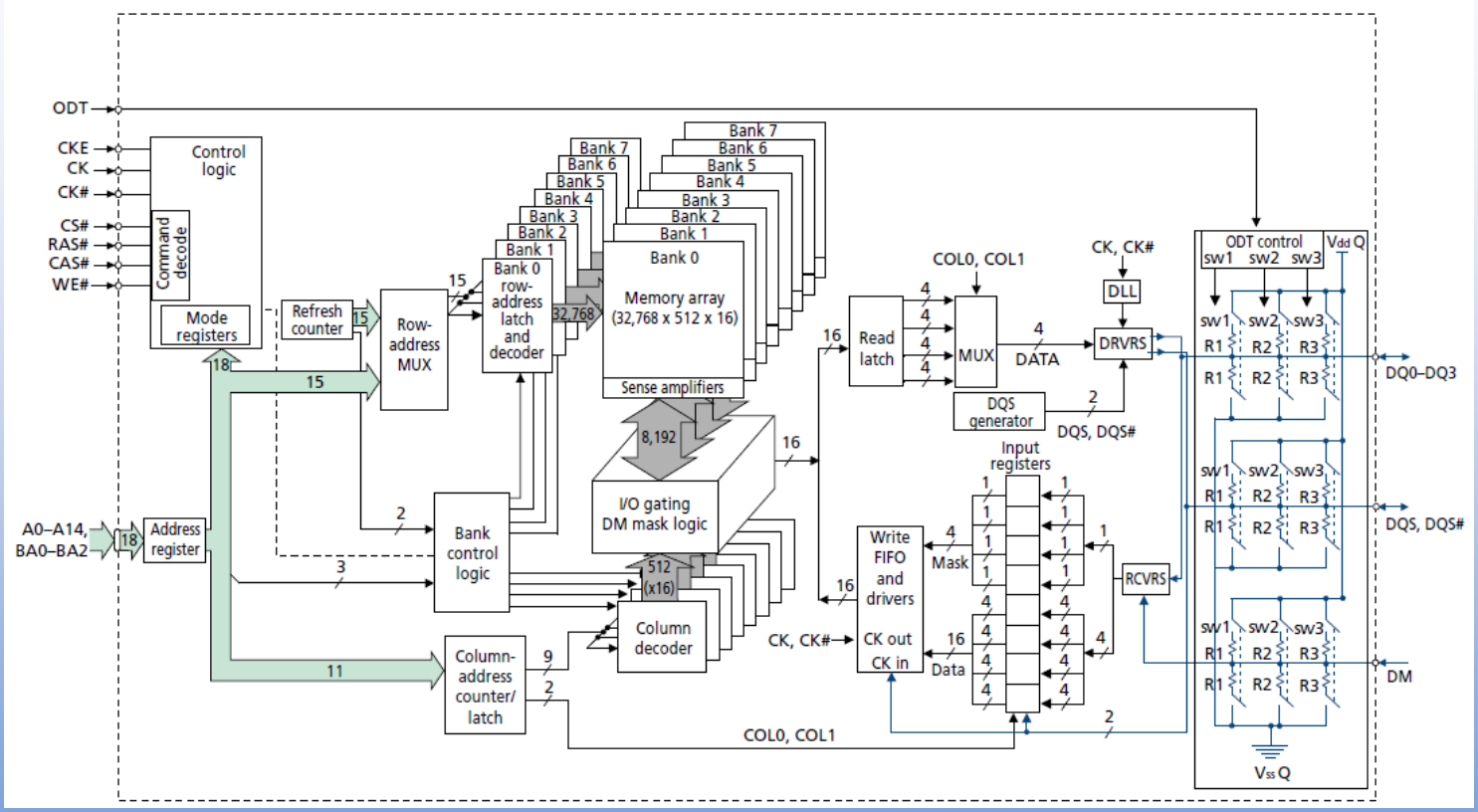


General Reliability

- General reliability is interested in the failure modes that will manifest as a result of any environment, age, or usage parameters

- But manufacturers devote significant resources to testing these devices – why do we need to test, and how are we different?
  - On a device-by-device basis, we have much more time to screen all parts.
  - Ability to identify outlying devices is a useful screening method that can be applied to devices used in space
  - Certain parameters of NASA use may be outside of standard usage – long life, extreme environments, off-spec sheet use
  - We need to be knowledgeable about running these devices to support program questions

Device Complexity



- Many different types of structures:
  - DRAM Cells, Registers, Buffers, Drivers, Voltage Regulators, Charge Pumps, Functional blocks: CRC, Pipelines, State Machines
  - Each has its own failure risk and parameter dependencies

Approach

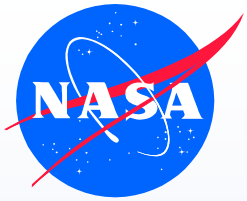
- Use acceptance testing to establish outliers
  - 100's of test hours per device possible
  - Compared to minutes or less by manufacturer
- Perform accelerated life testing
  - Establish failure mechanisms of a given lot
  - Determine if the lot meets requirements

Test Matrix

$$X\left(p, M, F(t), Pat(t), V, T, f, D, S(t)\right) = \begin{cases} Pass\,/\,Fail \\ Range \\ Limit \\ \#\,Counts \end{cases}$$

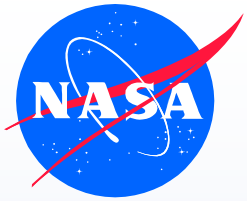
- General reliability testing covers a vast set of target parametrics and operating parameters
  - p – parameter (e.g. data access time)
  - M – device mode
  - F(t) – device function during test
  - Pat(t) – data pattern during test
  - V – operating bias
  - T – environment temperature
  - f – clock rate
  - D – duty cycle
  - S(t) – stress history of device
- In addition:
  - # of test devices in sample
  - # of desired manufacturers
  - # of test lots

General reliability test matrix is intractable - it requires targeted selection of tested elements.



Things to Measure

- Presently we do the following
  - Monitor current under different operating modes
  - Extract the cell retention time
  - Examine changes over 1000 hour stress test
- We are working towards (up-screen/life test)
  - Examine leakage current on I/Os
  - Determine output voltages
  - Determine the operating frequency range
  - Run pattern-based screening tests



Pattern Dependency

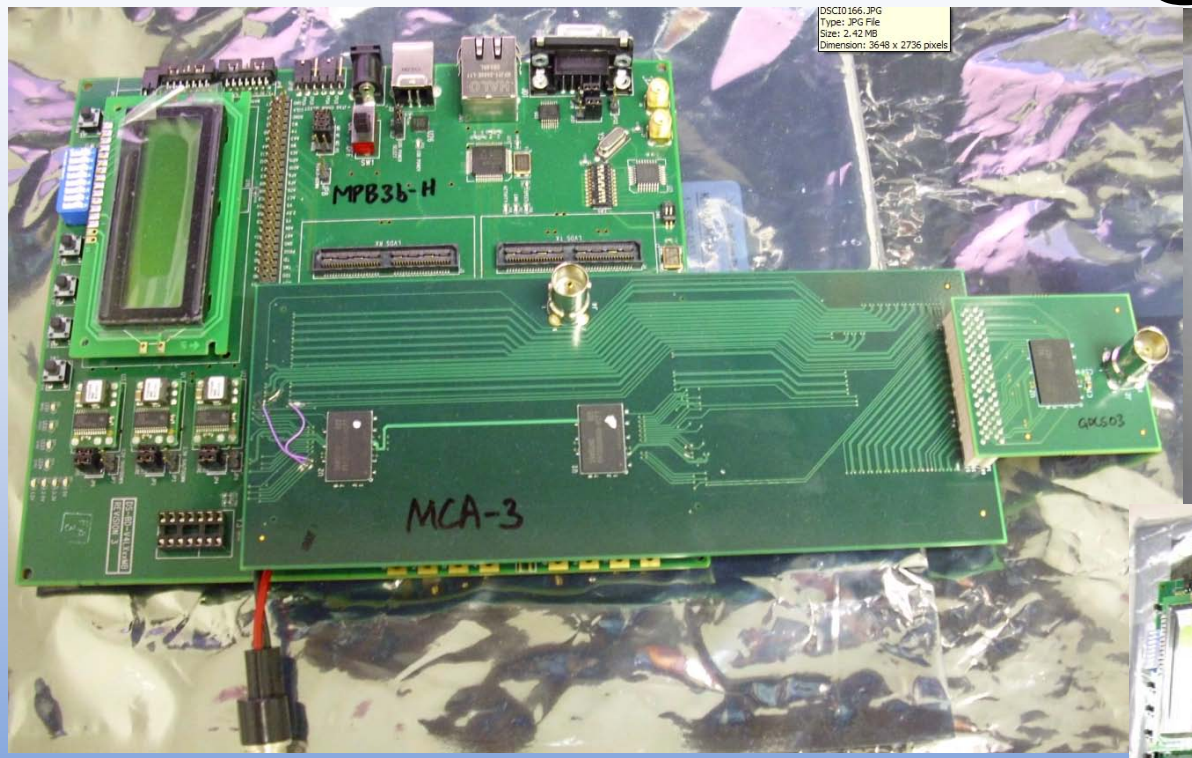
- DRAM storage arrays may have complex pattern dependency
  - Time intensive
  - Huge space of potential patterns
  - Cell retention can be related to pattern used

- Will be invaluable for handling flight anomalies
  - Any observed pattern dependencies during testing can be applied to flight
  - Ability to rule out reliability at a source of flight anomalies is useful

Moving to DIMMs

- Pros
  - Very low cost per device (~10$ vs. ~200$)
  - Interchangeable between testers (standard)
    - Enables many types of testing to establish device details
- Cons
  - Impossible to measure individual power
  - All devices on same DIMM in same exposure group
  - Difficult to get desired device parameters
- Bottom Line
  - Will provide a good way to sample many different types of issues
  - May provide good data but are not a vehicle for buying flight parts
  - Test equipment may be viable for flight acceptance…

Test Resources @ JPL



Clockwise: Single DUT tester, mounting in environment chamber, multi-DUT chamber

- Uses JPL's DUT mounting design

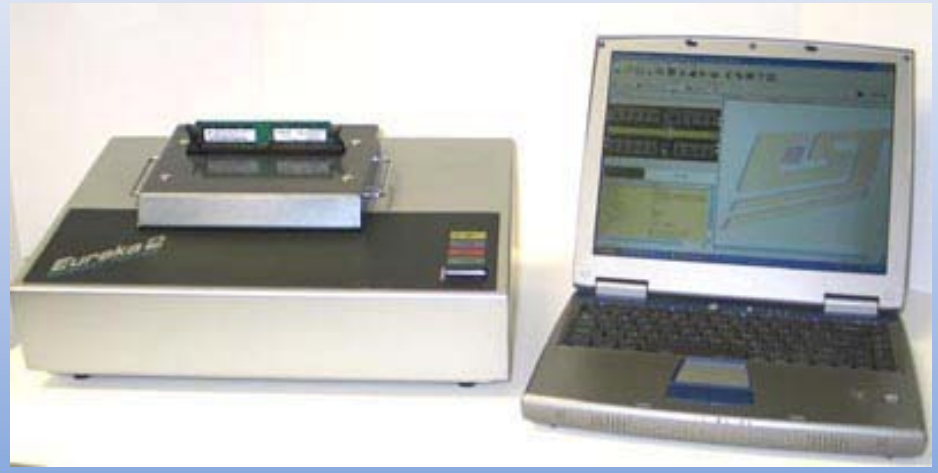
Test Resources @ JPL

- Credence D10 is a high-capability tester (up to 400MHz, but not well suited to run DUTs at high speed due to expense of interface board)
- Good for testing detailed timing parameters, leakage currents, and I/O voltage levels.
- Life testing, high speed operation, and pattern-dependent characterization of devices will still require other resources

Plan to have this online for individual parts in August 2012

Eureka Tester

- Added an industrial DDR2 DIMM tester
  - Performs standard acceptance tests on DIMMs
  - Frequency range, standard pattern sensitivity



- Also built adapter between loose test parts
  - Interchangeable with functional & parameter testers

DIMM Adapter

- Built adapter to connect to custom test system
- Will be used to perform:
  - Cell retention time studies with several patterns
  - Enable testing in thermal chambers up to 9 DIMMs at a time

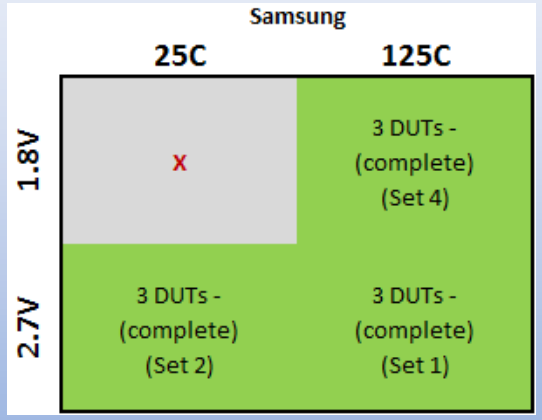
Interoperability

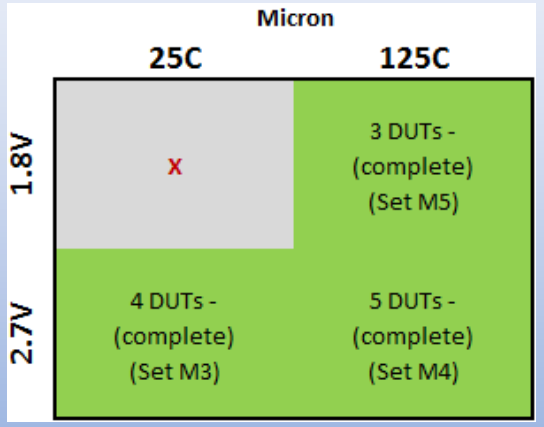
- Loose parts:
  - Can work on all systems with use of DIMM adapter –

- DIMMs:
  - Can only be used on industrial tester (Eureka) and JPL memory functional tester

Last Year's Testing

- Test Matrix: 78nm 2Gb DDR2 devices

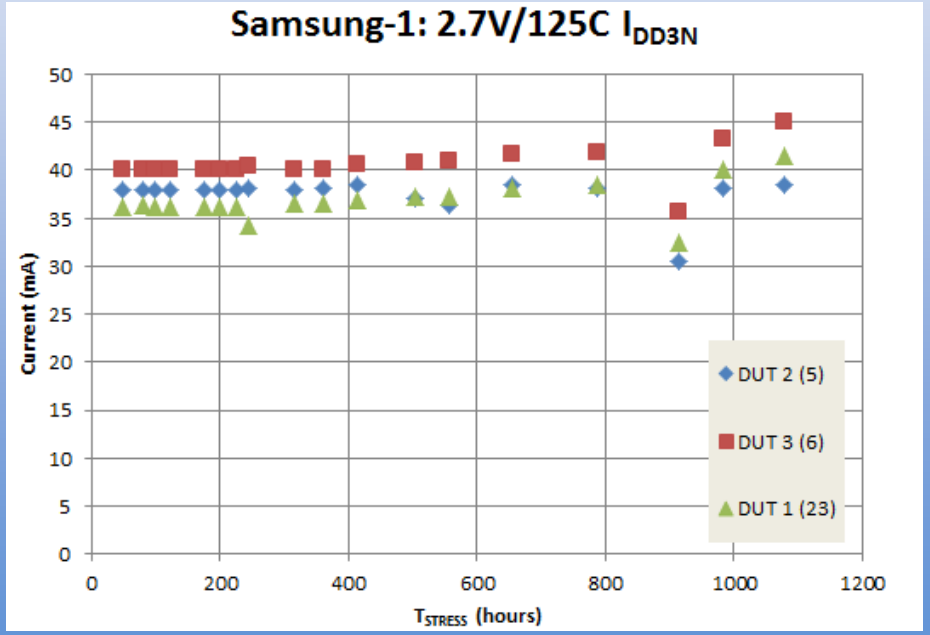


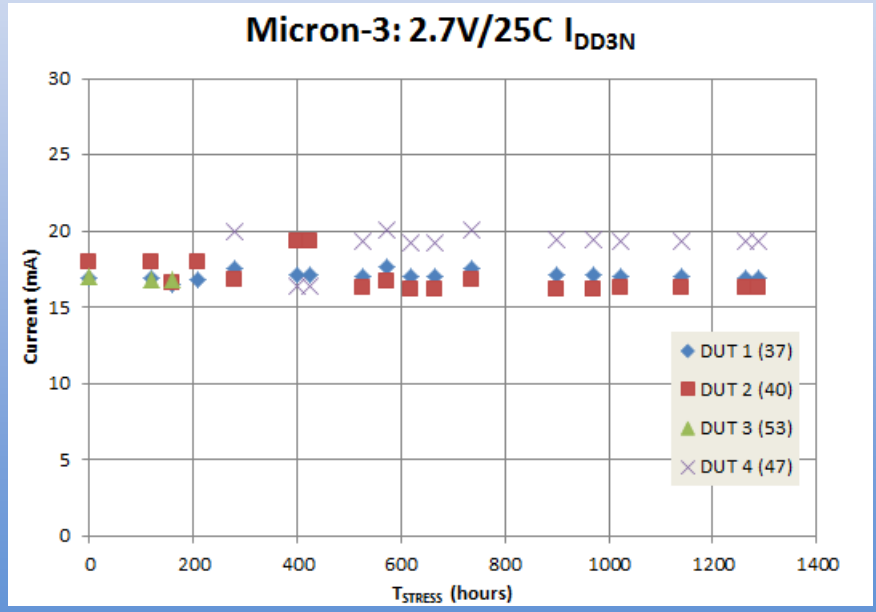


- Testing at 2.7V hindered by internal regulation
- Micron devices at 2.7V had 3 failures, but the statistics are low

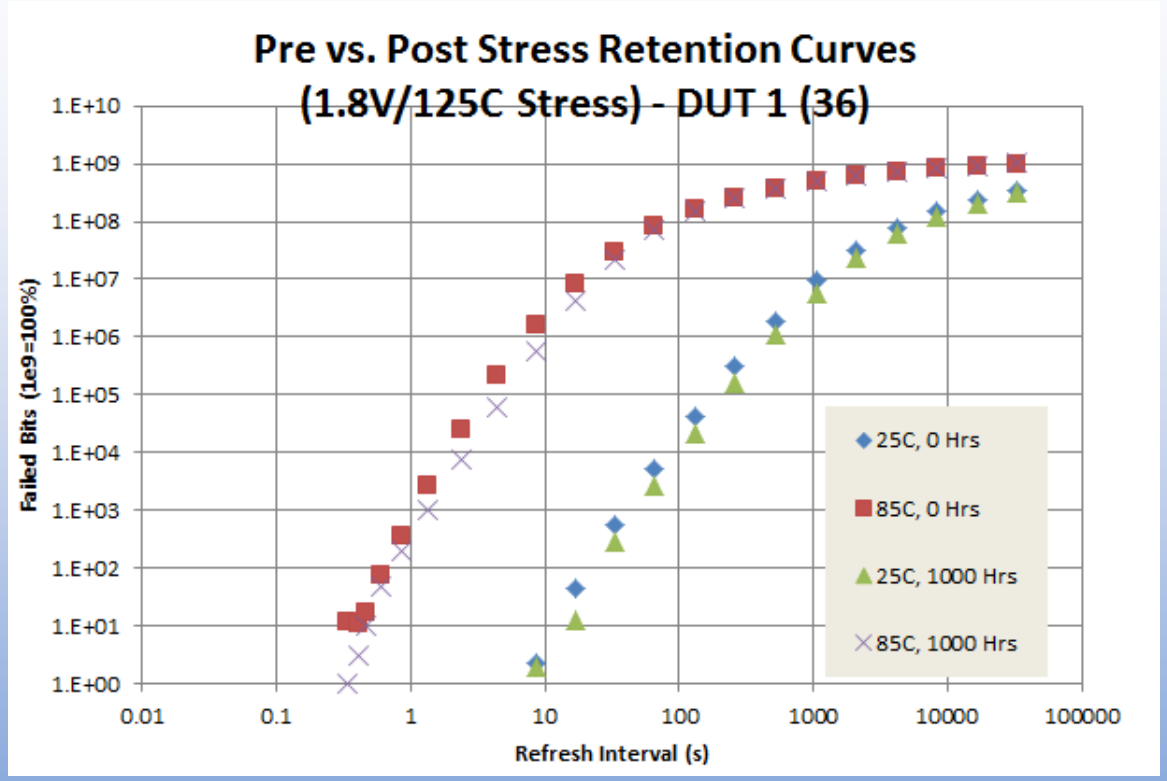
Minor Device Degradation

- Observed operational currents did not degrade significantly over 1000 hours at 2.7V and/or 125°C
- Abrupt jumps due to difficulty with 2.7V Operation





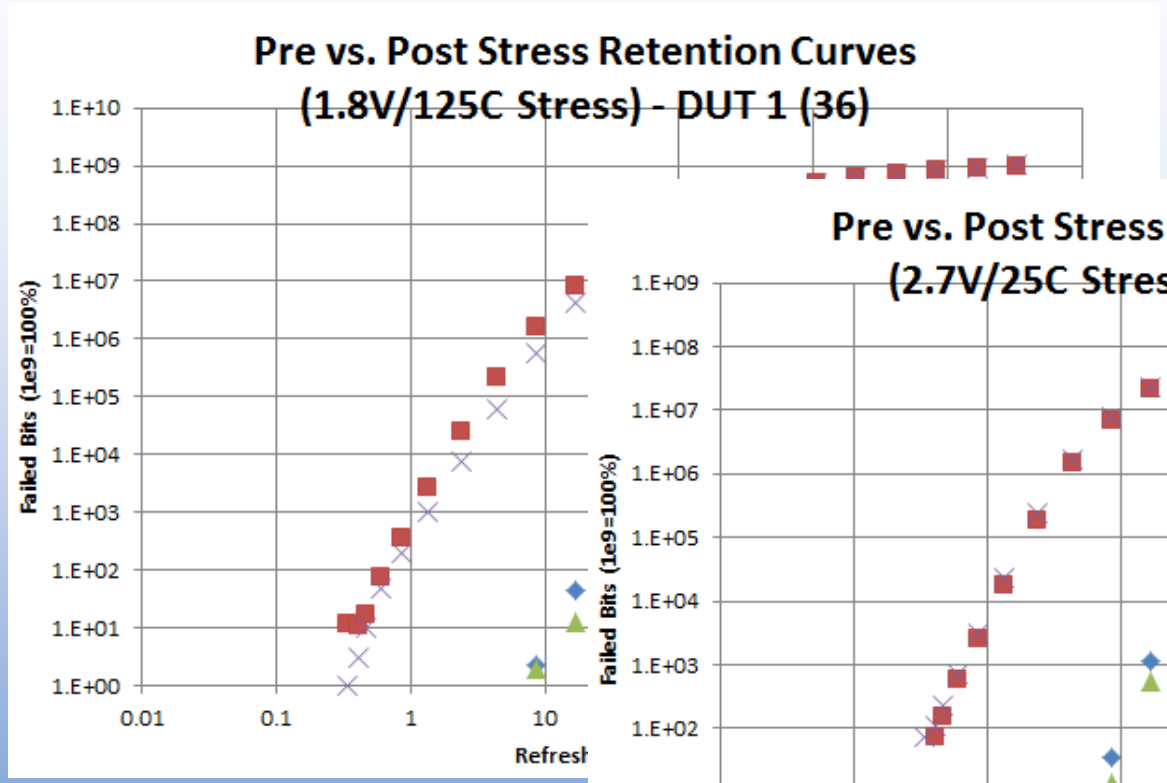
Test Efforts

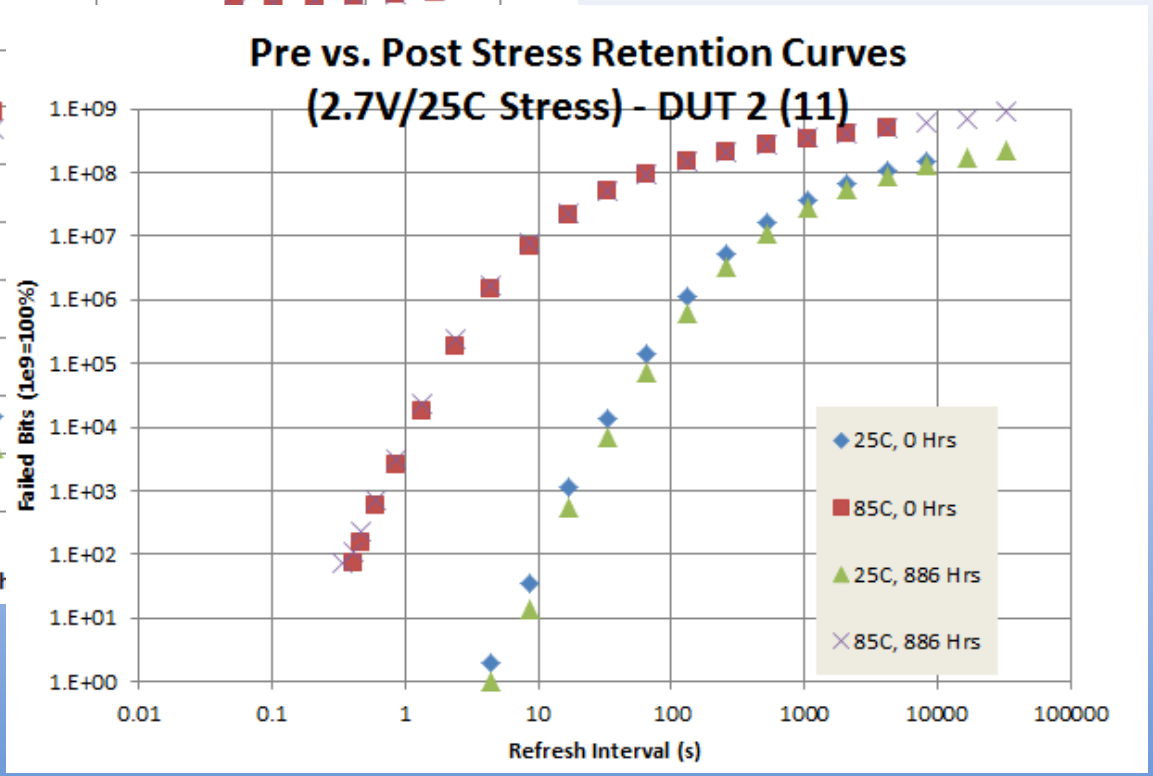


- Micron – Typical 125°C behavior
- Limited imprinting was apparent in Micron devices

25°C Measurement has thermal uncertainty (Explains change at 25°C)

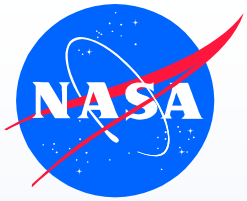
Test Efforts





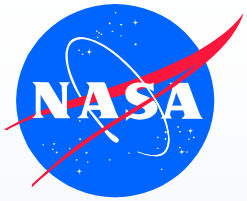
- Micron – Typical 125°C behavior
- Limited imprinting was apparent in Micron devices

- Samsung – Typical
- Pre/Post Stress – No apparent change



Summary of Results

- Performed 1000 hour testing at 1.8 and 2.7 V as well as 25 and 125°C
- Acceleration showed no significant changes until device failure
  - Failures are a significant result, but they are not hinted at by precursor degradation
- Failure likely due to out-of-spec operation
- Device characterization somewhat limited
  - Made us reexamine the test approach
- Examination for mechanisms limited
  - Device expected degradation modes unknown
  - Intractable matrix for examining mechanisms
- **Limited ability to factor out test conditions**



Future Directions

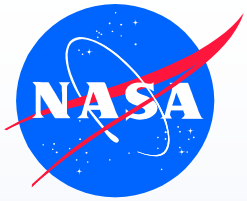
- Widen scope of target devices
  - Continue efforts to identify potential DDR2 devices
  - Migrate to DDR3 soon
- Increase test capabilities
  - Development of operating codes and protocols for equipment
    - Credence
    - Eureka
    - Functional tester
- Increase cross-NEPP support
  - New DIMM-based and loose-die based form factors will be more flexible to synergize with GSFC efforts

Conclusion - I

- Qualification approach seeks to provide useful data for NASA programs
  - NASA-Specific and Program-Specific acceptance testing
  - Develop understanding of device family to identify outliers
  - Perform limited life testing
- Reliability test matrix is too big
  - DDR devices are essentially complex ICs with many subcomponents
  - Building additional capabilities to support more testing
  - Test plans must be based on sampling and key measurements
- DUT options and interchangeability
  - Building fully interchangeable system for testing loose devices
  - Making test systems support DIMMs as well

Conclusion - II

- Test hardware development
  - Functional test system to support many DIMMs at once
  - Parametric testing of loose devices with Credence coming online
  - Incorporating industrial acceptance test hardware for DIMMs
- Test efforts
  - Last year's 78nm parts highlighted need for more characterization
  - Testing targeted static pattern at 125C/2.7V
  - Device failures are indicative of useful test, but difficult interpretation
- Future efforts will continue to improve testing capability
  - Perform characterization testing on recently acquired DIMMs
    - Parametrics, data pattern impact on cell retention, etc.



END

References

- Micron 2Gb DDR2 data sheet
- Mosis tech_cmos_rel FAQ “Reliability in CMOS IC Design: Physical Failure Mechanisms and their Modeling”
- Wikipedia DDR4 entry
- Jin Et. Al. “Prediction of Data Retention Time Distribution of DRAM by Physics-Based Statistical Simulation” – shows potential mechanism for our response is traps under the gate.

Additional Resources

- http://www.sciencedirect.com/science/article/pii/S0026271402000306
- http://trs-new.jpl.nasa.gov/dspace/handle/2014/20169
- http://ieeexplore.ieee.org/Xplore/login.jsp?url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel5%2F8520%2F26927%2F01197774.pdf%3Farnumber%3D1197774&authDecision=-203
- http://www.quickstartmicro.com/Sample%20Slides%20Quick%20Start%20IC%20Reliability.pdf