Radiation Qualification of Flash Memories

T.R. Oldham
Dell Services Federal Government

and K.A. LaBel
NASA Goddard Space Flight Center

To be presented by Timothy Oldham at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on nepp.nasa.gov.
Outline

• Introduction/Background
  – Flash Technology
  – Test Modes
  – Error Correction
  – Single Level Cell/Multi-Level Cell

• Total Ionizing Dose (TID)

• Heavy Ion SEE

• Proton Testing

• Combined Effects (Radiation/Reliability)

• Conclusions
Floating Gate Transistor

- Write (Program) operation—Fowler-Nordheim (FN) injection of electrons into FG
- Erase operation—FN injection of electrons from FG to substrate
- Repeated P/E operations cause damage to tunnel oxide
- High voltage charge pumps are critical to Program and Erase operations, usually the first thing to fail
Flash Architectures

NAND

NOR
Flash Advantages

• Low cost per bit
• Low Power
• Nonvolatile
• Attractive for space applications for the same reasons widely used in hand held, battery powered, consumer electronics
• Radiation response is variable, as one would expect for unhardened commercial technology, but often pretty good
Operating/Test Modes

- Typically have dozens of test modes, can only test a few
- Static mode, unbiased
- Static mode, biased
- Dynamic Read
- Dynamic Read/Write
- Dynamic Read/Erase/Write
- New! ONFI (Open NAND Flash Interface) enables high throughput (133 Mbytes/sec)
Error Correction

- Most NAND flash does NOT meet its performance or reliability specs without ECC
- Since ECC is critical to the system, it should be part of the test
- Most SLC NAND has about 3% redundant memory for ECC; e.g. 8G NAND has pages 4Kx8, or 32 Kbits, with an additional 128 bytes (1024 bits) for ECC
- Simple Hamming code for a memory segment of $2^N$ bits requires $N+1$ bits for SEC (single error correction), or $N+2$ bits for SEC-DED (SEC-double error detection)
- Redundant memory is sufficient to hold SEC or SEC-DED Hamming code to correct one bit of every 512 bits

To be presented by Timothy Oldham at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on nepp.nasa.gov.
SLC/MLC

- Single Level Cell NAND is typically specified as having $10^5$ P/E cycle endurance, and 10 year retention
- Multi-Level Cell NAND typically has 5000 P/E cycle endurance with 10 year retention
- MLC requires more robust error correction, because initial voltage margins are smaller
- New products being introduced by the industry are overwhelmingly MLC
TID Testing

- In accordance with MIL-STD-TM 1019.8, using Co-60 γ-source, nominal $V_{DD} + 10\%$, at room temperature
- DOD Test Guideline document recommends five parts, minimum—we prefer five in Read Only mode and five more fully exercised at each dose level
- TID response of unhardened commercial NAND flash memories varies widely among manufacturers and among technology nodes for a given manufacturer, but the best results are very good
- NAND flash sometimes survives TID exposure past 100 krad (SiO$_2$)—good enough for most NASA missions
- NOR flash is much more sensitive than NAND flash
Heavy Ion SEE Testing

- In accordance with ASTM F1192
- Try to get data with at least four ions (different LETs), and check for angular effects
- Use all test modes: Static, with and without bias; Dynamic Read; Dynamic R/W; Dynamic R/E/W
- Control logic errors (SEFIs) more important than single bit upsets
- Functional failures usually associated with high voltage Write and Erase operations, usually due to charge pump failures
## Control Logic Errors

<table>
<thead>
<tr>
<th>ERRCnt</th>
<th>DATA</th>
<th>EXP</th>
<th>BIE</th>
<th>BLOCK</th>
<th>PAGE</th>
<th>COL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>2509</td>
<td>13</td>
<td>907</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>2509</td>
<td>13</td>
<td>925</td>
</tr>
<tr>
<td>3</td>
<td>32</td>
<td>0</td>
<td>1</td>
<td>2538</td>
<td>37</td>
<td>1245</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>2540</td>
<td>58</td>
<td>1328</td>
</tr>
<tr>
<td>5</td>
<td>16</td>
<td>0</td>
<td>1</td>
<td>2541</td>
<td>8</td>
<td>779</td>
</tr>
<tr>
<td>6</td>
<td>32</td>
<td>0</td>
<td>1</td>
<td>2542</td>
<td>39</td>
<td>1208</td>
</tr>
<tr>
<td>7</td>
<td>128</td>
<td>0</td>
<td>1</td>
<td>2543</td>
<td>36</td>
<td>1234</td>
</tr>
<tr>
<td>8</td>
<td>128</td>
<td>0</td>
<td>1</td>
<td>2543</td>
<td>36</td>
<td>1252</td>
</tr>
<tr>
<td>9</td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>2577</td>
<td>47</td>
<td>952</td>
</tr>
<tr>
<td>10</td>
<td>16</td>
<td>0</td>
<td>1</td>
<td>2586</td>
<td>20</td>
<td>718</td>
</tr>
<tr>
<td>11</td>
<td>32</td>
<td>0</td>
<td>1</td>
<td>2587</td>
<td>57</td>
<td>1783</td>
</tr>
<tr>
<td>12</td>
<td>32</td>
<td>0</td>
<td>1</td>
<td>2587</td>
<td>57</td>
<td>1801</td>
</tr>
<tr>
<td>13</td>
<td>32</td>
<td>0</td>
<td>1</td>
<td>2602</td>
<td>0</td>
<td>1155</td>
</tr>
<tr>
<td>14</td>
<td>4</td>
<td>0</td>
<td>1</td>
<td>2658</td>
<td>24</td>
<td>1773</td>
</tr>
<tr>
<td>15</td>
<td>4</td>
<td>0</td>
<td>1</td>
<td>2674</td>
<td>26</td>
<td>1767</td>
</tr>
<tr>
<td>16</td>
<td>64</td>
<td>0</td>
<td>1</td>
<td>2697</td>
<td>45</td>
<td>318</td>
</tr>
<tr>
<td>17</td>
<td>16</td>
<td>0</td>
<td>1</td>
<td>2711</td>
<td>20</td>
<td>1386</td>
</tr>
<tr>
<td>18</td>
<td>16</td>
<td>0</td>
<td>1</td>
<td>2711</td>
<td>20</td>
<td>1404</td>
</tr>
<tr>
<td>19</td>
<td>32</td>
<td>0</td>
<td>1</td>
<td>2714</td>
<td>29</td>
<td>1226</td>
</tr>
<tr>
<td>20</td>
<td>32</td>
<td>0</td>
<td>1</td>
<td>2714</td>
<td>29</td>
<td>1244</td>
</tr>
<tr>
<td>21</td>
<td>8</td>
<td>0</td>
<td>1</td>
<td>2728</td>
<td>33</td>
<td>771</td>
</tr>
<tr>
<td>22</td>
<td>8</td>
<td>0</td>
<td>1</td>
<td>2728</td>
<td>33</td>
<td>789</td>
</tr>
</tbody>
</table>

- **Groups of two or more closely spaced errors, where each word has the same bit in error**—ECC would see these as uncorrectable errors
- **Transient noise in the Read circuit is causing erroneous Reads**—these addresses will be correct the next time they are Read

To be presented by Timothy Oldham at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on nepp.nasa.gov.
SEE Lessons Learned

- Want to keep exposure low enough to avoid collective (multiple ion) effects, but high enough for good statistics—trade offs to make effective use of beam time
- Important to estimate event rates in space: flux at LET>60 is less than one ion/cm² per 100 years, flux in an accelerator can be 15 orders of magnitude higher
- High current events are sometimes caused by multiple ion interactions—not necessarily SEE
- Flash memories have bit error rates many orders of magnitude better than standard volatile memories, because of nonvolatile feature
Acceptable SEFI rates and functional failure rates depend on the particular system.

Mitigation strategies are also unique to the system.

Frequently, the SEFI rate and failure rate in space is low enough that the program decides to accept the risk.
Proton Testing

• Guideline is to do proton test if threshold LET for SEE is $<15$ MeV/mg/cm$^2$, which is true for all unhardened commercial flash

• The one proton test done on unhardened commercial flash produced no single ion effects, only TID damage

• Need for proton testing is unclear
Radiation/Reliability Combined Effects

- Endurance and retention after radiation exposure has been tested, and retention failures have been observed.
- The number of retention errors is small enough that existing ECC can easily correct them, in SLC memories.
- MLC memories may be more sensitive.
- So far, no combined effects test is necessary for part qualification.

To be presented by Timothy Oldham at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on nepp.nasa.gov.
Conclusions

- Flash memory offers performance advantages over some other technologies
- Unhardened commercial technology has variable radiation response, and always requires testing
- Best results obtained in testing commercial flash are very good—it is possible to use them in space
- More and more, flight programs are seriously considering flash memory for some applications