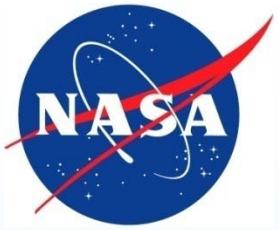
NEPP Electronic Technology Workshop
June 11-13, 2012

National Aeronautics
and Space Administration



Single Event Effects in Field Programmable Gate Array (FPGA) Devices: Update 2012

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To be presented by Melanie D. Berg at the NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on http://nepp.nasa.gov/.

NASA Goddard Radiation Effects and Analysis Group (REAG) FPGA Testing Supporters and Collaborators

- **Supporters:**
  - **Defense Threat Reduction Agency (DTRA)**
  - **NASA Electronics Parts and Packaging (NEPP)**
- **Collaborators:**
  - **Microsemi**
  - **Xilinx**
  - **Tower Jazz**
  - **BAE/Achronix**

Major Accomplishments (1) Single Event Upset (SEU) Testing

- **Microsemi**
  - **RTAX4000D:**
    - **Performed heavy ion SEU testing at Lawrence Berkeley National Laboratory (LBNL). March 2012. Data processing and analysis on going**
    - **Improvements in SEU cross sections (σ_{SEU}) versus RTAX2000s!**
  - **ProASIC3:**
    - **Performed heavy ion SEU testing at Texas A&M Cyclotron Facility (TAMU) August 2011 and December 2011.**
    - **Submitted December 2011: ProASIC3 SEU Test report. Report includes new developments regarding Flip-Flop (DFF) frequency effects.**

Major Accomplishments (1) – SEU Testing (Continued)

- **Xilinx**
  - **Submitted test plan: August 2011**
  - **Completed board design May 2012**
  - **Verified the V5/V5QV fault injector/scrubber was fully functional on new boards May 2012**
  - **Created 18 variations of shift register and counter device under test (DUT) test structures. Variations are based off of selected level of triple modular redundancy (TMR) and single event transient (SET) filters May 2012**
- **Tower/Jazz**
  - **Completed preliminary testing of Tower/Jazz ASICs at LBNL May 2012**

Major Accomplishments (1) – SEU Testing (Continued)

- **BAE/Achronix**
  - **Completed second phase of Heavy ion and Laser testing of the RadRunner FPGA. March 2012**
  - **Analysis is on-going**

Major Accomplishments (2) Mentor Triple Modular Redundancy (TMR) Tool

- **Assisted Mentor graphics with developing an automated TMR tool**
  - **Tool can support a variety of TMR schemes and a variety of FPGA device types**
  - **Tool is used in our radiation test campaigns**
- **Presented an invited talk at the Israel Solutions Expo, November 2011:" *Complexity Management and Design Optimization Regarding a Variety of Triple Modular Redundancy Schemes through Automation*"**

Major Accomplishments (3) – FPGA Model Development and Data Analysis

- Presented an invited talk at the Canadian Space Agency FPGA Workshop, "New Developments in Field Programmable Gate Array Single Event Upsets and Fail-Safe Strategies," October 2011.
- Included additional DFF frequency effects within the REAG FPGA SEU model. Opposing frequency effects have been observed and are now characterized: November 2011
- Presented a course at the International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA) November 2011. Included new DFF frequency effects discussion
- Presented a talk at the Hardened Electronics and Radiation Technology (HEART) Conference April 2012: "Single Event Upset Test and Analysis of Field Programmable Gate Array Devices for Critical Space Applications"
- Presented an invited talk at the Single Event Effects (SEE) Symposium April 2012:" Characterizing Data Path Single Event Upsets in a Synchronous Design"

Major Accomplishments (4)
Combined Radiation Environment Study

- **Commenced a new study on combined radiation environment effects using the Microsemi ProASIC3 as the DUT**
  - **Total ionizing dose (TID) Testing (Co-60) on the ProASIC3 Devices performed at NASA Goddard 03/2012**
  - **Heavy ion SEU Testing on the same TID ProASIC3 devices that were exposed to CO-60 performed at LBNL 03/2012**
  - **Additional Heavy ion SEU Testing on the same TID ProASIC3 devices that were exposed to CO-60 performed at LBNL 05/2012**
- **Data Analysis is on going… unexpected-interesting data… stay tuned**

Major Accomplishments (5)
FPGA Test Guideline Documentation

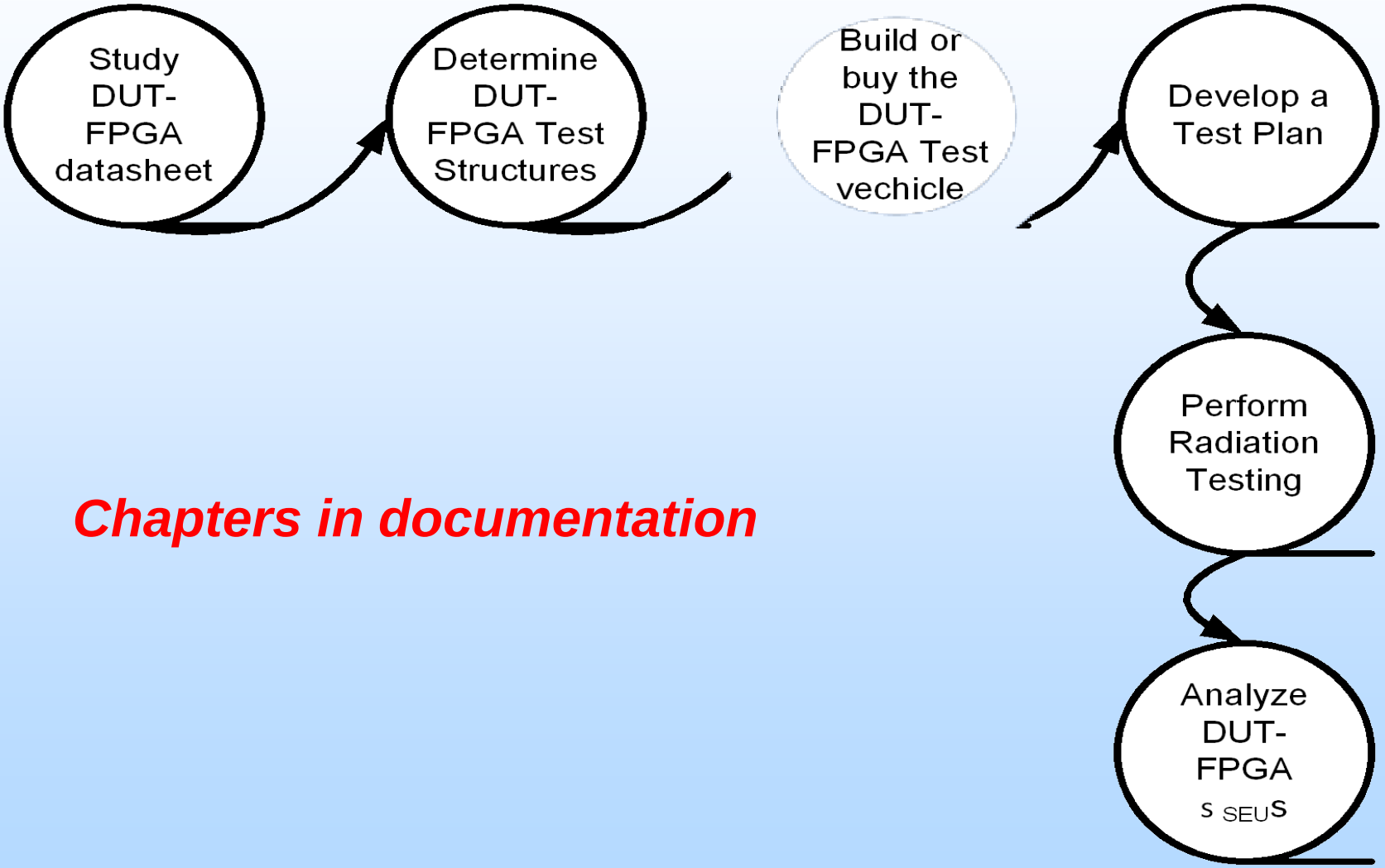
- **Title: Guidelines for Single Event Upset Test and Analysis for Field Programmable Gate Array Devices:**
  - **Submitted 02/01/2012: Preliminary FPGA Guidelines**
  - **Submitted 05/14/2012: Second version of FPGA Guidelines**
- **Guidelines are under review**

FPGA Test Guideline Documentation

Impact to Community

- **Currently it is difficult to compare test data because of differences in test vehicle and test methodology**
- **The SEU Test Guideline Documents will create standardized test methodologies and provide a means for data comparison across organizations**

Technical Highlights –
FPGA SEU Test Guidelines



Chapters in documentation

To be presented by Melanie D. Berg at the NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on http://nepp.nasa.gov/.

Build or Buy the DUT FPGA Test Vehicle

- Here's the question: Custom or off-the-shelf?
- The optimal answer is use the best of both.
- Before you get started understand:
  - The kind of DUT that you are testing
  - What type of tests you plan to perform
  - The limitations that your selected test vehicle

Test Vehicle Responsibilities and Considerations

- The SEU test vehicle is responsible for:
  - Applying DUT stimulus and
  - Monitoring DUT outputs with the following requirements:
    - Identification, differentiation, and isolation of various (and unexpected) error signatures
    - report upsets to the user
- Robust test vehicles require custom design; e.g., processor based test vehicles generally do not provide the resolution of control and visibility as compared to custom built testers

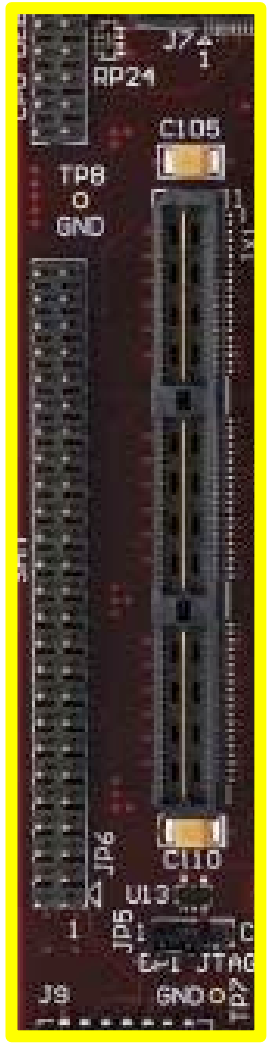
Input Stimulus and the Test Vehicle

- **Functional control:**
  - **Types of DUT functional input control: Clocks, resets, data inputs**
  - **Devices that can perform functional control: Functional generators, Computers, (semi)custom FPGA test boards**
  - **Concerns:**
    - **Managing frequencies of operation: high-speed control can be challenging.**
    - **Synchronizing inputs and managing skew between inputs.**
    - **Operating the device in a realistic manner**

Monitoring DUT during Irradiation

- **Types of error detection equipment: oscilloscopes, logic analyzers, computers or (semi)custom FPGA test boards**
- **Error Detection Logistics:**
  - **Capture data**
  - **Compare DUT outputs to expected values. How?:**
    - **Visually (not recommended as sole method); i.e., watching the error indication on the error detection equipment**
    - **Using equipment event triggers**
    - **Custom comparison circuitry**
  - **Differentiate upset types: e.g., clock tree SETs , DFF SEUs, combinatorial logic captured SETs, or configuration faults.**
  - **Count SEUs**

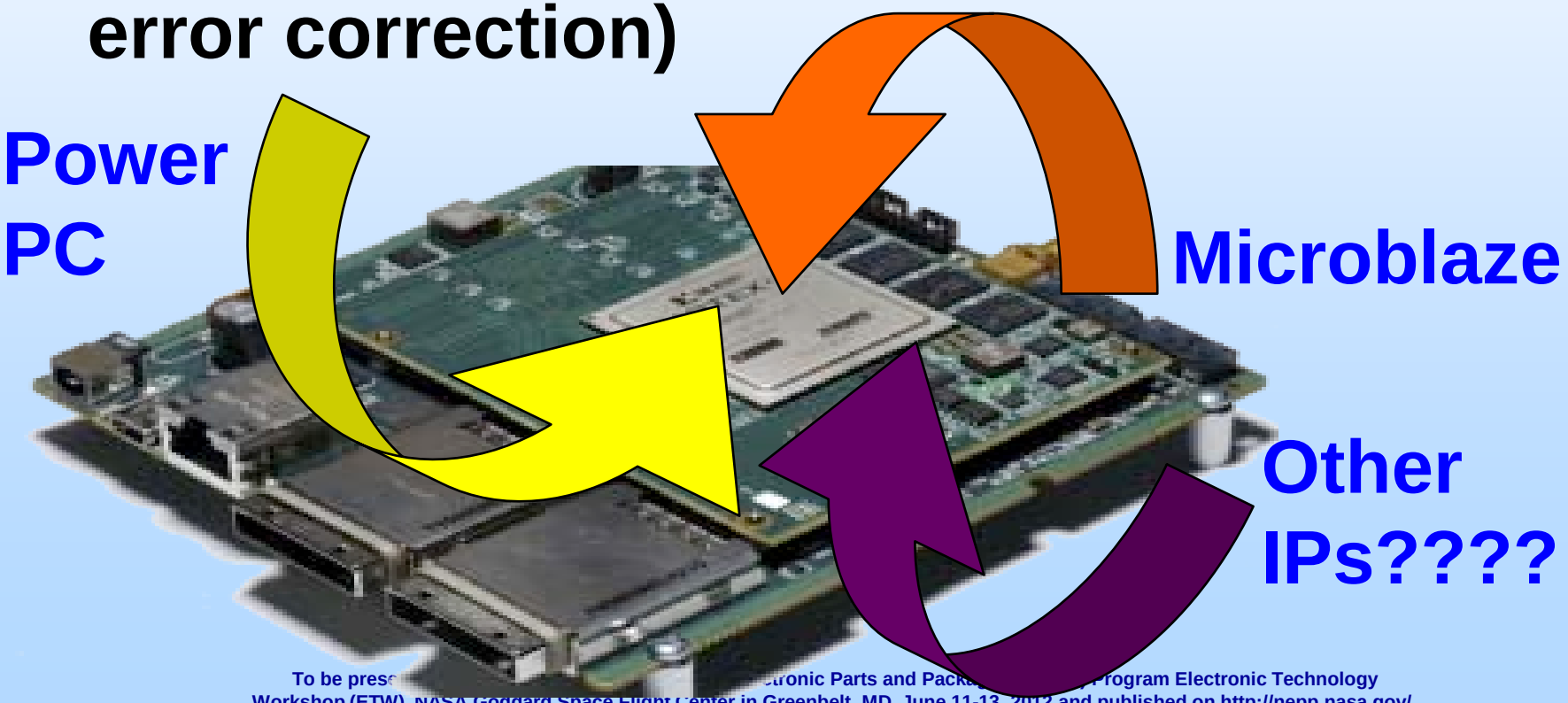
On-the-Shelf Test Vehicle Solutions: (1) Evaluation Boards



Limited available I/O Interfaces for DUT Control and Monitoring

On-the-Shelf Test Vehicle Solutions: (2) Intellectual Property (IP) Cores

- Some FPGAs contain a PowerPC or…
- Using the FPGA as a blank slate…You can map IP into the FPGA (e.g., Microblaze or error correction)



Problems with PowerPC or IP - Processor Based Test Vehicle Solutions

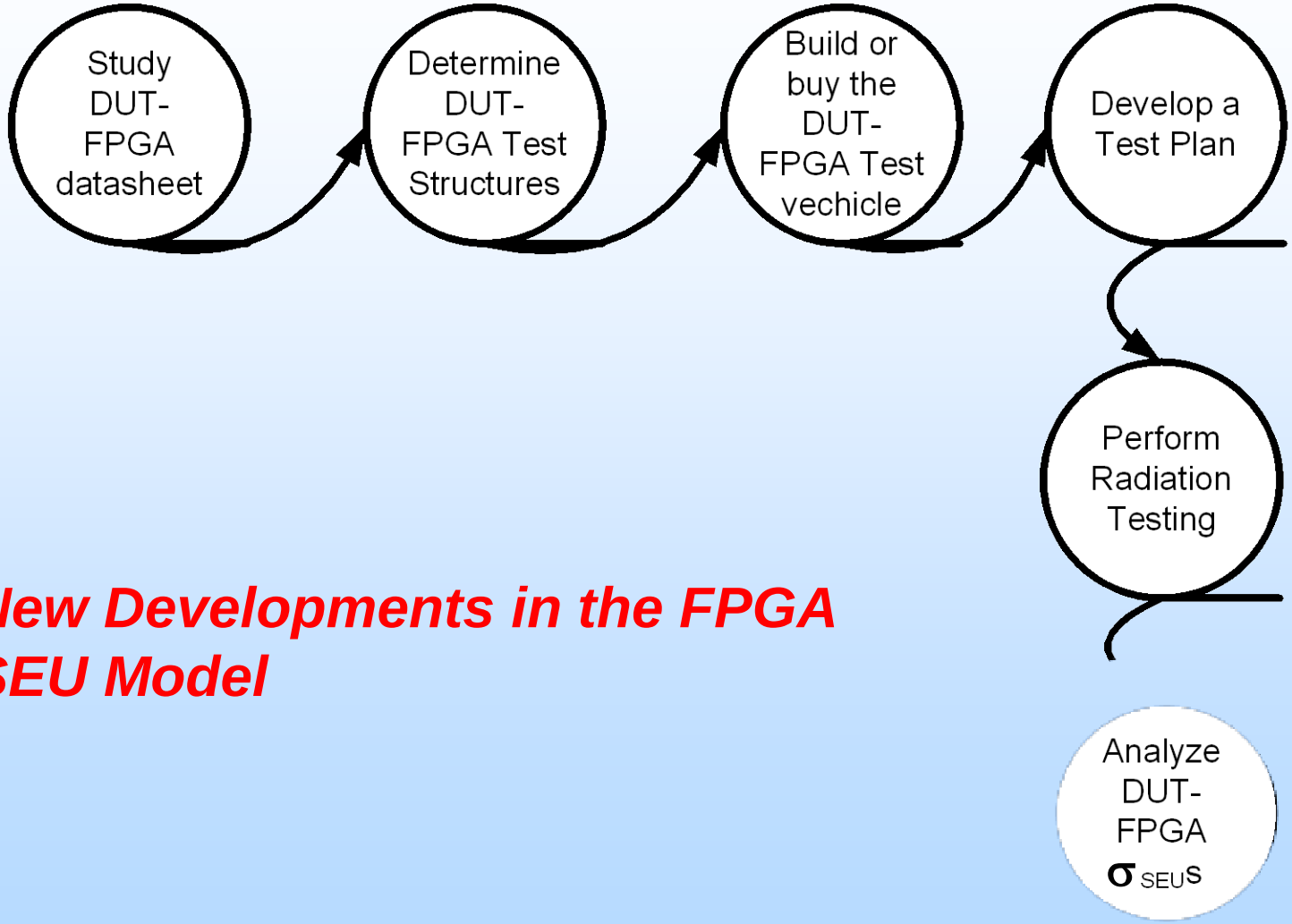
- Monitoring SEUs require:
  - Capturing data and
  - Reporting data with additional information
- Data capture resolution is key during SEU testing:
  - Unexpected error signatures
  - Speed of incoming DUT data to the test vehicle
- Synchronization of data capture from the DUT to the tester is challenging
- Problems with Processors:
  - Limited resolution and frequency control
  - Limitations on synchronization control

The REAG Solution

- **Use of the Low Cost Digital Tester (LCDT)**
  - **Two current versions of LCDT: Spartan-6 or Virtex-5 FPGA core**
  - **Custom made DUT control (input stimuli)**
    - **Proven to work up to 500MHz**
  - **Custom made DUT monitoring and data capture**
    - **Able to capture data in the GHz range (use of multiple clock edge sampling and re-synchronization techniques)**
    - **100's MHz range does not require multiple clock edge sampling**
    - **Has proven to provide more comprehensive data from SEU testing than processor based solutions**
- **In addition to the LCDT:**
  - **Logic analyzers as a backup monitor**
  - **Oscilloscopes for I/O SET monitoring**

Technical Highlights –

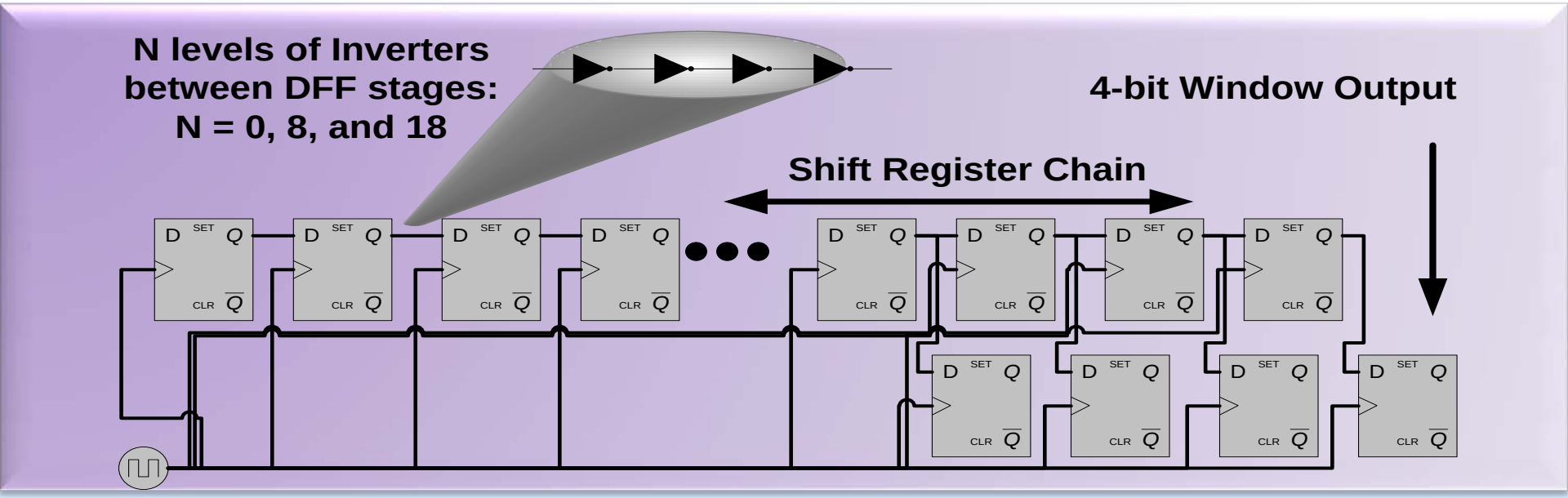
FPGA SEU Test Guidelines



New Developments in the FPGA SEU Model

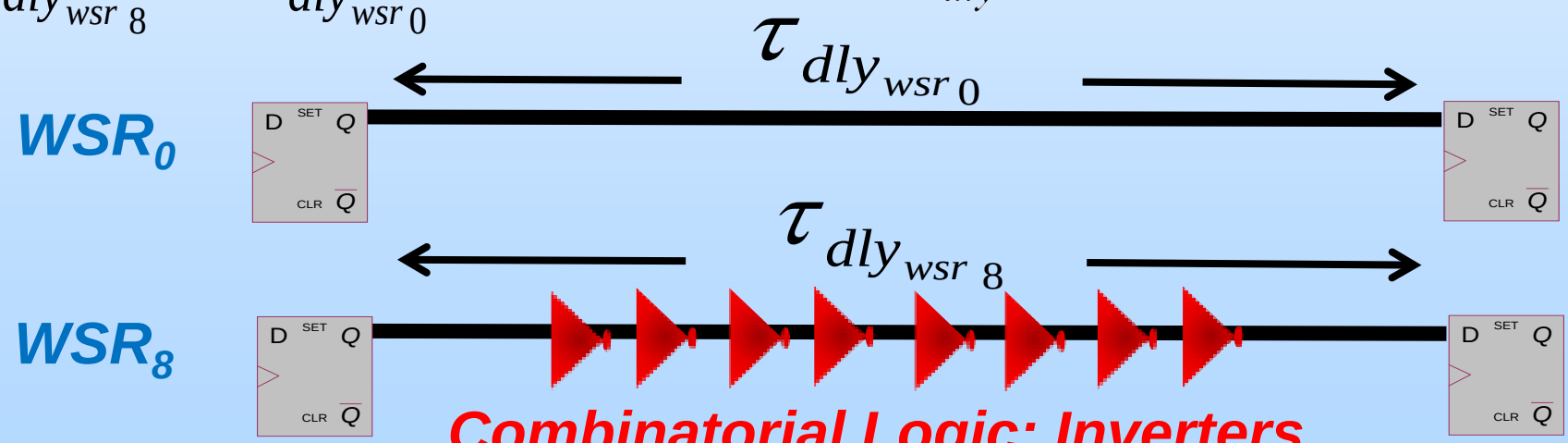
To be presented by Melanie D. Berg at the NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on http://nepp.nasa.gov/.

Radiation Test Structures: Windowed Shift Registers (WSRs)



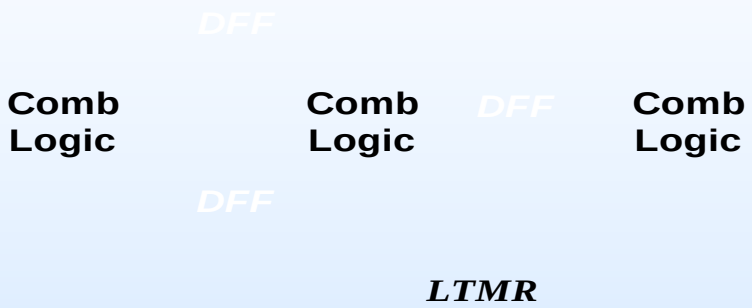
$\tau_{dly_{wsr\ 8}} > \tau_{dly_{wsr\ 0}}$

τ_{dly} = path delay from DFF to DFF



Combinatorial Logic: Inverters

Radiation Test Structures: Local Triple Modular Redundancy (LTMR)



Masks upsets from DFFs

Corrects DFF upsets if feedback is used

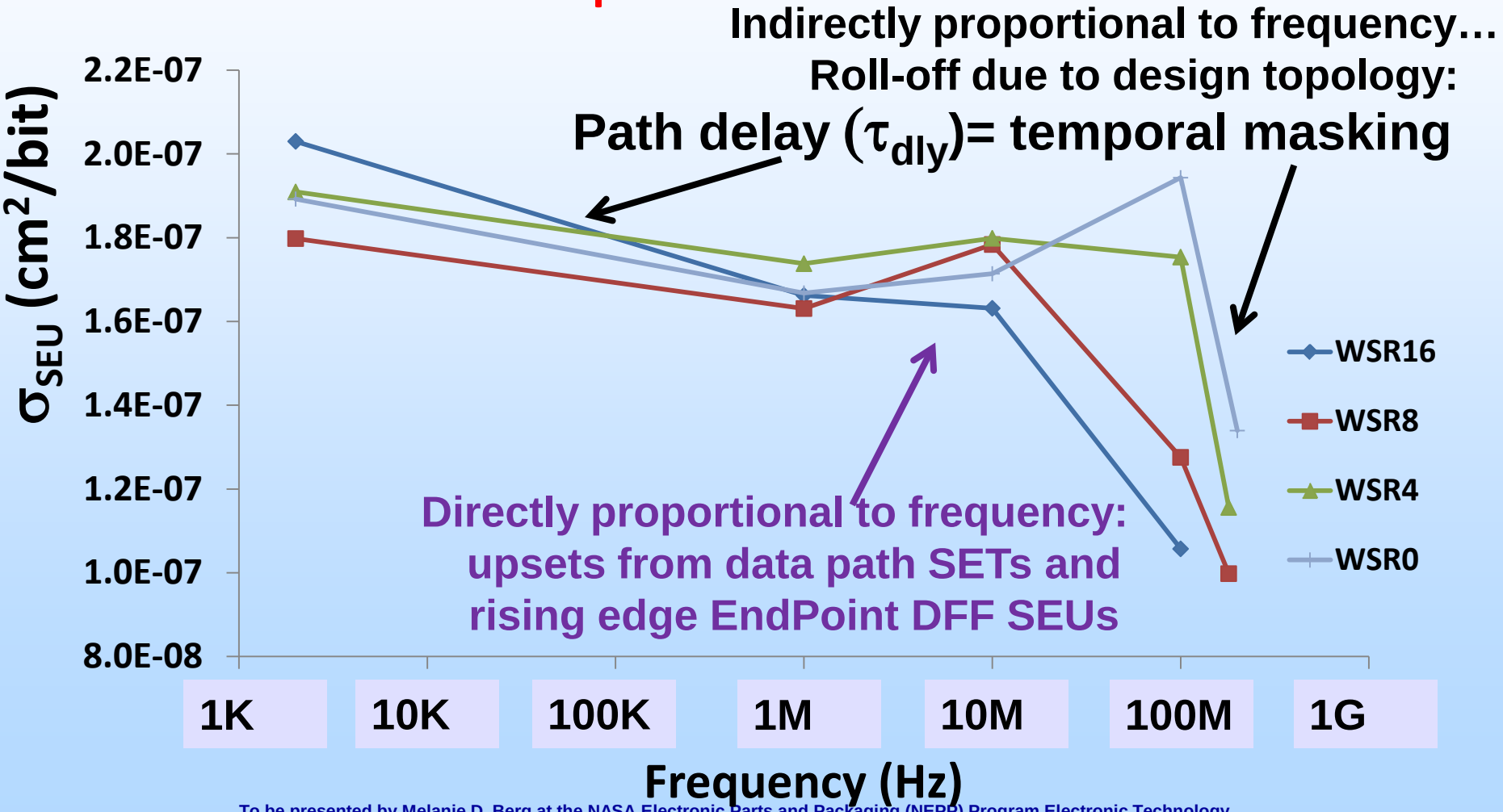
Only the DFFs are triplicated and mitigated

- **Following Examples are of ProASIC3 Heavy Ion Testing**
- **We tested WSRs with LTMR and without LTMR**

Technical Highlights

NASA Goddard REAG FPGA SEU Model and ProASIC3 Testing- DFF Frequency Effects

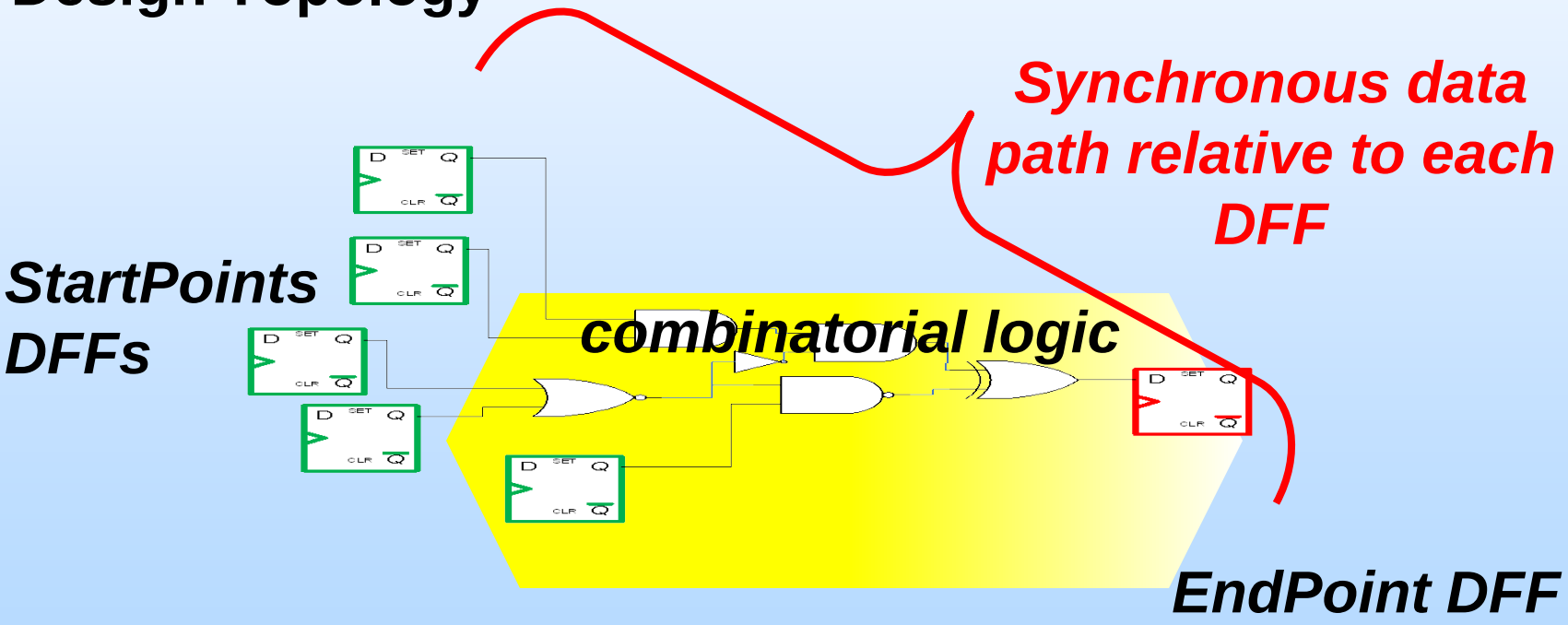
LET = 28.8 No TMR – checker pattern



Data Analysis Background

Probability of DFF upset is based on:

- Logic that feeds into the DFF input pin
- The internal susceptibility of the DFF
- Design Topology



StartPoints DFFs and combinatorial logic ➔ EndPoint DFF

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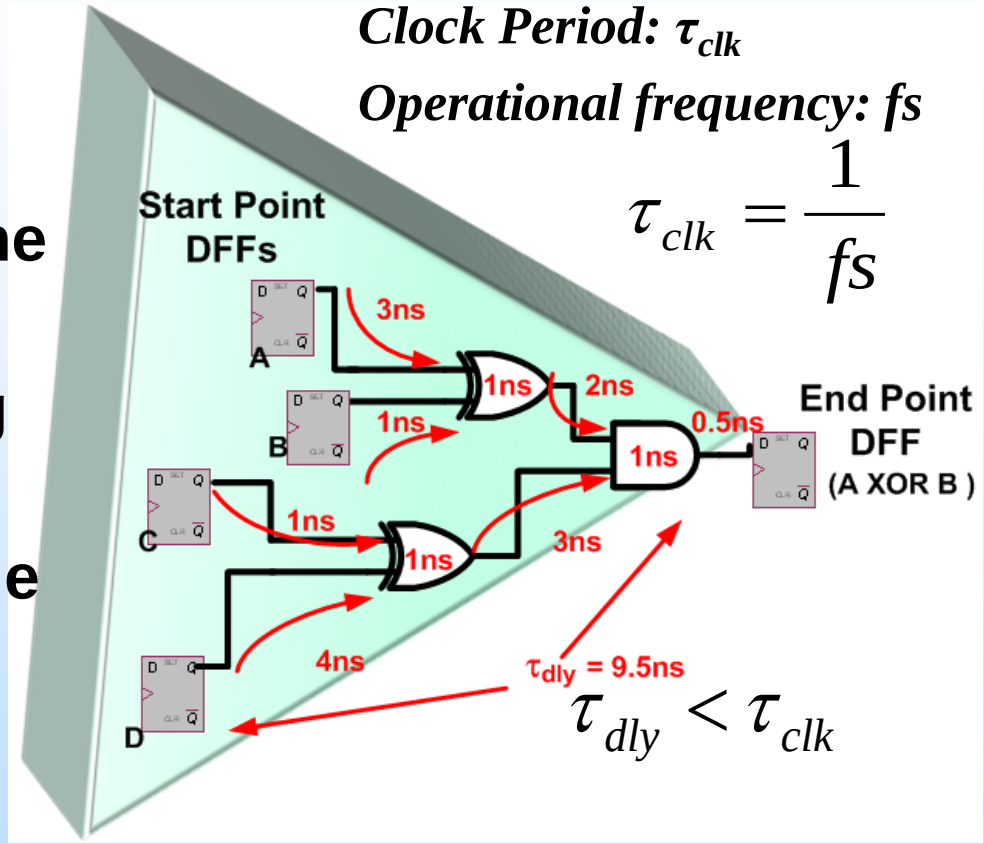
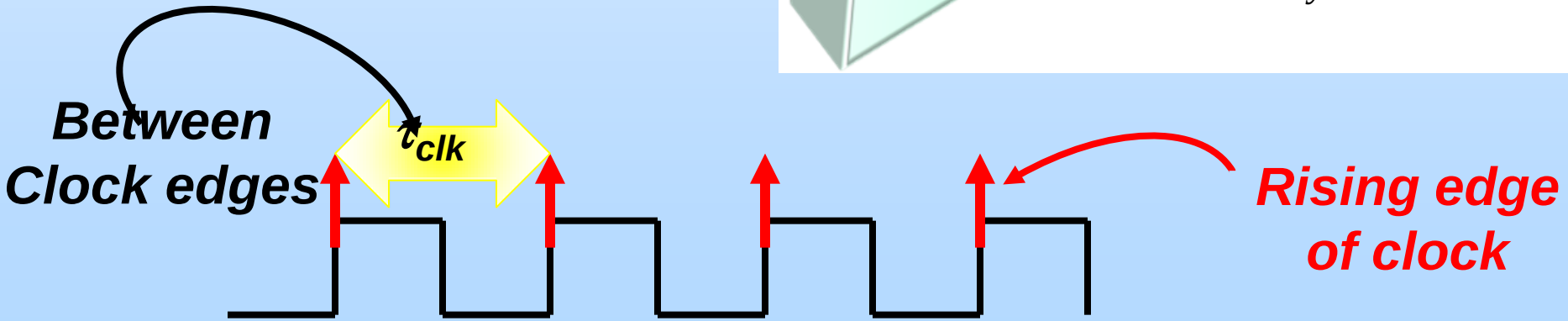
Terminology and Definitions for Synchronous Designs

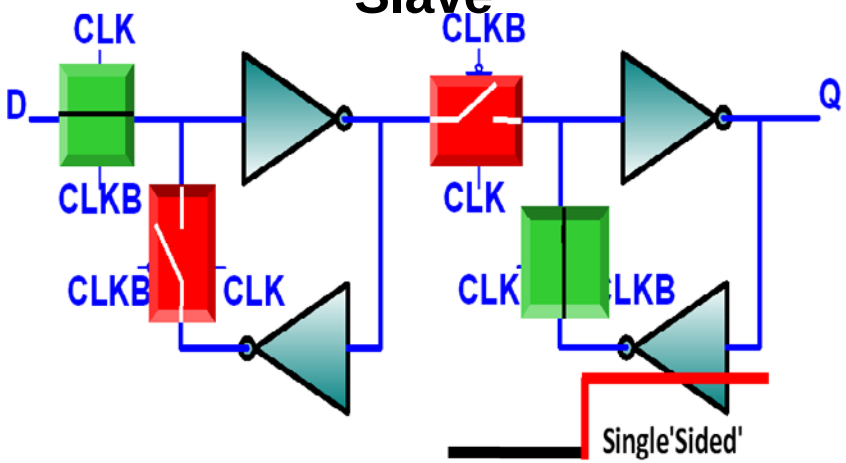
- **Combinatorial Logic (CL): Compute between clock edges**
- **DFFs: Hold (or sample) at the rising edge of a clock**
- **State is defined at the rising edge of clock**
- **Each StartPoint has a unique delay path (τ_{dly}) to reach an EndPoint**



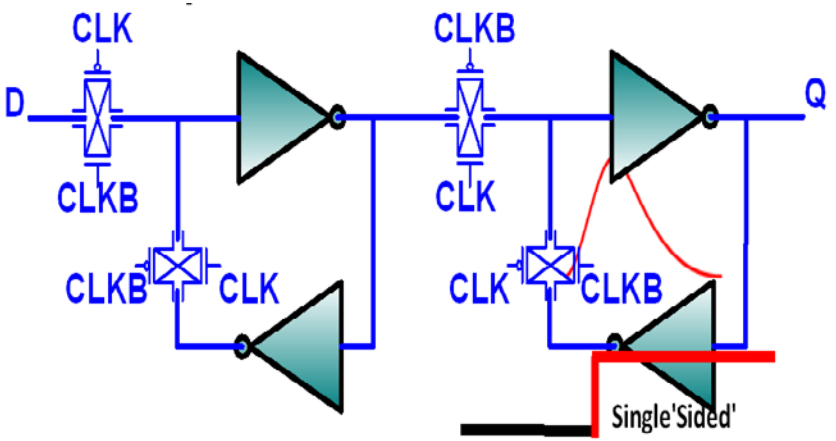


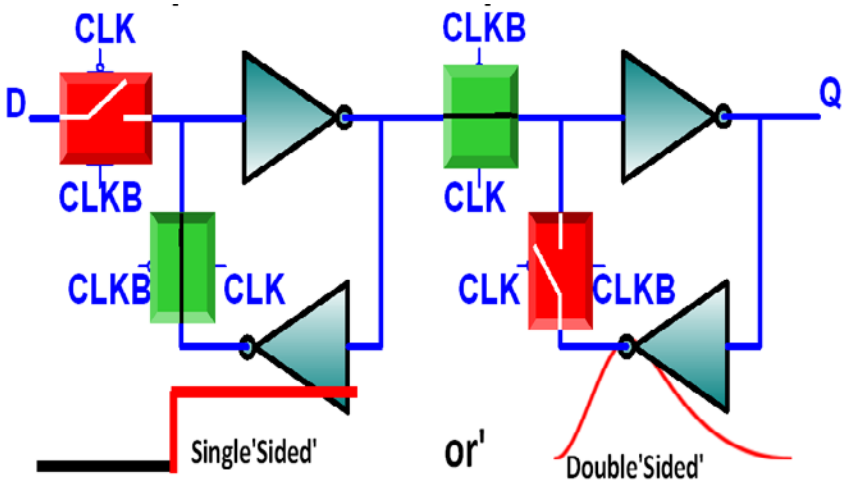
Clock State Controls SEU Signature

Clock Low: Single Sided Upset from Slave

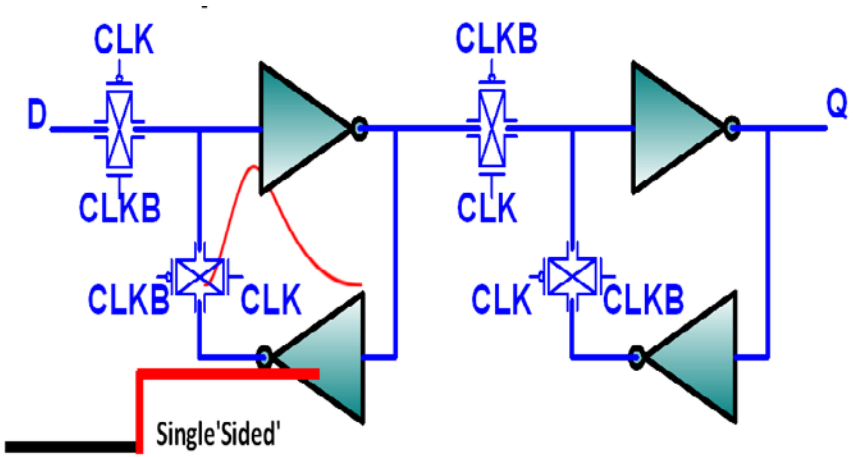


Clock High→Low: Slave Captures its SET





Clock High: Single Sided Upset from Master or SET from Slave



Clock Low→High: Master Captures its SET

Summary of DFF SEU Susceptibility

Clock state	Upset Type	System Effect
High	Master: Single sided Slave: SET	Between rising clock edges
Low	Slave: Single sided	Between rising clock edges
High➔ Low	Slave latches its own transient: Single sided	Between rising clock edges
Low➔ high	Master latches its own transient: Single Sided	At rising clock edge

- ***Between rising clock edges: must be captured by the next clock edge to cause a system upset(if not later masked)***
- ***At rising clock edge: system upset (if not later masked)***

Characterizing SEUs Generated Internally to a DFF

$$P(fs)_{DFFSEU} = \alpha P(fs)_{DFFSEU} + \beta P(fs)_{DFFSEU} + P(fs)_{DFFSET}$$

EndPoint:

Percentage of single sided upsets that occur at clock edge (low to high)

- **Frequency dependent: Master SET gets trapped during transition from transparent to hold state (rising edge of clock)**
- **SEUs are considered a state change**

StartPoint:

SETs generated in slave when clock is high

StartPoint:

Percentage of single sided upsets that occur between clock edges

- **Not Frequency dependent: Master or slave is in hold state**
- **Frequency dependent: Low➔High transition**
- **SEUs are not considered a definitive state change**

Putting it All Together: NASA REAG FPGA Data Path Susceptibility Model

$$P(fs)_{functional\ Logic}$$

$$\sum_{k=1}^{\#EndPoint\ DFFs} P_{logic(k)} * \left(\alpha P(fs)_{DFFSEU(k)} + \sum_{j=1}^{\#StartPoint\ DFFs} \left(\beta P(fs)_{DFFSEU(j)} (1 - \tau_{dly(j)} fs) * P_{logic(j)} \right) + \sum_{i=1}^{\#CL} \left(P_{gen_{(i)}} * P_{prop_{(i)}} * P_{logic_{(i)}} * \tau_{width_{(i)}} fs \right) \right)$$

EndPoint — Increase with frequency

StartPoints — Decrease with frequency

CL

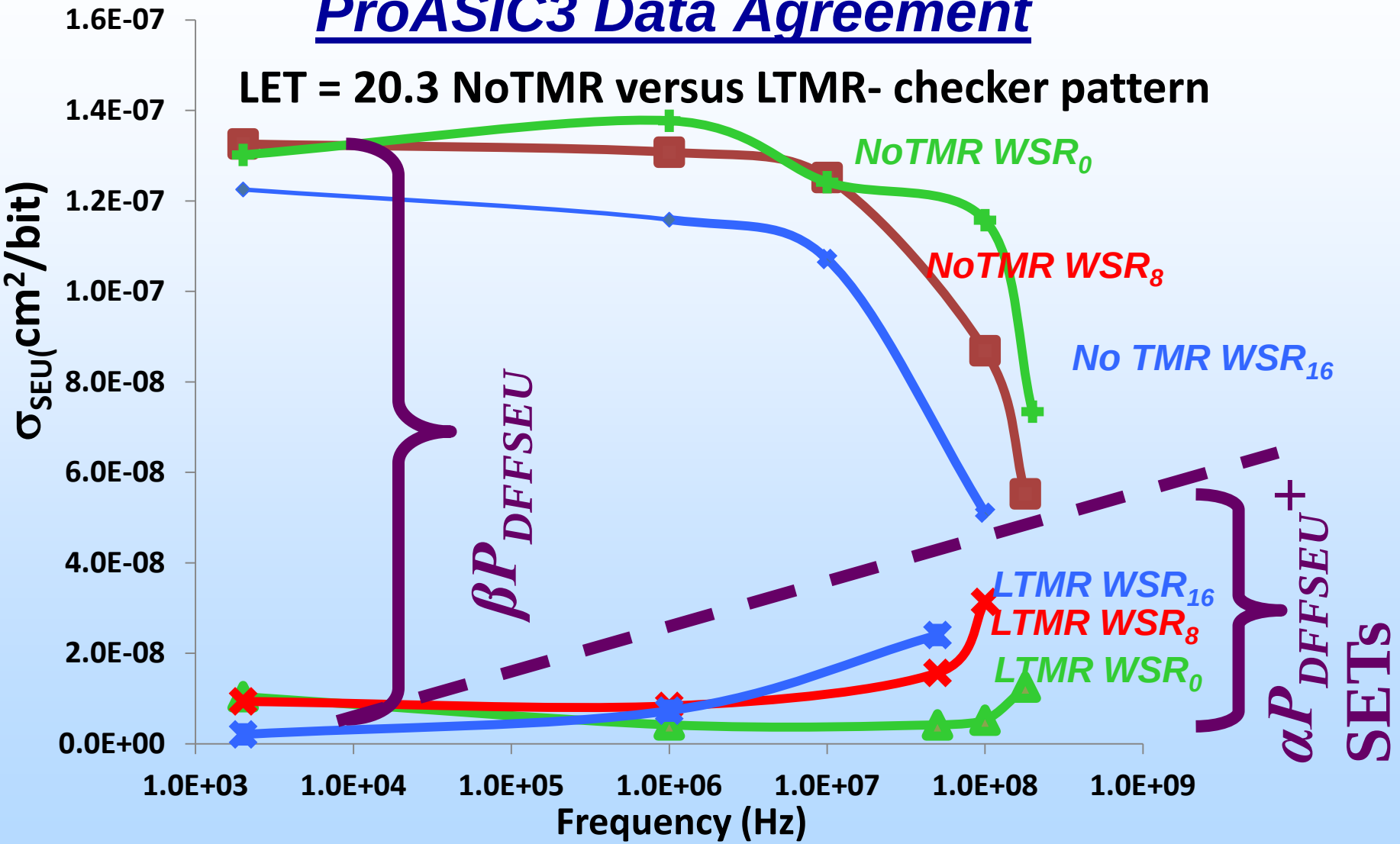
EndPoint Logic Masking

Note:

- $P_{logic(k)}$ ➔ *EndPoint Logic Masking*
- $P_{logic(j)}$ ➔ *StartPoint Logic Masking*
- $P_{logic(i)}$ ➔ *Combinatorial Logic Masking*
- $\tau_{dly(j)}$ ➔ *Delay from StartPoint to EndPoint*
- $P_{gen(i)}$ ➔ *CL SET generation*
- $P_{prop(i)}$ ➔ *CL propagation*
- $\tau_{width(i)}$ ➔ *SET width*

Technical Highlights

NASA Goddard REAG FPGA SEU Model and ProASIC3 Data Agreement

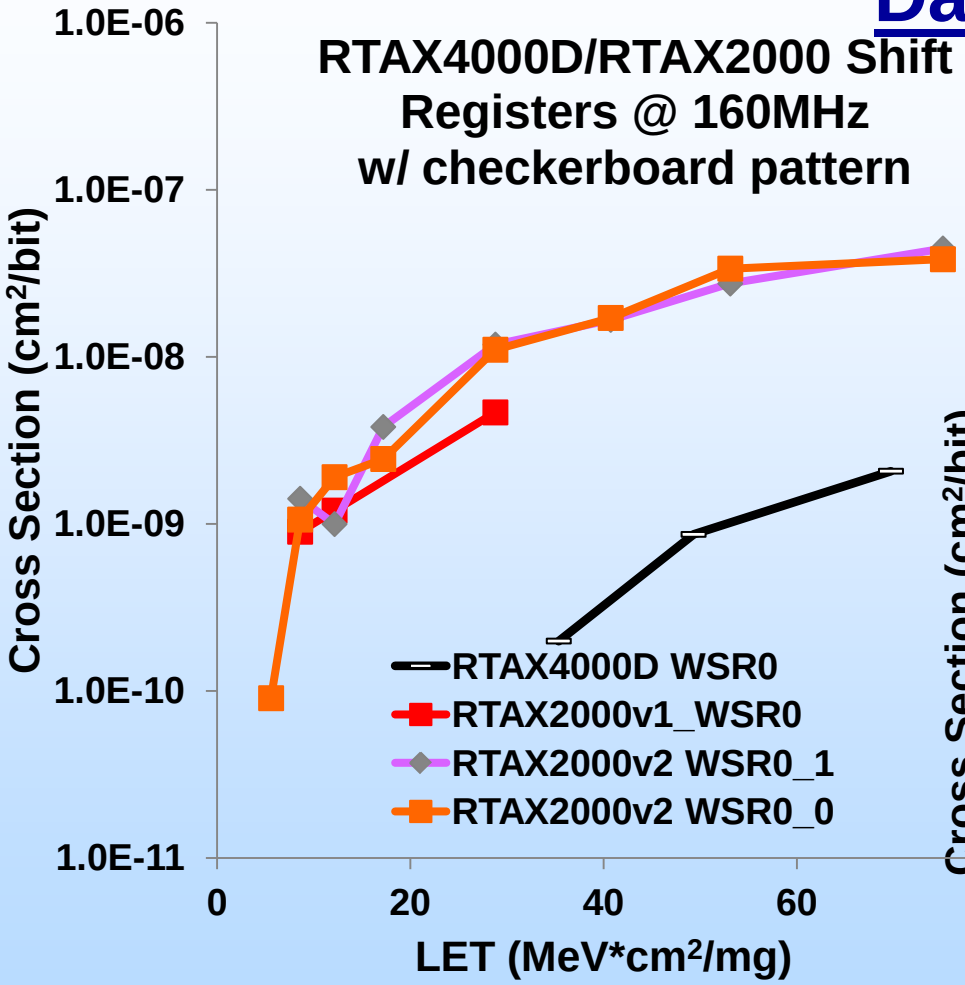


$$SEUs \approx \alpha P(fs)_{DFFSEU} + \beta P(fs)_{DFFSEU} + P(fs)_{DFFSET} \qquad SETs \approx P_{gen} P_{prop} \tau_{width} fs$$

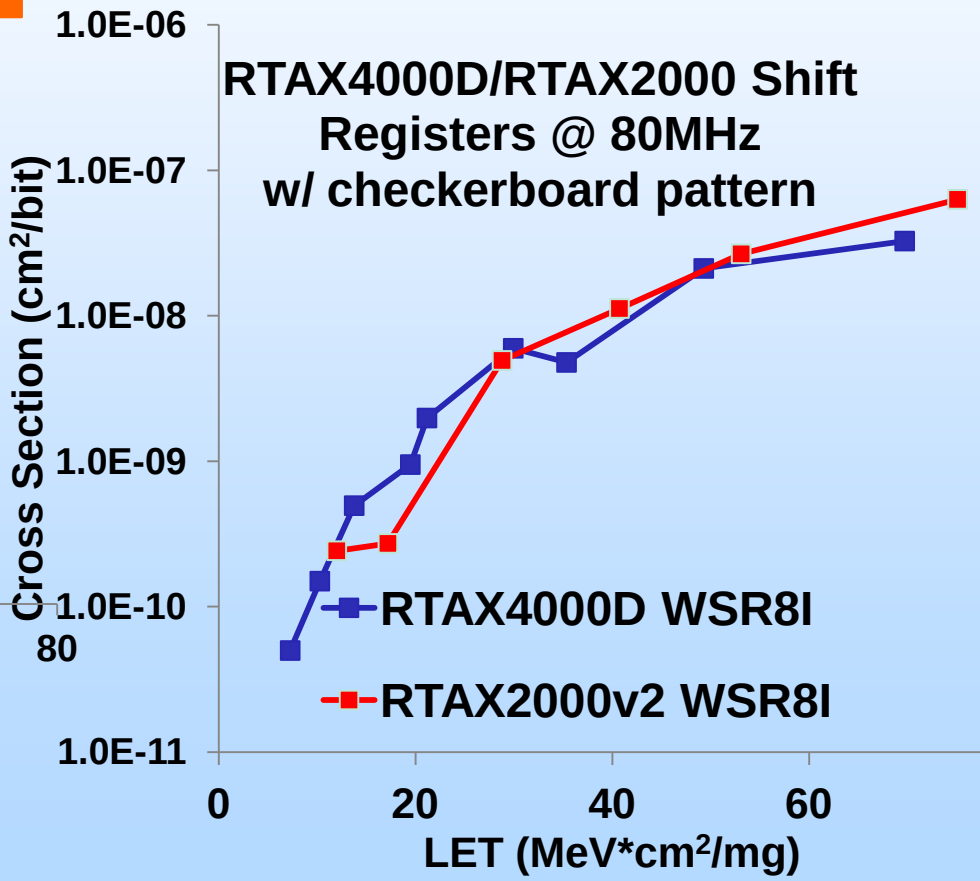
Microsemi RTAX4000D FPGA Data

Technical Highlights

RTAX4000D versus RTAX2000s WSR SEU Data



Didn't make a significant difference when adding CL in data path

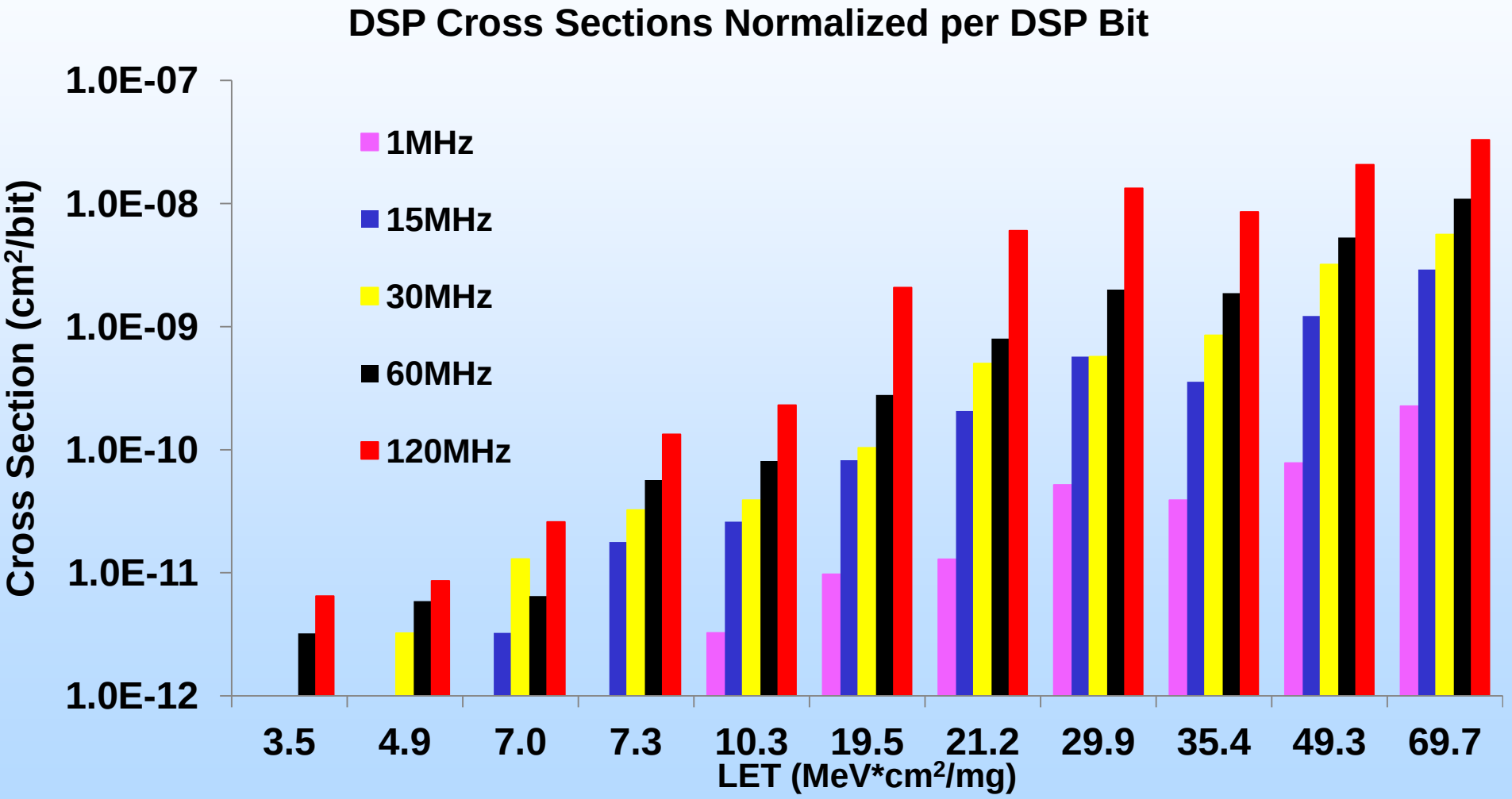


4000D has additional mitigation on DFF buffers

Technical Highlights

RTAX4000D DSP Cross Sections

Significant amount of performance per error event



Plans FY12 (1)

- Further development and application of the REAG FPGA Single Event Upset (SEU) model to a variety of FPGA types… on going
- Microsemi
  - Complete RTAX4000D SEU data analysis and test report: 06/2012
  - Complete ProASIC3 TID data analysis and test report: 07/2012
  - Complete Phase I ProASIC3 combined radiation environment effects data analysis and test report: 07/2012
- Xilinx
  - Heavy ion test and analysis of the Virtex 5QV (SIRF) FPGA 06/2012
  - Use of Mentor Graphics TMR synthesis Tool
- Tower Jazz
  - Heavy ion test of custom test structures in their 180nm SiGe/CMOS process 05/2012
  - Test report due data contingent on data analysis and potential additional testing

Plans FY12 (2)

- **BAE/Achronix**
  - **Complete data analysis and test report: 06/2012**
- **RADECS 2012 paper submission "Characterizing Single Event Upsets in a Synchronous Data Path", M. Berg, M. Friendlich, H. Kim, J. Pellish and K. LaBel**

  We present an SEU model and supporting data demonstrating frequency effects that deviate from conventional theory. In addition, the model emphasizes design topology versus circuit-element contributions to SEU cross-sections.

- **FPGA guidelines documentation editing**
- **TMR Tool Evaluation:**
  - **Work with Mentor Graphics to enhance their TMR insertion tool**
  - **Potentially analyze Synopsis' TMR insertion tool**