HiREV NEPP Technical Interchange: “CMOS Physics of Failure Lifetime Modeling”

Jon Osborn, Chris Paul, Jim Dixon, John Scarpulla, Ron Lacoe, Dave Eccles
The Aerospace Corporation
June 13, 2012
Presented to NASA NEPP
Meeting at NASA GSFC
Topics of Discussion

• Multi-Level PoF Modeling & Simulation
• HiREV nano-CMOS Road-Map
• FY12 Lifetime Focus Areas
• CMOS Failure Modes Under Investigation
• Analog Mixed Signal Lifetime Simulation
• 90nm CMOS ASIC Full-Chip Lifetime Model
• Looking Forward
Multi-Level PoF Lifetime Modeling

1M+ Transistors

1K-100K Transistors

1-1000s Transistors

1-100s Transistors

1000s of Atoms

Circuit Complexity

Atomistic Sims

Device-Level Simulation

Analog Mixed Signal Circuit-Level Simulations

Digital IP Block Circuit-Level Simulation (AgeMOS, MOSRA, RelExpert, New Models Needed)

Full-Chip ASIC Lifetime Modeling (New Models Needed)

(AgeMOS, MOSRA, RelExpert)

(TCAD, Multi-Physics PDE FEM)

(MD, DFT, New Models Needed)
## HiREV FY12 nanoCMOS Roadmap

<table>
<thead>
<tr>
<th>FY10</th>
<th>FY11</th>
<th>FY12</th>
<th>FY13</th>
<th>FY14</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm</td>
<td>Test Chip Def and Design</td>
<td>Test Chip Fab</td>
<td>Evaluation</td>
<td></td>
</tr>
<tr>
<td>45nm</td>
<td>Rel Test Chip Def and Design</td>
<td>Test Chip Fab</td>
<td>Evaluation</td>
<td></td>
</tr>
<tr>
<td>32nm</td>
<td>Rel Test Chip Def and Design</td>
<td>Test Chip Fab</td>
<td>Evaluation</td>
<td></td>
</tr>
<tr>
<td>130nm AMS IRIS Eval.</td>
<td>90nm Digital IRIS Eval.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22nm</td>
<td>Rel Chip</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

HiREV Support (Coordination, IP Control, Management, …)
FY12 HiREV/Aerospace Focus Areas

- Circuit-level BoL/EoL Modeling & Simulation
- Foundry Technology Qualification Data and Models
- Device-level BoL/EoL PCM/RO Characterization
- Product-level Highly Accelerated Stress Testing
- Micro/nano Chemical and Physical DPA/NDE BoL/EoL

Credible Lifetime Assessment
CMOS Failure Modes Under Investigation

- **Front-End-of-Line (FEOL)**
  - Hot Carrier Injection (HCl)
  - Negative Bias Temperature Instability (NBTI)
  - Stress Induced Leakage Current (SILC)
  - Gate Oxide Time Dependent Dielectric Breakdown (GO-TDDB)

- **Radiation Degradation**
  - Total Ionizing Dose (TID)
  - Rad/Rel Synergistic Effects

- **Back-End-of-Line (BEOL)**
  - Electromigration (EM)
  - Stress Voiding (SV)
  - Contact & Via Opens
  - Inter-level Dielectric TDDB (ILD-TDDB)

- **Advanced Packaging**
  - Ceramic Strength
  - Interconnect Metallurgy
  - Adhesive Polymers
**Atomistic simulation of HCI degradation in CMOS**

**FY12 Mid-Year Accomplishment**

**Goal:** Apply atomistic simulation techniques to understand the generation and action of interface and boundary defects resulting from hot carrier injection (HCI) within the channel of CMOS transistors

**Methodology:**
- Molecular dynamics (MD) of initial interface structure
- Density functional theory (DFT) electronic structure calculations for latent defects (e.g. strained bonds, Si-H, etc...)
- Quantum analysis of latent defect hot carrier capture cross section
- DFT-MD simulations of atomic relaxations following carrier capture
- MD simulations of large scale oxide relaxation
- Analysis of defect trapping/charging for end-to-end degradation predictions

**Current Status:**
- CMOS, 2 nm thick gate oxide, polySi gate
- Amorphous gate oxide generated using MD
- Plane wave DFT calculations of defects

**Need MD/DFT Model for Each Failure Mode**
FY11 HiREV Vanderbilt University Collaboration, nano-scale 3D Imaging → TCAD → SEE Response

3D TCAD Model Created for MRED

Simulate Single Event Energy Deposition for Al vs. W

Increase Error Rate for High Qcrit Logic
“Bottoms-Up” MOSFET Device, Analog Mixed Signal and Digital Circuit Aging Process

Analog Mixed Signal:
- Obtain BoL MOSFET BSIM
- Develop EoL “Aged” MOSFET BSIM
- Validate BoL/EoL BSIM w/ PCM Data
- Use SPICE to Identify Stressed Dev. In Ckt.
- Replace w/ Uniquely “Aged” Devices
- Simulate Corners at Chronological Times
- Once Circuit Out of Spec. => Lifetime

Large Digital IP Block:
- Obtain BoL Digital Lib. (e.g. Synopsis)
- Develop EoL “Aged” Digital Timing Library
- Validate BoL/EoL Timing w/ Test Data
- Integrate Switching to Determine “Age”
- Replace w/ Uniquely “Aged” Timing Models
- Simulate Corners at Chronological Times
- Timing Margin=0ns => Lifetime

Small Digital IP Block:
- Extract Worst-Case Timing Path
- Replace w/ Uniquely “Aged” MOS Devices
- Simulate Corners at Chronological Times
- Timing Margin=0ns => Lifetime

BSIM: Berkeley SPICE IGFET Model

DISTRIBUTION A. Approved for public release; distribution unlimited.
130nm Device Aging Simulation Methodology

- Develop a device aging calculation for each reliability wear out mechanism based on the physical understanding of the mechanism, data and models available from foundry, literature, and our experimental data
- Review the operating conditions of each transistor in the circuit to identify those that are expected to suffer degradation due to NBTI, HCI, and TDDB
- Project changes in the BSIM (Berkeley Short-channel IGFET Model) models used for these selected transistors at 10, 20 and 40 years to simulate the effects of aging on the circuit
- Compare Beginning of Life (BoL) Simulations with “aged” End Life (EoL) models to simulate degraded circuit performance that illustrates the aging effect
Ex: Analog Mixed Signal Circuit
VCO / Divider Aging

• Inputs
  – \( V_{dd} = 1.5V \)
  – 3 Bit Programmable VCO Frequency tuning (8GHz)
  – Analog input for Fine Tuning
  – Control Bit Selects Divide by 2 or 3
  – VCO Current Reference
  – Divider Current Reference

• Output
  – VCO Differential Output
  – Divider Differential Output
Characterization of 130 nm 8rf Models
Measurement v. Simulation for BoL NMOS and PMOS

- In this example the $V_{th}$ is 0.432 V, $G_{max}$ is 10.4 mS
- BSIM 3f5 Level 8 Foundry BoL Model
### Ex: Operating Point of 130-nm MOSFETs in Circuit

<table>
<thead>
<tr>
<th>FET Number</th>
<th>Circuit Type</th>
<th>W (µm)</th>
<th>L (µm)</th>
<th>nf</th>
<th>m</th>
<th>vs (V)</th>
<th>Vg (V)</th>
<th>Vd (V)</th>
<th>Id (mA)</th>
<th>Freq (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCO_10GHz Ibias</td>
<td>20</td>
<td>0.25</td>
<td>5</td>
<td>1</td>
<td>1.5</td>
<td>0.89</td>
<td>0.35</td>
<td>0</td>
<td>0.09374</td>
</tr>
<tr>
<td>2</td>
<td>VCO_10GHz Ibias</td>
<td>500</td>
<td>0.25</td>
<td>125</td>
<td>1</td>
<td>1.5</td>
<td>0.888</td>
<td>0.7174</td>
<td>8.695</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>VCO_10GHz Ibias</td>
<td>38.5</td>
<td>0.25</td>
<td>10</td>
<td>1</td>
<td>1.5</td>
<td>0.89</td>
<td>0.522</td>
<td>0.7185</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>VCO_10GHz Ibias</td>
<td>120</td>
<td>0.12</td>
<td>10</td>
<td>1</td>
<td>1.5</td>
<td>1.005</td>
<td>1.005</td>
<td>0.7986</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>VCO_10GHz Ibias</td>
<td>120</td>
<td>0.12</td>
<td>10</td>
<td>1</td>
<td>1.5</td>
<td>1.005</td>
<td>1.005</td>
<td>0.7986</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>VCO_10GHz Ibias</td>
<td>16</td>
<td>0.4</td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0.5521</td>
<td>0.522</td>
<td>0.2341</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>VCO_10GHz Ibias</td>
<td>16</td>
<td>0.4</td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0.5521</td>
<td>1.005</td>
<td>0.7986</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>VCO_10GHz Ibias</td>
<td>860</td>
<td>0.4</td>
<td>215</td>
<td>1</td>
<td>0</td>
<td>0.5521</td>
<td>0.09374</td>
<td>21.41</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>VCO_10GHz Ibias</td>
<td>16</td>
<td>0.4</td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0.5521</td>
<td>1.005</td>
<td>0.7986</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>VCO_10GHz Ibias</td>
<td>540</td>
<td>0.4</td>
<td>135</td>
<td>1</td>
<td>0</td>
<td>0.5521</td>
<td>0.117</td>
<td>15.86</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>VCO_10GHz ControlBits</td>
<td>2</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>12</td>
<td>VCO_10GHz ControlBits</td>
<td>2</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>13</td>
<td>VCO_10GHz ControlBits</td>
<td>2</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>14</td>
<td>VCO_10GHz ControlBits</td>
<td>2</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>15</td>
<td>VCO_10GHz ControlBits</td>
<td>2</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>16</td>
<td>VCO_10GHz ControlBits</td>
<td>2</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>17</td>
<td>VCO_10GHz ControlBits</td>
<td>2</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>18</td>
<td>VCO_10GHz ControlBits</td>
<td>1</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>19</td>
<td>VCO_10GHz ControlBits</td>
<td>1</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>20</td>
<td>VCO_10GHz ControlBits</td>
<td>1</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>21</td>
<td>VCO_10GHz ControlBits</td>
<td>1</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>22</td>
<td>VCO_10GHz ControlBits</td>
<td>1</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>23</td>
<td>VCO_10GHz ControlBits</td>
<td>1</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>24</td>
<td>VCO_10GHz ControlBits</td>
<td>1</td>
<td>0.12</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>25</td>
<td>VCO_Core</td>
<td>24</td>
<td>0.12</td>
<td>6</td>
<td>1</td>
<td>0</td>
<td>0.77</td>
<td>0.77</td>
<td>4.347</td>
<td>0</td>
</tr>
<tr>
<td>26</td>
<td>VCO_Core</td>
<td>24</td>
<td>0.12</td>
<td>6</td>
<td>1</td>
<td>0</td>
<td>0.77</td>
<td>0.77</td>
<td>4.347</td>
<td>0</td>
</tr>
<tr>
<td>27</td>
<td>VCO_MIM_Bank</td>
<td>8</td>
<td>0.12</td>
<td>2</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>28</td>
<td>VCO_MIM_Bank</td>
<td>8</td>
<td>0.12</td>
<td>2</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>29</td>
<td>VCO_MIM_Bank</td>
<td>8</td>
<td>0.12</td>
<td>2</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>30</td>
<td>VCO_MIM_Bank</td>
<td>8</td>
<td>0.12</td>
<td>2</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>31</td>
<td>VCO_MIM_Bank</td>
<td>8</td>
<td>0.12</td>
<td>2</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>32</td>
<td>VCO_MIM_Bank</td>
<td>8</td>
<td>0.12</td>
<td>2</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>33</td>
<td>VCO_MIM_Bank</td>
<td>8</td>
<td>0.12</td>
<td>2</td>
<td>1</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>34</td>
<td>VCO_Prefbuf</td>
<td>32</td>
<td>0.12</td>
<td>32</td>
<td>1</td>
<td>0.1177</td>
<td>1.005</td>
<td>0.996</td>
<td>7.928</td>
<td>0</td>
</tr>
<tr>
<td>35</td>
<td>VCO_Buf</td>
<td>40</td>
<td>0.12</td>
<td>32</td>
<td>1</td>
<td>0</td>
<td>0.09374</td>
<td>1.005</td>
<td>0.9438</td>
<td>10.71</td>
</tr>
<tr>
<td>36</td>
<td>DIV_Bias</td>
<td>40</td>
<td>0.25</td>
<td>10</td>
<td>1</td>
<td>0</td>
<td>0.3396</td>
<td>0.3396</td>
<td>0.2</td>
<td>0</td>
</tr>
<tr>
<td>37</td>
<td>DIV_Bias</td>
<td>200</td>
<td>0.25</td>
<td>50</td>
<td>1</td>
<td>0</td>
<td>0.3396</td>
<td>0.473</td>
<td>1.128</td>
<td>0</td>
</tr>
<tr>
<td>38</td>
<td>DIV_Bias</td>
<td>400</td>
<td>0.25</td>
<td>100</td>
<td>1</td>
<td>0</td>
<td>0.3396</td>
<td>0.2095</td>
<td>1.905</td>
<td>0</td>
</tr>
<tr>
<td>39</td>
<td>DIV_Bias</td>
<td>400</td>
<td>0.25</td>
<td>100</td>
<td>1</td>
<td>0</td>
<td>0.3396</td>
<td>0.2027</td>
<td>1.894</td>
<td>0</td>
</tr>
<tr>
<td>40</td>
<td>DIV_Bias</td>
<td>400</td>
<td>0.25</td>
<td>100</td>
<td>1</td>
<td>0</td>
<td>0.3396</td>
<td>0.1973</td>
<td>1.885</td>
<td>0</td>
</tr>
<tr>
<td>41</td>
<td>DIV_Bias</td>
<td>400</td>
<td>0.25</td>
<td>100</td>
<td>1</td>
<td>0</td>
<td>0.3396</td>
<td>0.1925</td>
<td>1.877</td>
<td>0</td>
</tr>
<tr>
<td>42</td>
<td>DIV_Bias</td>
<td>28</td>
<td>0.25</td>
<td>7</td>
<td>1</td>
<td>0</td>
<td>0.3396</td>
<td>0.698</td>
<td>0.1686</td>
<td>0</td>
</tr>
</tbody>
</table>
Current Activity: CMOS-Based Physics of Failure - NBTI

IBM 130 nm bulk technology
Nitrided SiO₂ gate dielectric

V₉₅ = -3.25 volts for 0 < t < 1500 s
V₉₅ = 0.00 volts for 1500 < t < 3000 s
V₉₅ = 1.50 for 3000 < t < 3500 s
V₉₅ = -1.00 for 3500 < t < 4000 s
Etc

Point of Contact: Rod Devine (505)-846-4822
roderick.devine.ctr@kirtland.af.mil


Question: Does this extend beyond 90nm?

Reprinted courtesy of AFRL

Approved for public release, distribution is unlimited. (PA # 377ABW-2012-0689)
130nm NBTI Stress Measurement

- Device stressed at $V_{\text{gate}} = -2.3 \ \text{V}$ at a temperature of 140 C
- Very little degradation observed even at 100 ks
- Initial BSIM model matches the initial measurement as well as it matches the post-stress measurement
- The 130nm 8rf PFET is insensitive to NBTI under these circuit conditions
HC Stress data for $V_d = 2.5\, \text{V}$ and $V_g = 1.25\, \text{V}$

- BSIM4 Models were matched to measured devices by parametric shifts in model parameters CIT, VTH, and Uo
  - *The threshold voltage increases with HCI stress due to charge trapping*
  - *Decreases in transconductance with aging were represented by a decrease in mobility resulting also from an increase in interface traps*
  - *The sub-threshold slope decreases with an increase in interface state density (CIT)*

Results show good model correlation with this approach

Modeling the lifetime for a particular circuit design, requires knowledge about the devices from that process lot and detailed simulation
HCI/NBTI Aging Simulation Process

- Establish BoL Circuit Sensitivities to Voltage, Temperature and Process
- Each transistor in the VCO/Divider Circuit was assigned a separate BSIM4 model instance.
- Variables were added to each BSIM4 model to account for parametric shifts from HCI/NBTI stress. The variables are contained in a separate “age” file that can be efficiently updated when new calculations are available.
- Parametric Shift variables included in the model are:
  - Mobility ($U_0$)
  - Threshold Voltage ($V_{TH0}$)
  - Interface Trap Capacitance ($C_{IT}$)
- The “aged” models were validated by comparing simulated NFET $I_d$-$V_g$ curve traces to measurements taken from actual aged devices.
- AC and DC bias conditions for each transistor in the circuit were tabulated and used to calculate HCI/NBTI stress and parameter shifts at 0, 10, 20 and 40 years.
- Circuit was run with updated parametric shift variables.
VCO / Divider Sensitivities

Temperature Sensitivity

The slope of the curve is 3.7mV/°C. To remain within the min/max data sheet specifications for output amplitude, the VCO/Divider would be restricted to an 8°C temperature range.

Bias Sensitivity

The Divider output varies by 0.5mV/1mV Vdd. To remain within the min/max data sheet specifications for output amplitude, Vdd would be restricted to +/-40mV.

Simulated at BOL, 27°C, and nominal process.
The Divider output varies by 660mV. To remain within the min/max data sheet specifications for output amplitude, the VCO/Divider would be restricted to within 6% of the process center.

Simulated at BOL, 27C, and nominal bias and process
Circuit age, temperature and process parameters can be selected from a pulldown menu.

Sample age model file with Vth, U0 and CIT parameter shifts for transistors 25 and 26.
130-nm AMS Sims Summary

• The output amplitudes of the VCO and Divider are sensitive to shifts in temperature, process and voltage
• The time to failure depends on the use conditions and definition of failure
• The process for simulating the 130nm circuit after aging is operating efficiently and providing good correlation to measured data
  – Performed simulations for 0, 10, 20, 40 years under worst-case bias/temperature conditions
• Next Steps Include:
  – Characterize phase noise as a function of age
  – Provide Bias/Temperature Recommendation for Life Testing Activity
  – Repeat for 90-nm 9SF AMS and 90/65-nm Digital Only Designs
90nm Digital ASIC Circuit Aging Status

- Received 90nm design database
- Full circuit logic simulation(s) performed
- Primetime Static Timing Analysis Done
- Primetime Si SPICE Netlist extraction of worst-case path(s) complete
- HSPICE Simulation of timing paths begun
- 90nm Aged MOS models under development
Next Step: Physics of Failure - Based Circuit Modeling

- Done using Xyce™ developed at Sandia National Lab
- Designed for large-scale problems
- Potential access to source code
- Access to local expertise
- Xyce has radiation modeling, which could be obtained in the future.

Future Work

PoF based development of $V_{th}(t)$
- Experimental dependence on bias, $T$, duty cycle and frequency must be developed and then extrapolated to years.

Single NAND gate with a 1fF load

Multiple NAND gates

Initial Circuit Testing Done on a Ring Oscillator
- 50% duty cycle is ideal
- Common circuit
- 11 NAND gates using the 65 nm PTM models
- Base frequency of 3.5 GHz
- For $\Delta V_{th}=-0.1$ volts the frequency drops by 15%

Point of Contact: Kenneth Kambour (505) 853-3157
kenneth.kambour.ctr@Kirtland.af.mil

Presented at MRQW Dec. 2011

Reprinted courtesy of AFRL
Approved for public release, distribution is unlimited. (PA # 377ABW-2011-1645)
Full Chip 90nm CMOS ASIC Reliability Modeling Tool

Specify chip basic information:
- Die area
- Geom.
- VDD
- # gates
- Etc.

Interconnect statistics (Rent’s Rule) 100%

Specify environment in first hour (T, V, off time cycles, Frequency, etc.)

Electro-migration 100%

Stress Voiding 40%

NBTI 100%

Dielectric Breakdown

Hot Carriers

Packaging Factors

Perform running sum to generate cumulative hazard

Increment time 100%

Sum

Extract Probability of failure vs. time $P_f(t)$, & overall failure rate $\lambda$.

Contact: John Scarpulla or Jon Osborn
Digital ASIC Lifetime Failure Criterion
(i.e. 1 failure per week or per year, …etc.)

Distribution of delta delays due to all failure modes $\Sigma$ over all corners

### Timing slack

- **ASIC Timing slack**
  - Ex: 100ps

### Probability of a negative timing slack (BER Requirement)

- User’s tolerance for bit errors is expressed as BER requirement

### Ex: At one 1GHz, 1 Failure per Week
- **BER** = $10^{-14}$

Contact: John Scarpulla or Jon Osborn
Ex: NBTI User Dashboard Inputs

Contact: John Scarpulla or Jon Osborn
Ex: Mission Use Condition

Specified mission temperature and on/off state

- Temperature (°C)
- time (hours)
- Specified mission temperature and on/off state
- on=1, off=0

Contact: John Scarpulla or Jon Osborn
Ex: Time evolved FIT rate calculation

Contact: John Scarpulla or Jon Osborn
CMOS ASIC PoF Lifetime Modeling – Looking Forward

• Develop PoF MD/DFT models of each of the major CMOS Failure Modes (Atomistic-Level)
  – *Provides better understanding of PoF and basic mechanisms*
  – *Coupled with nano-scale DPA, may enable in silico reliability prediction*

• Develop automated process to extract RelExpert compatible aged MOS models for any process node (Device-Level)
  – *BSIM Pro+ AgeMOS does not do SOI and Foundry Models are proprietary*
  – *Enables process specific End-of-Life Analog Mixed Simulation of circuits*

• Develop process to include BEOL wear-out mechanisms into circuit-level reliability simulator (Circuit-Level)

• Develop automated process to extract time evolved digital cell library timing degradation models (Circuit-Level)

• Complete Full-Chip 90nm CMOS ASIC Simulator (ASIC-Level)

• Develop advanced packaging time evolved failure rate models (ASIC-Level)
Summary

• HiREV nanoCMOS PoF Modeling Progress is Steady
  – *Primarily addressing device/circuit/ASIC lifetime reliability*
  – *Expanding into basic mechanisms and packaging*

• Multiple Technology Nodes Under Investigation
  – *Program Pull at 130/90/45nm*
  – *IR&D Interest at 32nm*

• Many opportunities for NEPP and HiREV to collaborate on PoF reliability data collection and model development at device/circuit/ASIC as well as package/board/unit levels of integration

Need more info?
Contact: Jon Osborn, Jon.V.Osborn@aero.org, 310-336-5453
Acknowledgement

“This work supported by the National High Reliability Electronic Virtual (HiREV) Center under AFRL Support”

and

“This work supported by The Aerospace Corporation under the “Reliability By Design Corporate Research Initiative”

“All trademarks, service marks, and trade names are the property of their respective owners”