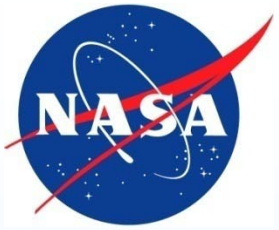
NEPP Electronic Technology Workshop
June 11-12, 2013

National Aeronautics
and Space Administration



Radiation Qualification of Flash Memories

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To be presented by Dakai Chen at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-12, 2013 and published on nepp.nasa.gov.

Outline

- Purpose of the test guideline
- Key considerations
- Single event effects (SEE)
- Proton susceptibility
- Total ionizing dose (TID)
- Combined effects (TID + Reliability)
- Lessons learned

Purpose

- **Provide guidance to space flight programs and technology developers for radiation testing and qualification of nonvolatile memories (NVMs), with emphasis on modern flash memory devices**
- **Key contributors: Tim Oldham – primary author, Steve Buchner, Ken LaBel**

How to Test Flash Memory?

- What are you looking for?
- Know the environment – what type of particles will the part be exposed to?
- How will you operate the Flash throughout the mission?
- How to select beam parameters?
- What is the degradation mechanism?

SEE Testing

- **ASTM F1192 – Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices**
- **Determine the applicable operation modes**
- **Understand the error modes**
- **Heavy ion testing and alternative sources**
- **Susceptibility to protons**

ASTM International, known until 2001 as the American Society for Testing and Materials (ASTM)

Operating Conditions

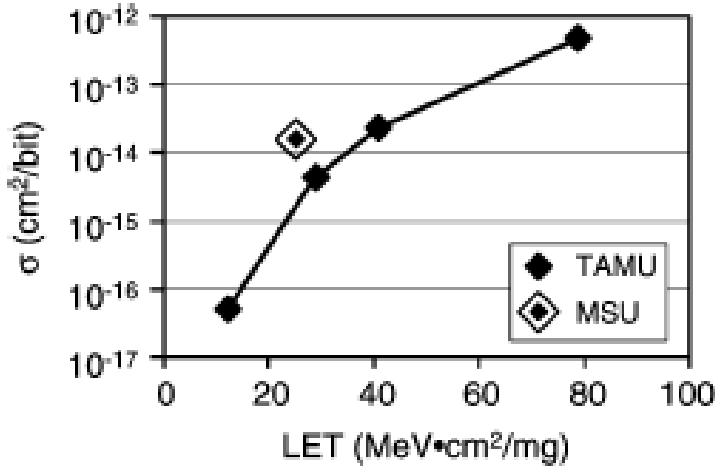
- **Operation modes**
  - **Static mode (powered and unpowered), dynamic Read, dynamic Read/Write, dynamic Read/Erase/Write**
- **Pattern sensitivity**
  - **0 to 1 errors common than 1 to 0 errors**
  - **Checkerboard pattern ideal to check for both error types**
- **Frequency sensitivity**
  - **Not a challenge due to the lower operating speeds relative to volatile memories**

SEE Error Modes

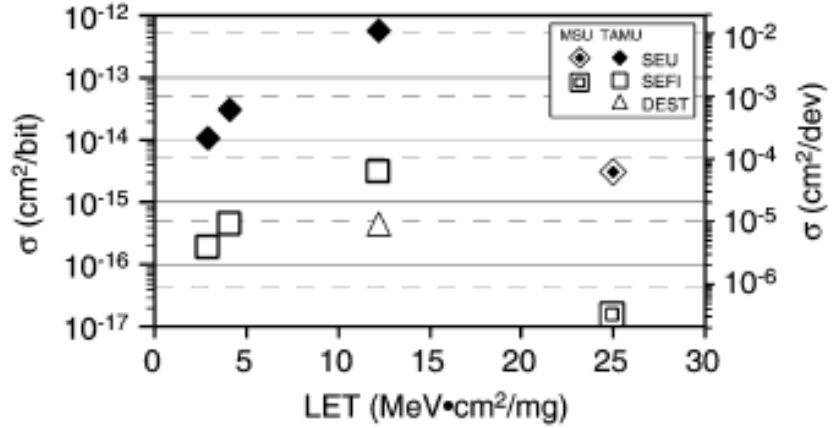
- **Single bit upset**
  - **Memory cell charge leakage**
- **Multiple bit upset**
  - **Typically due to control circuit error**
- **Stuck Bits**
  - **Micro-dose effects**
- **Functional Interrupt**
  - **Control logic error leading to large scale errors (page or block errors)**
- **Functional Failure**

TAMU = Texas A&M University; MSU = Michigan State University;
R/E/W = Read/Erase/Write operation

Static mode



Dynamic mode (R/E/W)

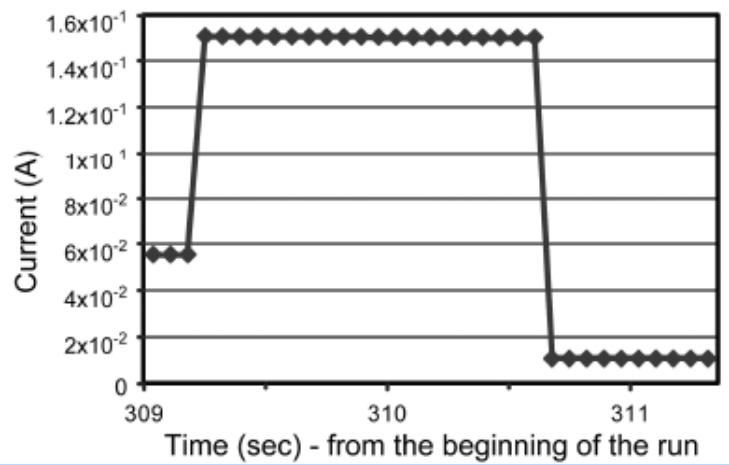


T. R. Oldham, et al., *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3217-3225, Dec. 2006.

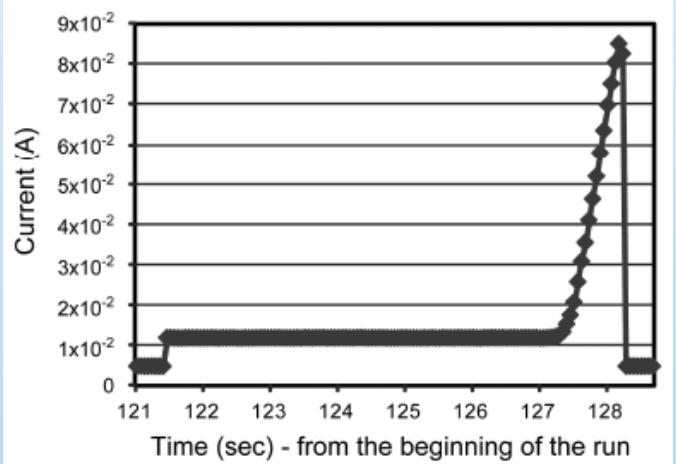
Functional Failure

- **Destructive events can be caused by Single Event Gate Rupture (SEGR) or Single Event Latchup (SEL)**
- **Micro-latchups and SEGR can result in current spikes**
- **Signal contention can also cause SEL resulting in current spikes (multiple ion effect)**
- **Sensitive components located in the peripheral control circuits**
  - **Current spikes do not necessarily originate from the charge pump**
  - **Combinatory logic vulnerable to signal contention**

Micro-latchup



Signal contention



T.R. Oldham, et al., IEEE Radiation Effects Data Workshop Record, Las Vegas, NV, July 2011. pp. 152-160.

Heavy Ion Beam Parameters

- Choose ions with appropriate linear energy transfer (LET) and energy
  - Recommend test with at least four different effective LETs
- Flux should be kept low enough to prevent multiple ion effects
  - Signal contention can cause SEL resulting in current spikes
- Fluence should be high enough for sufficient coverage
  - Test standards typically require 1×10^7 ions/cm^2
  - Average of 1 ion per 10 μm^2
  - Sufficient for deep submicron feature size technologies?
- Angular sensitivity
  - Increase in importance as feature size shrinks
  - May have greater impact for MLC devices

SEL = single-event latchup; MLC = multi-level cell

Other Sources to Evaluate SEE

- **Pulsed-Laser**
  - **Allows ability to identify locations of sensitive components (target the control circuits)**
  - **More cost effective than heavy ion testing**
  - **Not feasible if topside penetration is difficult**
  - **Two photon absorption for substrate penetration**
- **Milli-beam**
  - **Greater precision than broad beam, less precision than laser**
  - **Replicated some high current events; collective effects still possible**

Protons Susceptibility

- **Protons produce both SEE and TID (and Displacement Damage)**
- **When to evaluate for proton-induced SEE?**
- **Heavy ion upset threshold LET less than 15 MeV·cm^2/mg**
  - **Maximum LET from nuclear recoils with silicon atoms**
  - **Limited range of recoil atoms relative to heavy ions**
  - **Inappropriate to evaluate destructive effects**
- **Not particularly sensitive to SEE based on limited test results**

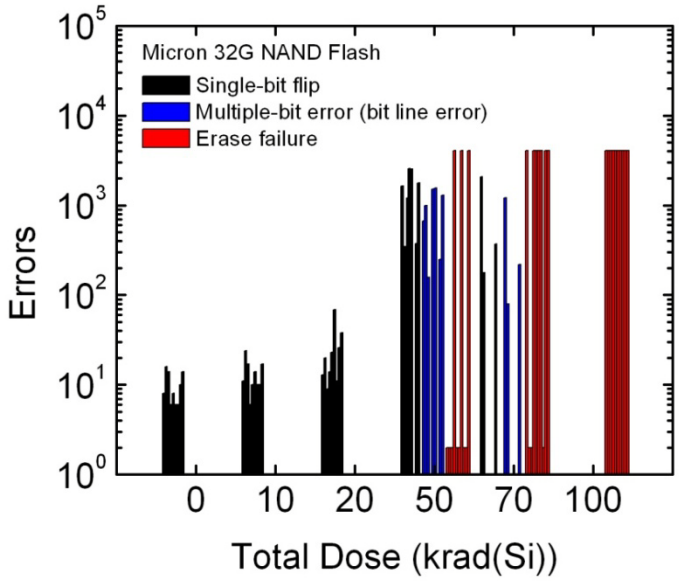
SEE = single-event effects; TID = total ionizing dose; LET = linear energy transfer

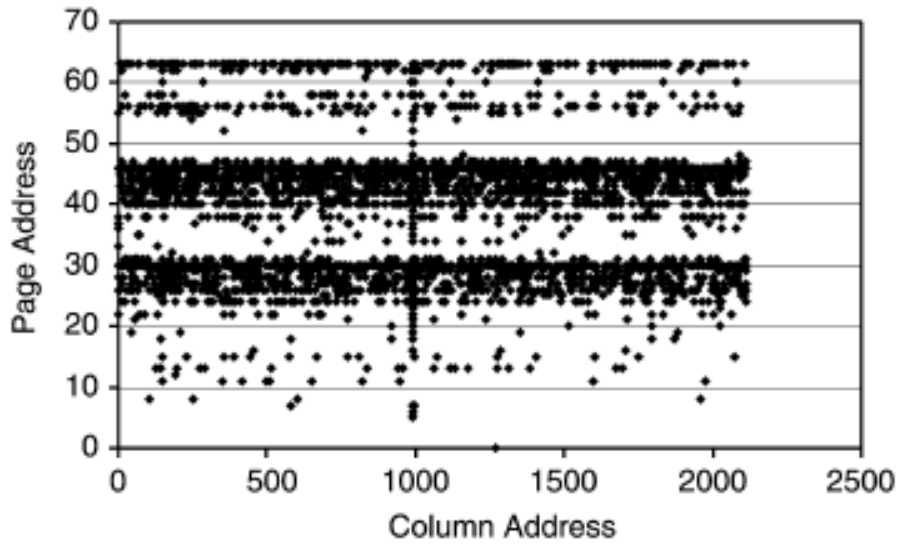
TID Testing and Combined Effects

- **Test standard: MIL-STD-750 Test Method 1019**
- **Typically flash will remain in static bias (or unpowered) or standby mode for the majority of the mission duration**
- **Device characterization**
  - **Accumulated bit flips: Read only during exposures**
  - **Operational functionality: Cycled (R/E/W) during exposure**
  - **Large sample size can be a challenge (at least 5 for each condition)**
- **Does TID affect retention and endurance?**

TID = total ionizing dose; R/E/W = Read/Erase/Write; CMOS = complementary metal oxide semiconductor

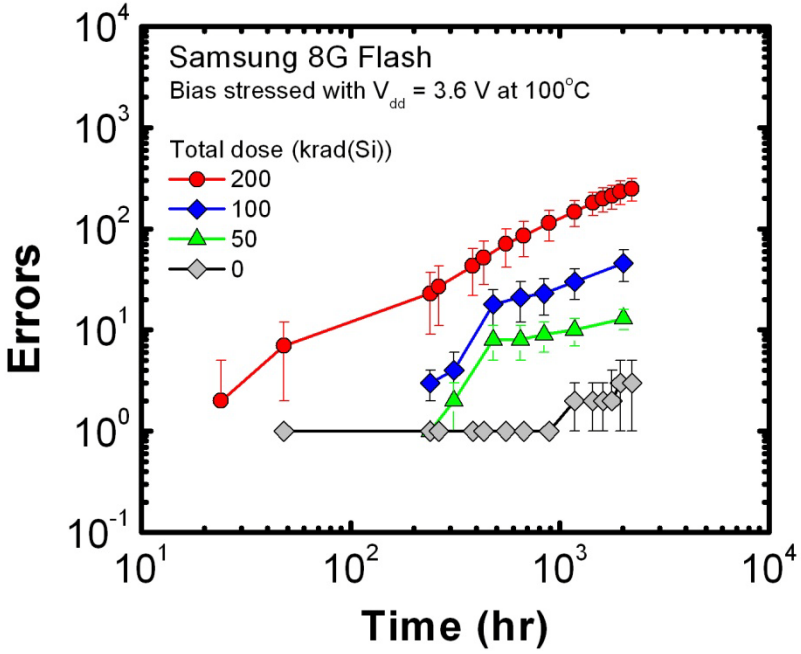
TID Degradation Characteristics





- **Single bit errors are primarily 0 to 1 errors**
- **Bit line and word line errors cause multiple-bit errors**
- **Functional failure due to inability to perform block erase**
- **Annealing can correct some bit errors, but charge pump failures are difficult to recover**

Combined Effects



T. R. Oldham, et al., *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 3011-3015, Dec. 2012

- **Parts will experience TID and aging in flight**
- **TID irradiation followed by 1000 hour life test: 10% overvoltage, 100°C**
- **Retention errors increase with increasing TID**
  - **Nonlinear dependence: 4x increase in dose caused 20x increase in errors**
- **Single bit errors dominate**
- **ECC expected to correct these errors**

TID = total ionizing dose; ECC = error correcting code

Error Correction

- **Most NAND flash will NOT meet its performance or reliability specifications without ECC**
- **Most SLC NAND have about 3% redundant memory for ECC**
  - **8G NAND has pages 4Kx8, or 32 Kbits, with an additional 128 bytes (1024 bits) for ECC**
- **Simple Hamming code for a memory segment of 2^N bits requires N+1 bits for SEC (single error correction), or N+2 bits for SEC-DED (SEC-double error detection)**
- **ECC implementation is vital for on-orbit applications, however ECC will not resolve control logic errors**

ECC = error correcting code; SLC = single-level cell (as opposed to MLC = multi-level cell)

TID Testing Lessons Learned

- Memory arrays are naturally robust against TID
- Control circuits are most vulnerable and critical
- Charge pump failures often determine TID hardness
- Necessary to cycle some parts in between doses to check for E/W functions
- TID can reduce retention over time, however errors correctable via ECC

TID = total ionizing dose; E/W = Erase/Write; ECC = error correcting code

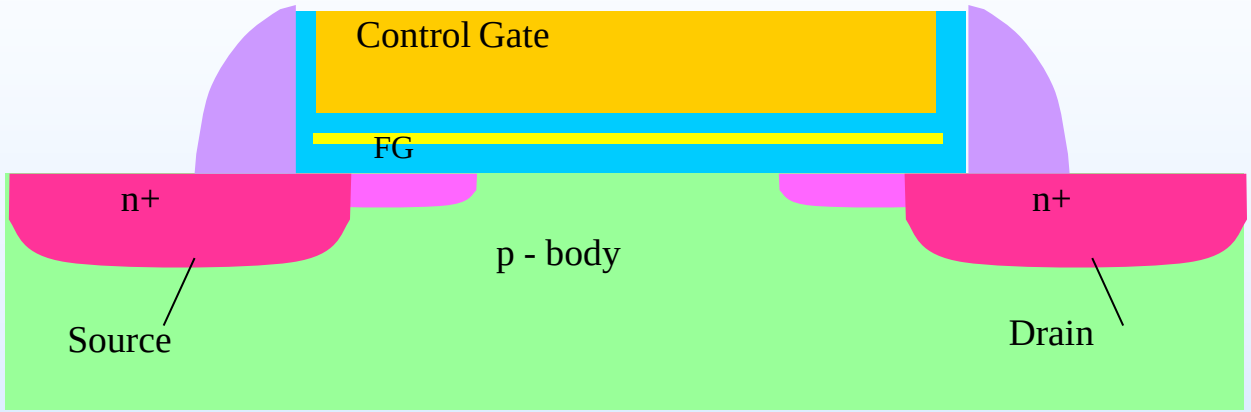
SEE Testing Lessons Learned

- **Choosing heavy ion beam parameters**
  - **Ion LET, energy and range**
  - **Keep flux low to avoid multiple ion effects**
  - **Irradiate to high fluence for good statistics—trade offs to make effective use of beam time**
  - **Highly scaled CMOS can be sensitive to angular effects**
- **Page/block errors and destructive events can originate from the control circuit**
- **Laser and milli-beam testing offer capability of better resolution to identify sensitive locations**
- **Proton sensitivity should be monitored closely**

LET = linear energy transfer; CMOS = complementary metal oxide semiconductor; SEE = single-event effects

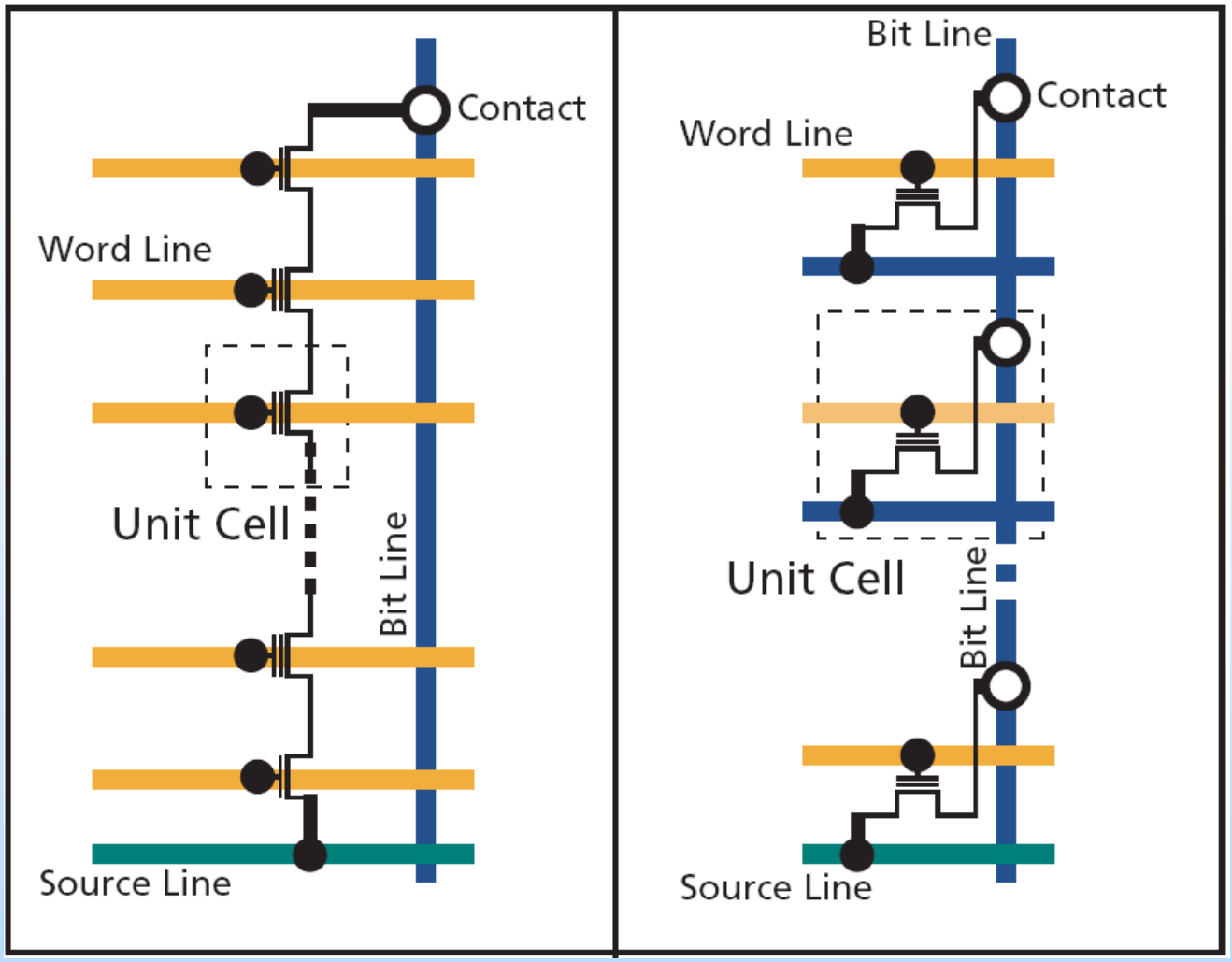
Backup Slides

Floating Gate Transistor



- **Write (Program) operation—Fowler-Nordheim (FN) injection of electrons into FG**
- **Erase operation—FN injection of electrons from FG to substrate**
- **Floating gate structure naturally hardened from charge leakage**
- **Control circuit elements, such as high voltage charge pumps, are more vulnerable to radiation-induced degradation**

Flash Architectures



NAND NOR

Why Flash?

- **Most mature Non-volatile memory technology**
  - **Low cost per bit**
  - **High density**
  - **Low power consumption**
- **Attractive for space applications for the same reasons widely used in handheld, battery powered, consumer electronics**
- **Radiation response is variable, as one would expect for unhardened commercial technology, but often pretty good**