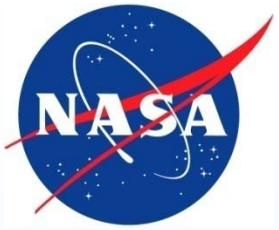
NEPP Electronic Technology Workshop
June 11-12, 2013

National Aeronautics
and Space Administration



Single Event Effects in Field Programmable Gate Array (FPGA) Devices: Update 2013

Melanie Berg

MEI Technologies, work performed for NASA GSFC;

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To be presented by Melanie D. Berg at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-12, 2013 and published on nepp.nasa.gov.

NASA Goddard Radiation Effects and Analysis Group (REAG) FPGA Testing Supporters and Collaborators

- **Supporters:**
  - **Defense Threat Reduction Agency (DTRA)**
  - **NASA Electronics Parts and Packaging (NEPP)**
- **Collaborators:**
  - **Xilinx**
  - **Satellite Servicing Capabilities Office (SSCO)**

FY12-FY13 Accomplishments– SEU Testing

- **Xilinx Virtex 5-QV field programmable gate array (FPGA)**
  - **Tests Performed:**
    - **August 2013,**
    - **November 2013, and**
    - **May 2013**
  - **Data is currently being processed and is under a nondisclosure agreement. For further information concerning data – see Kenneth LaBel**

FY12-FY13 Accomplishments – Presentations

- **Presented at the Radiation Effects on Components and Systems Conference September 2012: "Characterizing Data Path Single Event Upsets in a Synchronous Design"**
- **Presented at the Microelectronics Reliability and Qualification Workshop December 2012: "An Overview of the NASA Goddard Methodology for FPGA Radiation Testing and Soft Error Rate Prediction"**
- **Presented at the Single-Event Effects (SEE) Symposium April 2013: "Differentiating Scrub Rates between Space-Flight Applications and Accelerated Single-Event Radiation Testing for SRAM based Field Programmable Gate Arrays"**
- **Presented at the Single-Event Effects (SEE) Symposium April 2013: "Single Event Upsets (SEUs) That Cause Unanticipated Multiple Bit Upsets (MBUs) in Complex Designs and the Effects of Logic Masking"**
- **Presented at the Single Event Effects (SEE) Symposium April 2013: "An Overview of the NASA Goddard Methodology for FPGA Radiation Testing and Soft Error Rate (SER) Prediction "**

SRAM = static random access memory

FY12-FY13 Xilinx V5-QV Heavy Ion Accelerated Testing

V5 is a commercial Xilinx filed programmable gate array device; V5-QV is a radiation-tolerant device

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FPGA Structure Categorization as defined by NASA Goddard REAG:

REAG = Radiation Effects and Analysis Group is part of NASA/GSFC Code 561

SEU Cross-Sections (σ_{SEU}) = #upsets/particle/cm^2

$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Design σ_{SEU}

Configuration σ_{SEU}

Functional logic σ_{SEU}

SEFI σ_{SEU}

Sequential and Combinatorial logic (CL) in data path

Global Routes and Hidden Logic

We study σ_{SEU}s for each of the FPGA categories. Design test structures will depend on the category of investigation

Configuration Testing

- **Basic Configuration Static Test:**
  - **Load FPGA configuration**
  - **Irradiate device while the device is in a static state (no scrubbing of configuration memory)**
  - **Stop radiation beam and read back the configuration**
  - **Count configuration upsets and normalize by the number of particles of exposure (Configuration SEU cross section – σ_{SEU})**
- **All tests (regardless of type) include configuration read-back after each beam-run**

Xilinx V5-QV Heavy Ion Accelerated Testing: Test Structure Development – Functional Logic

- We start with simple test structures
- We increase complexity per test structure
- We study trends
- We try to make sense out of the convoluted data obtained from complex test structures

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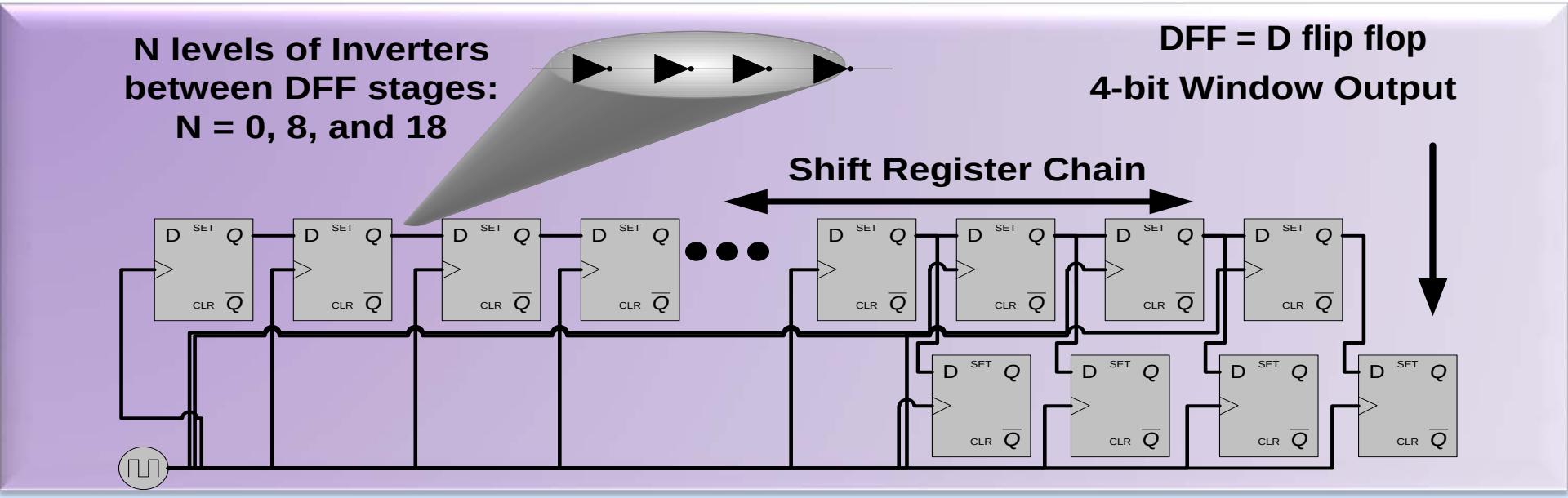
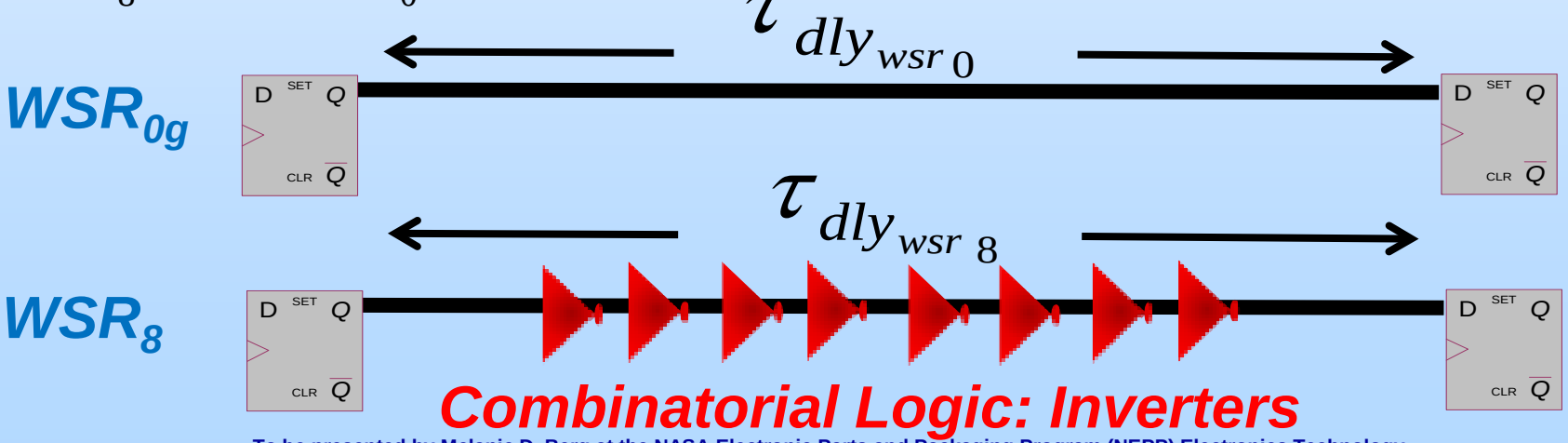
Functional Logic Radiation Test Structures: Windowed Shift Registers (WSRs)

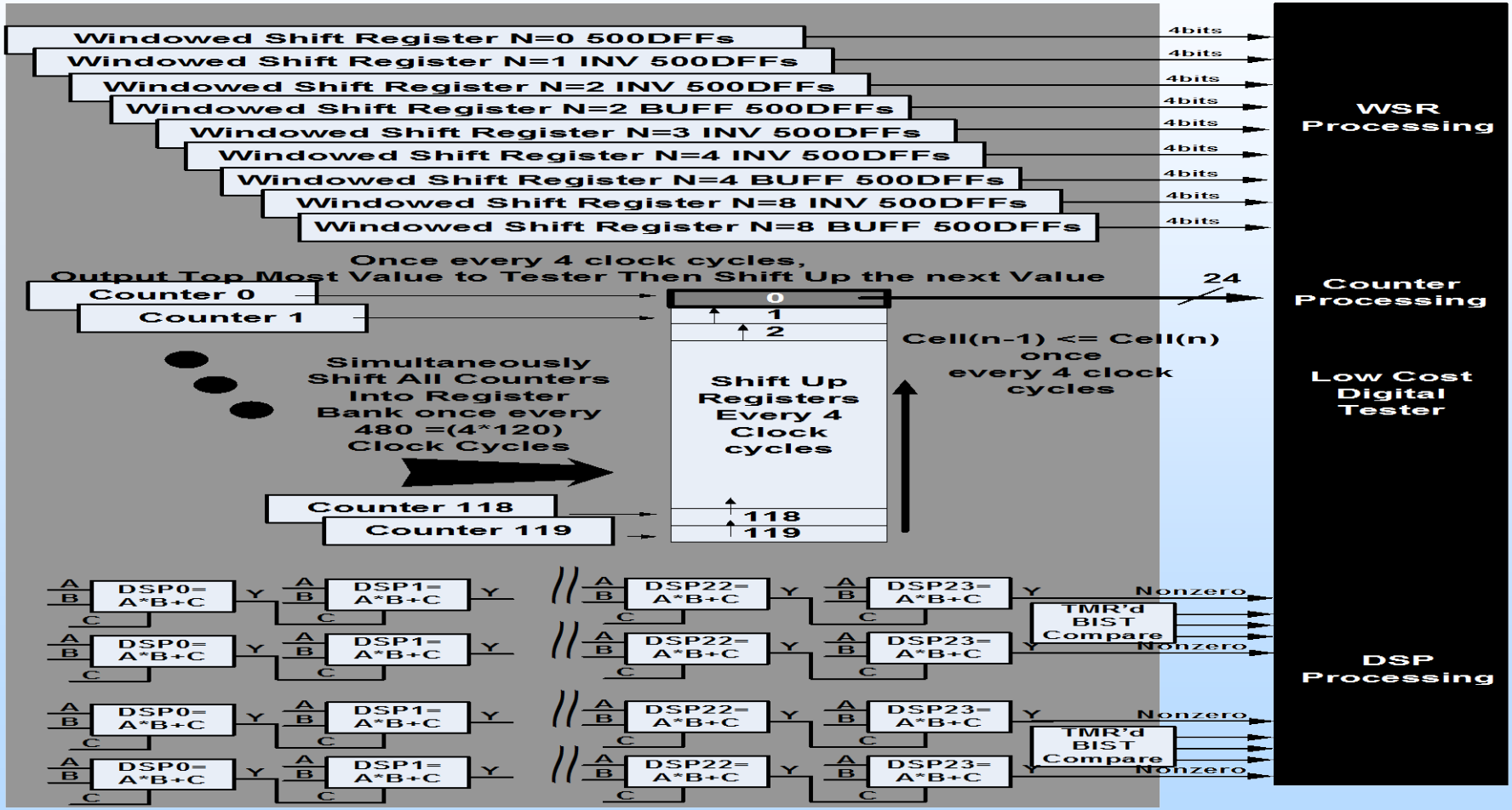


$\tau_{dly_{wsr\ 8}} > \tau_{dly_{wsr\ 0}}$

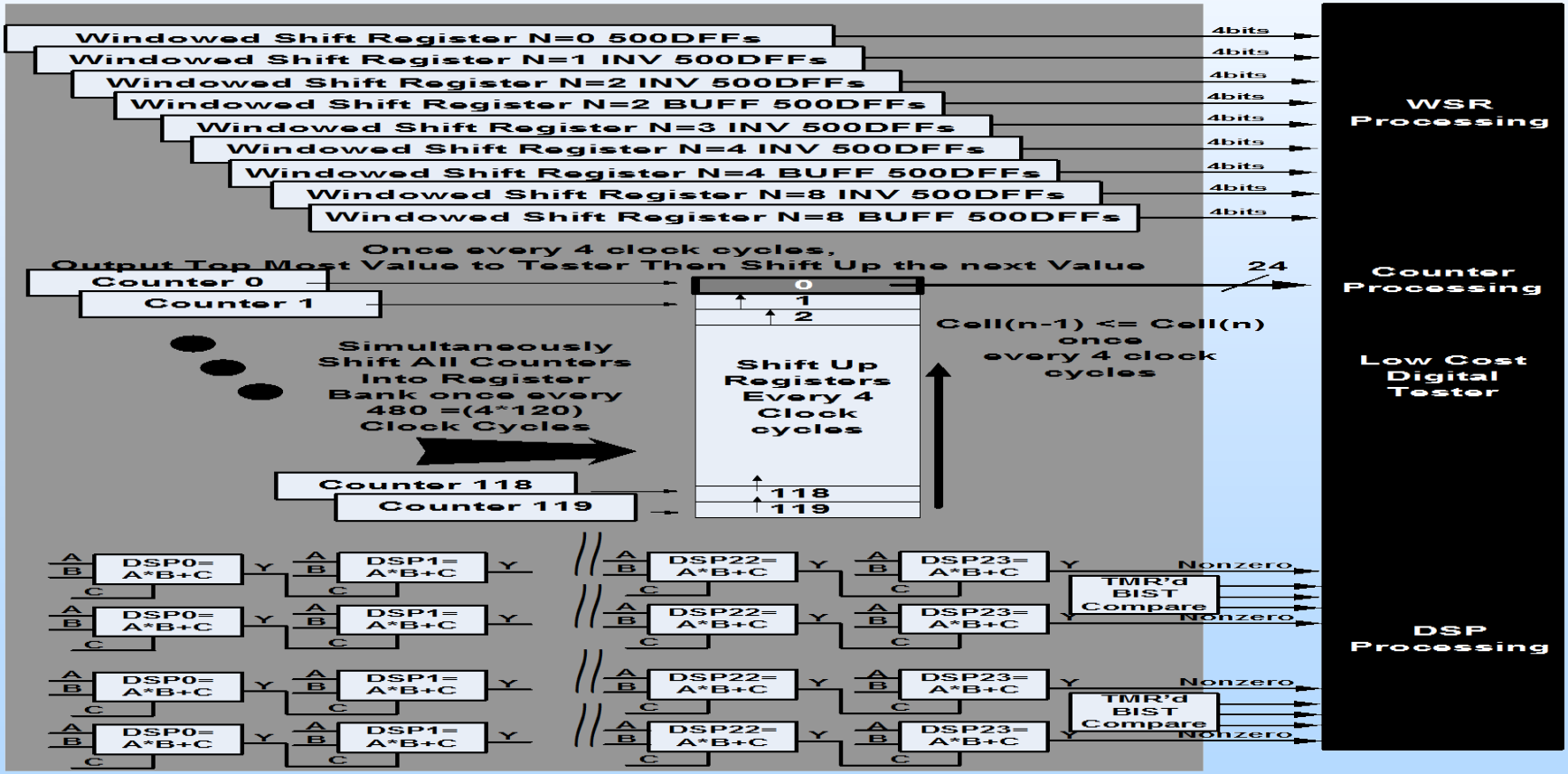
τ_{dly} = path delay from DFF to DFF



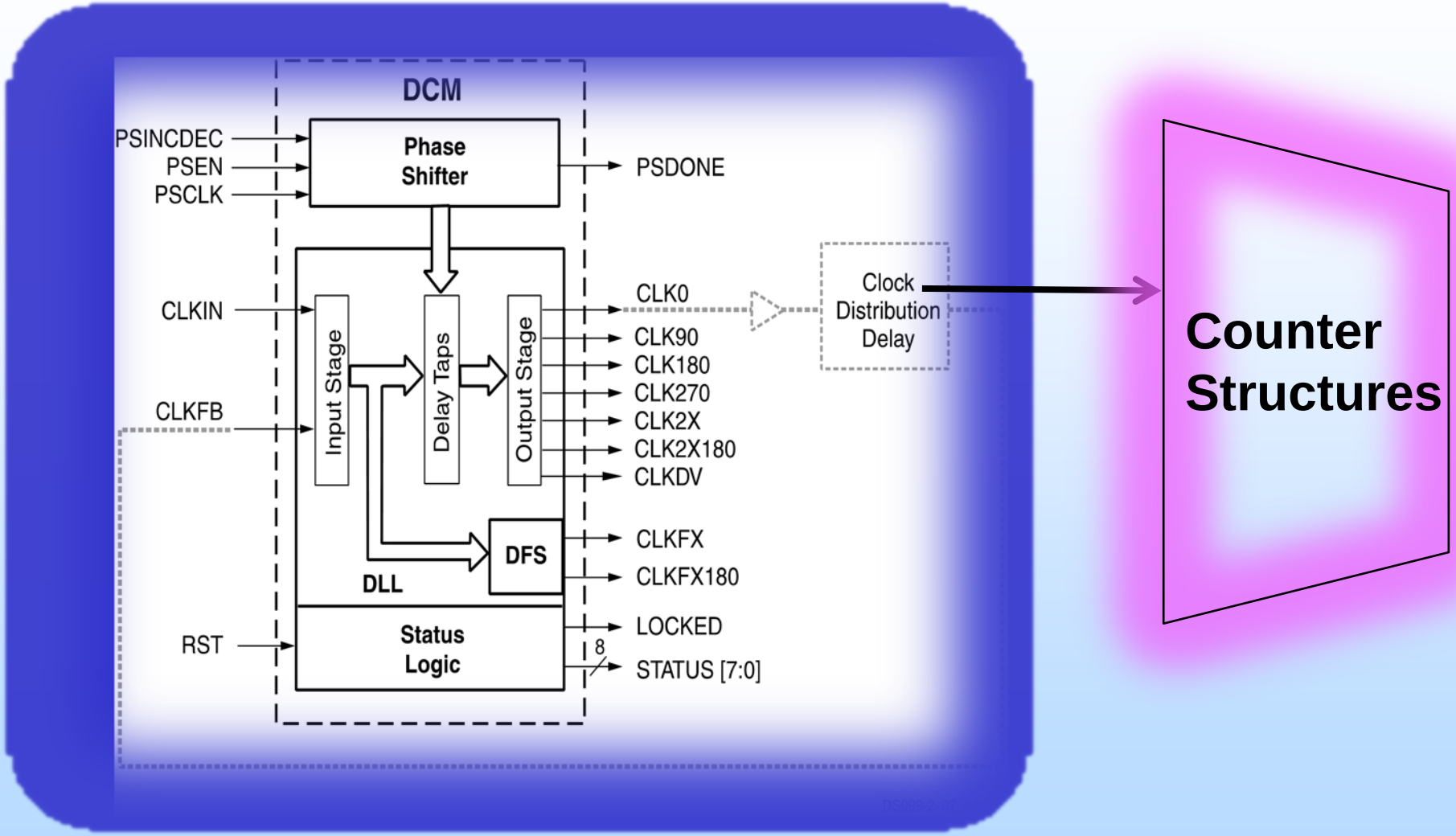
Functional Logic Radiation Test Structures: Counters



Functional Logic Radiation Test Structures: Digital Signal Processors (DSP)



Functional Logic Radiation Test Structures: Digital Clock Manager (DCM)



We are testing DCM susceptibility by connecting the block to a design with a state space with feedback

Investigating SEFIs

We look for particular error signatures to determine SEFI occurrence:

- **Read-back of configuration is mostly logic '0' – assume a Power On Reset (POR) glitch**
- **Unable to connect to the device to read-back – assume problem in the configuration interface**
  - **Hidden (to user) state machines**
  - **Configuration registers**
- **Global upsets in functional logic**
  - **Reset correction: clock tree or reset tree (global routing)**
  - **Configuration correction: configuration bit upset – not considered a SEFI**

SEFI: single event functional interrupt

TMR: Triple Modular Redundancy;
SET: Single Event Transient;

V5-QV Heavy Ion Accelerated Testing: Mitigation: TMR, Embedded SET Filter Insertion, and Scrubbing

Unlike the commercial Xilinx devices, the configuration in the V5-QV is hardened, hence we can evaluate various levels of TMR

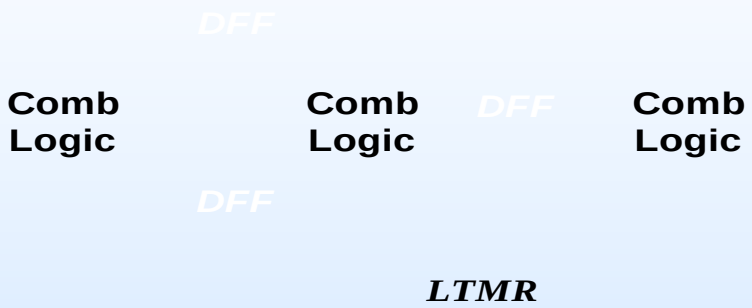
$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Low

Design σ_{SEU} — Configuration σ_{SEU} — Functional logic σ_{SEU} — SEFI σ_{SEU}

V5-QV is a radiation-tolerant device

Radiation Test Structures: Local Triple Modular Redundancy (LTMR)



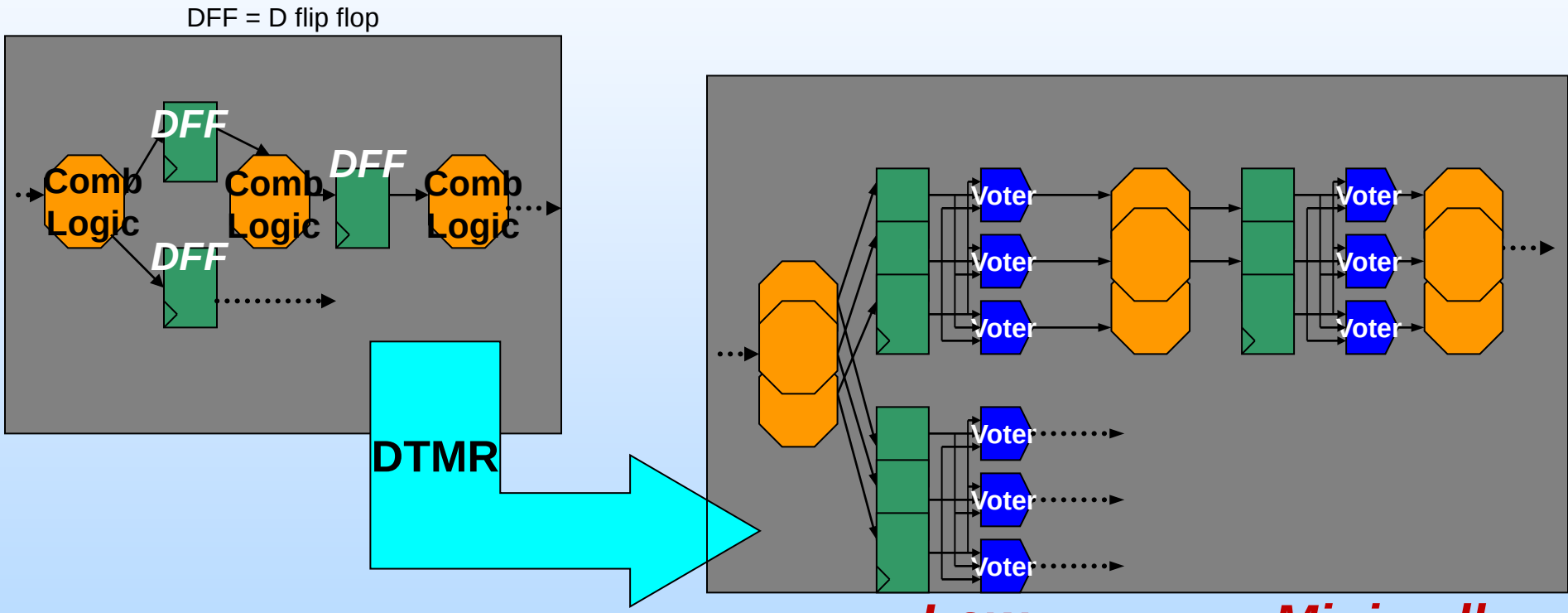
Masks upsets from DFFs

Corrects DFF upsets if feedback is used

DFF = D flip flop

Only the DFFs are triplicated and mitigated

Distributed Triple Modular Redundancy (DTMR): DFFs + Data Paths All DFFs with Feedback Have Voters

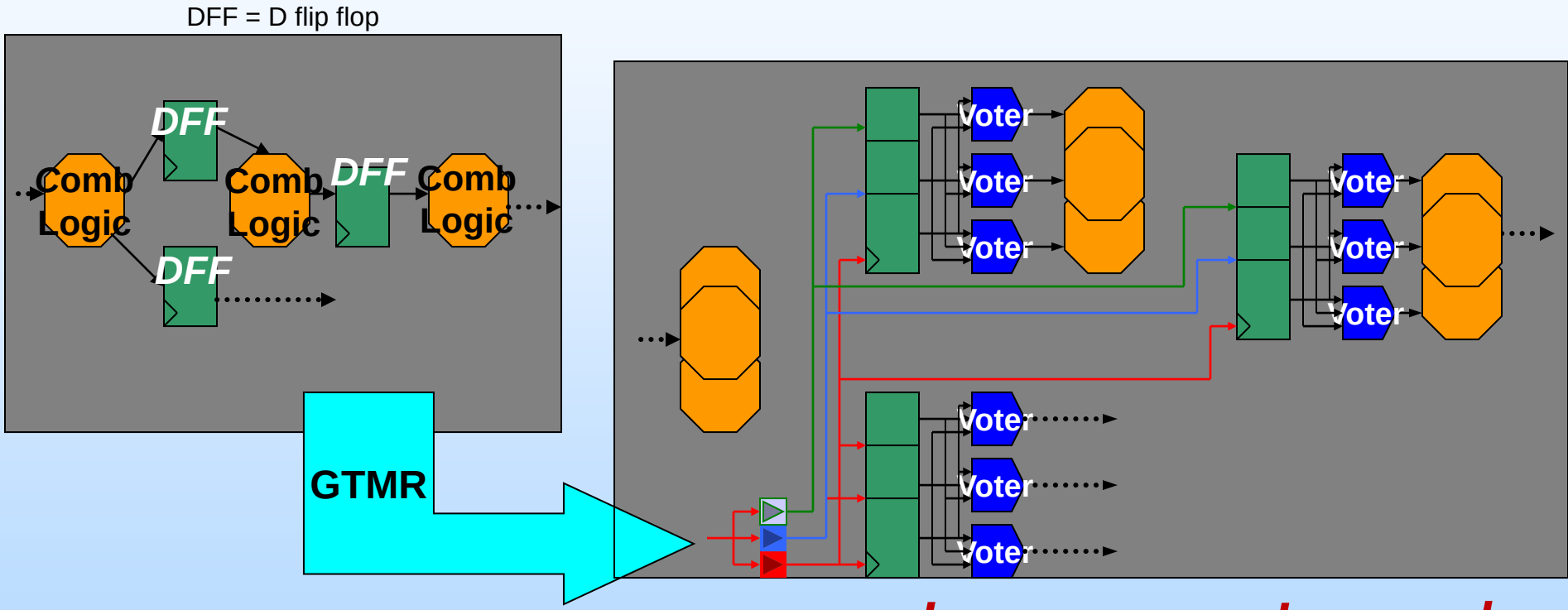


$$P(f_s)_{error} \propto P_{configuration} + P(f_s)_{functionalLogic} + P_{SEE}$$

Low

Minimally Lowered

Global Triple Modular Redundancy (GTMR):DFFs + Data Paths + Global Routes
All DFFs with Feedback Have Voters



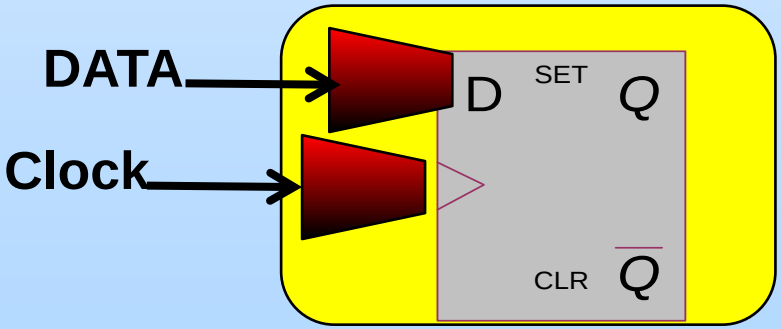
$$P(f_s)_{error} \propto P_{configuration} + P(f_s)_{functionalLogic} + P_{SEFI}$$

Low

Lowered

V5QV Embedded Single Event Transient Filters

- **The V5-QV has embedded SET filters placed on the data input and clock input of each DFF. Usage is optional**
- **Filters are expected to reduce the effects or the capture of SETs**
- **Xilinx reports that the SET filters reduce susceptibility**
- **NASA Goddard REAG has verified this claim**



SET: Single Event Transient;
DFF: flip-flop
REAG = Radiation Effects and Analysis Group is part of Code 561 at NASA/GSFC

Scrubbing Specifics

Scrubbing is the act of simultaneously writing into FPGA configuration memory as the device's functional logic area is operating with the intent of correcting configuration memory bit errors

- **Too many upsets in the system (due to accelerated flux) can cause unrealistic behavior… unrealistic σ_{SEU}s!**
- **Can manage the accelerated upset rate by varying flux**
- **Make sure scrubbing can keep up with your upset rate**
- **During irradiation our scrub rate for the Xilinx V5-QV is once every 100ms.**
- **Read-back after a test with scrubbing should have minimal number of configuration-bit upsets (excluding un-scrubbable bits)**

FPGA: field programmable gate array

σ_{SEU}: SEU cross-section

Test Designs and Mitigation

- **Shift registers were tested with:**
  - **No TMR, LTMR, DTMR, and GTMR**
  - **SET Filters on and SET Filters off**
  - **Configuration scrubbing**
- **Counters were tested with**
  - **No TMR, LTMR, DTMR**
  - **SET Filters on and SET Filters off**
  - **Configuration Scrubbing**
- **DSPs were tested with:**
  - **No TMR**
  - **SET Filters on and SET Filters off**
  - **Configuration Scrubbing**

LTMR: Local Triple Modular Redundancy;

DTMR: Distributed Triple Modular Redundancy;

GTMR: Global Triple Modular Redundancy;

SET: Single Event Transient;

DSP: digital signal processor block

V5-QV Heavy Ion Accelerated Testing: More Complex DUTs…MicroBlaze™ Soft Processor Core Testing

V5 is a commercial device; V5QV is a radiation-tolerant device

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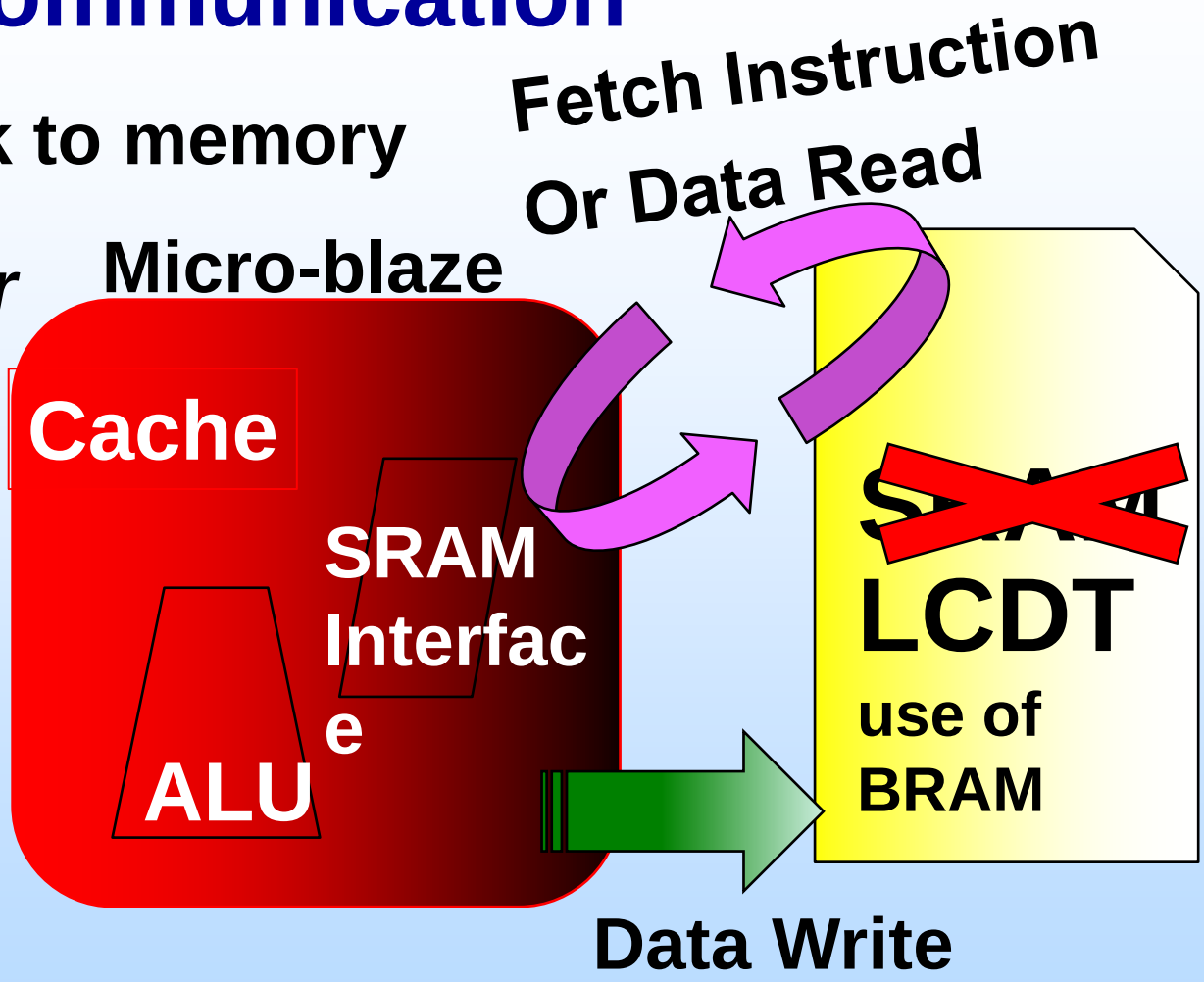
Processor and SRAM Communication

SRAM: Static random access memory
BRAM: Block random access memory

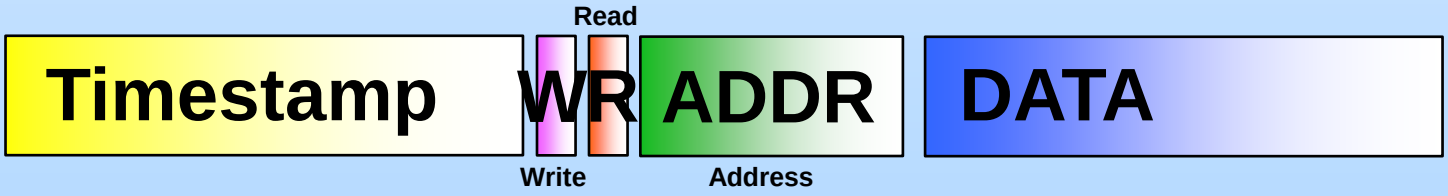
- **Processors talk to memory**
- ***Most processor radiation tests detect errors by erroneous SRAM memory writes***
- ***Visibility is limited***



- ***We increase visibility by replacing SRAM with the REAG low-cost digital Tester (LCDT)***

More on Increasing Visibility with Microprocessor Testing (1)

- As previously stated, the embedded SRAM in the tester (BRAM) takes the place of normal memory accesses
- In addition, each memory access is time stamped and logged in alternate bank of BRAM. Only the last 512 accesses are kept
- After each test run, the time stamped logs are output to the user



More on Increasing Visibility with Microprocessor Testing (2)

DUT: device under test

DUT

- Halted
- Error
- Trace Instruction
- Trace Valid Instruction
- Trace Exception Taken
- Trace Exception Kind
- Trace Register Write
- Trace Register Address
- Trace data cache Request
- Trace data cache Hit
- Trace Data cache Ready
- Trace Data cache Read
- Trace Instruction cache Request
- Trace Instruction cache Hit

TESTER

Watchdogs

Send watchdog errors to host PC

Future Plans

REAG Plans

- **V5-QV Testing FY13:**
  - **Configuration**
    - **Additional analysis of configuration SEFIs**
    - **Finish analyzing SEE information**
  - **Complete micro-blaze testing**
  - **Complete DCM testing**
- **Other devices FY13-FY14:**
  - **Xilinx Virtex 7 FPGA:**
    - **Configuration, TMR'd designs, SEFIs, clock tree structures, and more…**
  - **Microsemi RTAX4000D FPGA:**
    - **Integrated processor including usage of embedded DSP blocks**

SEFI = single-event functional interrupt; POR = power on reset;
SEE = single-event effect; DCM: Digital Clock Manager
TMR: Triple Modular Redundancy; DSP: Digital Signal Processing