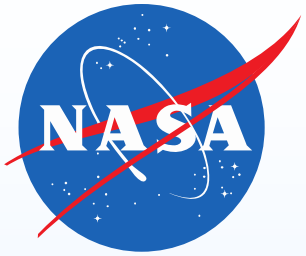

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CubeSat and Mobile Processors

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Acknowledgment:
This work was sponsored by:
The NASA Electronic Parts and Packaging Program (NEPP)

Outline

- Processor/Microcontroller Review
- Collaborations
- MSP430
- PIC
- Atmel AT91SAM9G20
- Intel Atom E620
- Snapdragon (APQ8064)
- Future/Conclusions

Motivation

- **Provide SEE and TID test data on processors and microcontrollers of interest for CubeSat and Small Missions**
  - **CubeSat Kit devices**
  - **Devices either flying or in designs being built**
  - **(and if enough interest, devices people would like to fly)**
  - **Future-looking devices**
- **Microcontroller focus is primarily on devices that are in designs right now – these are essentially the embedded market**
- **Microprocessor focus is on mobile devices where power is low and performance to power ratio is high**

Microcontroller Review

- Review of CubeSat kits
- Review of NASA CubeSat parts lists
- Direct interaction with community members

Device	Manufacturer	CubeSat?	NASA Sats	Others
MSP430F1611	TI	X		
MSP430F1612	TI	X		
MSP430F1618	TI	X		
MSP430F2619	TI		X	
MSP430FR5739	TI			X
C8051F120	Silicon Labs	X		
PIC24FJ256GA110	Microchip	X		
dsPIC33FJ256GP710	Microchip	X		
AT91SAM9G20	Atmel	X	X	
AT91SAM7	Atmel	X		
ATMEGA1281	Atmel	X		
ATMEGA164P	Atmel		X	
ATMEGA32U/8	Atmel		X	X
ATMEGA16U2	Atmel			X
Cortex-M3 MCU	ARM/General	X		
Other ARM9	ARM/General		X	X
PX32A	Parallax	X	X	
ColibriPXA270	Intel/Marvel			X
Sitara AM3505	TI		X	
Sitara AM3703	TI		X	X

Mobile Processor Review

- **Various CubeSats have flown with more capable processing**
  - **Usually C&DH is 8 or 16-bit MCUs, the "ARMs" are actually reduced capability Thumb™ processors**
  - **AAUSat-3, CANX-2 used a 32-bit ARM processor**
  - **Phonesat … flew … phones (and newer iterations are flying more)**
- **Expect that as CubeSat programs continue, need for more processing will be important**
- **Key drivers – same as for CubeSats in general**
  - **Small, low power, cheap**
  - **Generally accessible to low-budget environments (schools, R&D, etc.)**

Snapdragon/Atom Effort

- We focused on cell phone processors – primary player is ARM, with Intel trying to get Atom into play
- Avoid issues with closed architecture – i.e. not using Apple A6/A7/etc. (This is still an issue with ARM.)
- Most common phone processor in high-end devices is Snapdragon, with Krait CPU (similar to ARM Cortex A15)
  - We are currently looking at Snapdragon 600 and Snapdragon 800 (both TSMC 28 nm – low power)
  - Prototyping equipment readily available
  - Being used in the hobby space
  - These devices are in high production ~18 months

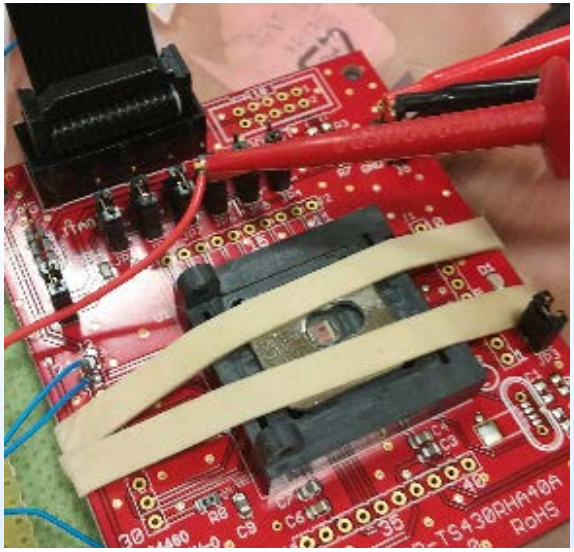
Collaborations

- **FPGA and Microprocessor Mitigation Working Group – Los Alamos National Lab – H. Quinn**
  - **Working to establish benchmarks:**
  - **compare effectiveness of mitigation**
  - **compare radiation hard to regular devices**
  - **general SEE sensitivity is secondary**
- **Intel device SEE evaluation with NAVSEA Crane**
  - **Working with Adam Duncan**
  - **See Austin's talk (yesterday) – Info on crash and cache parity on Atom E3825**
  - **Crane has evaluated a couple methods for testing SEE performance of Atom devices**
    - **using this information to target our testing better**
    - **This has been a bit harder than anticipated**

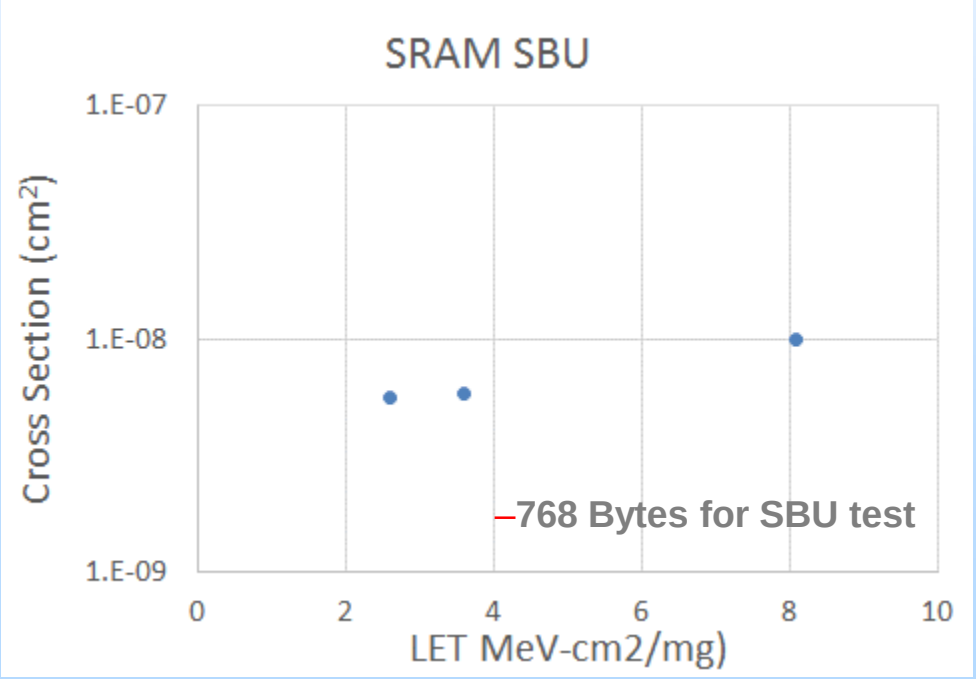
MSP 430 Overview

- **Originally identified through CubeSat kits:**
  - **MSP430F1611, MSP430F1612, and MSP430F1618**
  - **SEL testing performed on 1611 and 1612 – both devices show SEL, and 1618 is expected to as well (more later)**
  - **Limited SEE testing performed (SEL was primary focus)**
  - **TID testing performed on 1611 and 1612 – both showed problems between 10 and 20 krad.**
    - **Our devices primarily failed because they could not be reprogrammed with our suite of test software.**
    - **Results may be different if we don't reprogram the DUT – test pending**
- **Have also added MSP430FR5739**
  - **FRAM (expected to have better TID performance)**
  - **Epi (expected to have better SEL performance)**
  - **Has been tested for SEL and limited SEE**

SEE/SEL performance of MSP430FR5739

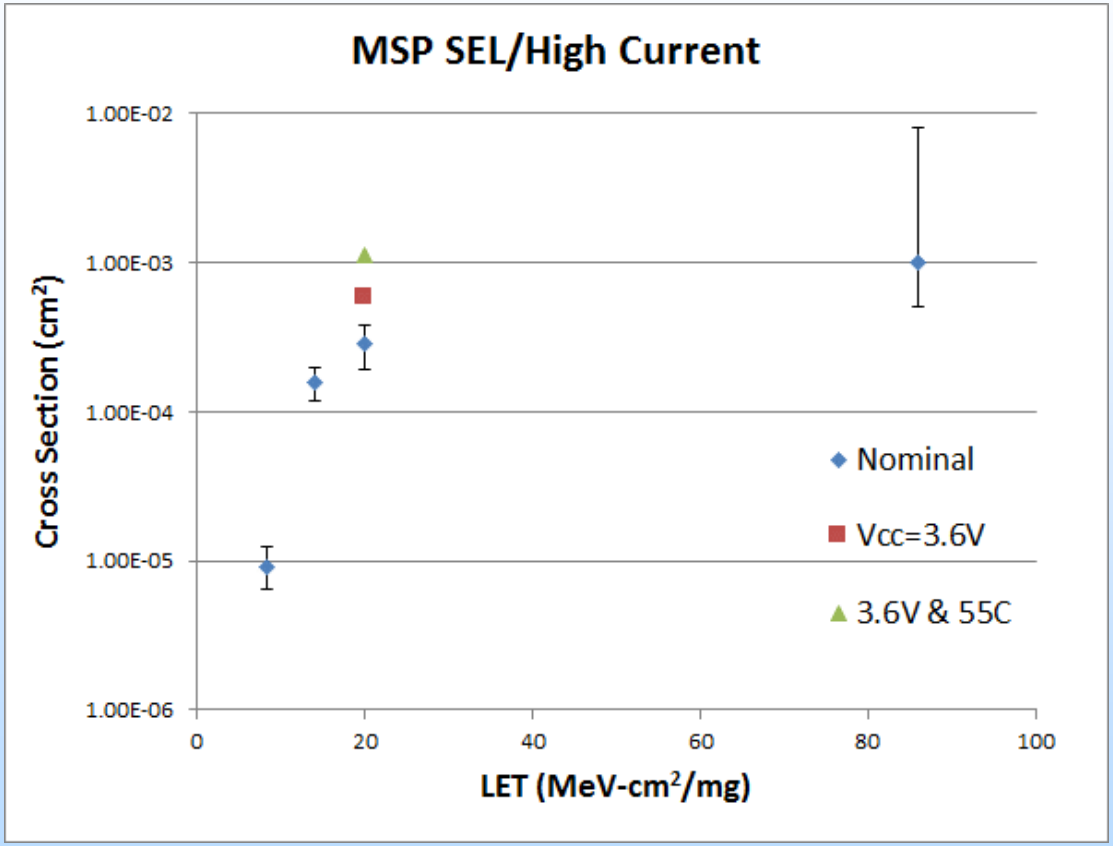


- Testing performed at TAMU on 6/18
- No SEL was observed
  - Exposed to $2x10^6/cm^2$ Au at 86 MeV-cm^2/mg
  - Tested at 3.6V and 85C (both max)
    - 85C took out the UART
- We did observe permanent damage
  - ~$1x10^{-5}cm^2$ at LET 86 – event not seen with $1.5x10^6$ at LET 8.1
  - Device does not function
  - Cannot be reprogrammed ("Inconsistent configuration information, discard unit and replace")



SEL/SEE Results – MSP430 – 1611 and 1612

- **SEL Characterization**
  - **0.05 A threshold**
  - **LET_{TH}~8 MeV-cm²/mg**
  - **Large σ by LET 20**
- **Not recovered by reset**
- **At about 1x10⁶/cm² (@ LET 86) test devices unprogrammable**



- **Error bars (nominal only) ~2σ,**
- **and include beam uncertainty**

TID Testing of MSP 1611 & 1612

- **Test procedure: between irradiation, tested with characterization programs – requires being able to reprogram devices:**
  - **LED blinker**
  - **Flash memory test program (provided in MSP development kit)**
  - **Whetstone test program**
- **Test steps: 1, 2, 5, 10, and 20 krad(Si)**
- **Unbiased devices showed no degradation at 20 krad**
- **Some biased 1611 devices became unstable at 10 krad**
  - **some devices failed to be reprogrammable at 20k, but instead seemed to be running the TID test program (LED blinking)**
- **Upcoming test pending to perform TID testing without reprogramming.**

PIC Overview

- PIC24 and dsPIC 33 devices have been tested for SEL, SEE, and TID
- Devices generally show relatively high SEL rate (about 10x higher than MSP430F1611)
  - No indication of damage
- TID performance (biased) is around 10krad(Si) with failures due to inability to reprogram.
  - Again, results may be different if we don't require reprogramming

PIC TID

- Performed unbiased testing of PIC24 and both biased and unbiased testing of dsPIC33
- Between irradiation, tested with characterization programs – requires being able to reprogram devices:
  - Flash memory test program (provided in MSP development kit)
  - Whetstone test program
  - SRAM test program
- Test steps: 1, 2, 5, 10, 15, 20 and 50 krad(Si)
- Unbiased devices failed at 20-50 krad(Si) – Failures due to inability to reprogram for post-rad evaluation.
- During biased testing, 2 out of 3 DUTs failed to reprogram at 10 krad(Si)
- Upcoming test pending to perform TID testing without reprogramming (address same problem as MSP).
  - And remaining biased TID test of PIC24 is planned.

SEE Testing – AT91SAM9G20

- **AT91SAM9G20-EK**
- **Bypassed regulators and provided power directly to DUT**
- **Test programs**
  - **Debug tools – direct OCM access**
  - **OCM write/read**

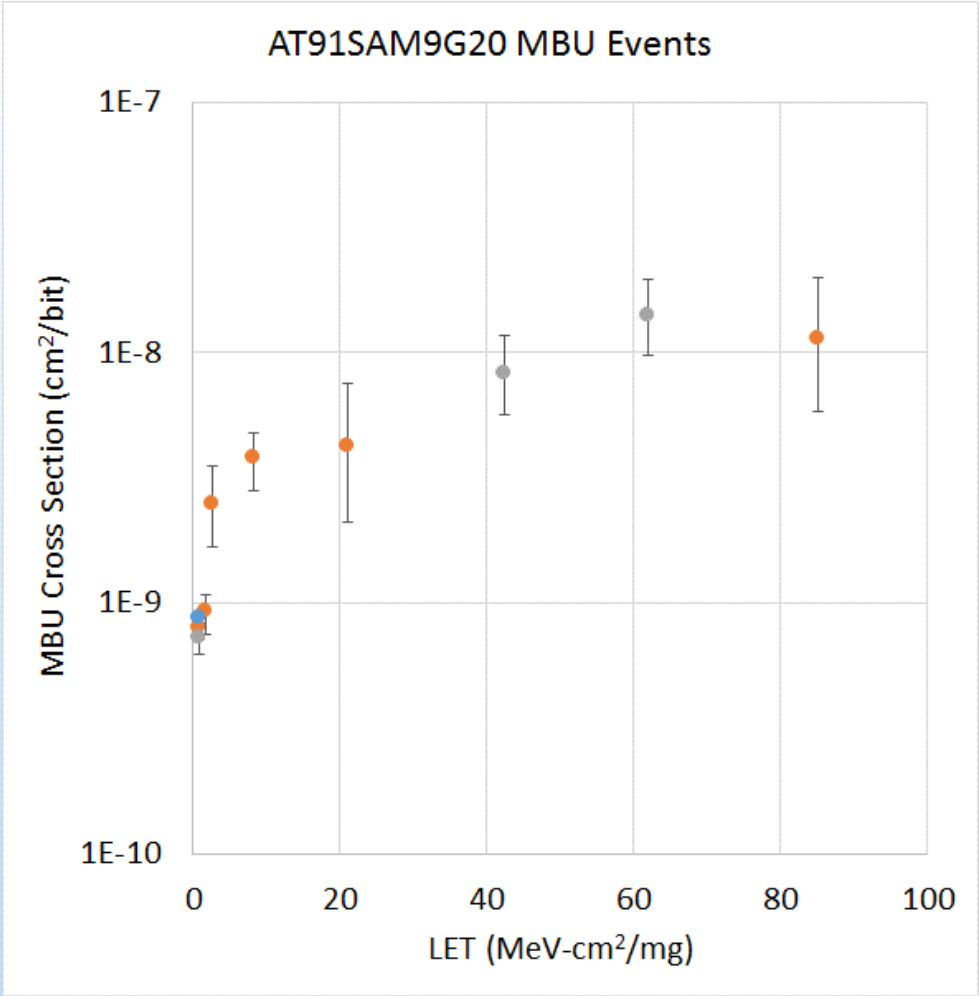
AT91SAM9G20 SEL/SEE

- **SEL monitored on 1V and 3.3V lines (limited at 200 and 300mA, respectively).**
  - **No significant changes (i.e. >20%) ever observed across all testing, tests performed at 85°C**
  - **No SEL (>1x10^{7}/cm^{2} at LET 86 MeV-cm^{2}/mg)**

- **Observed reset/restart of processor – these appear to always be functional (i.e. device communicates with debugger)**
  - **Observed crashes and resets with live code**
  - **Live code and debugging setup produce similar measurements**
  - **Reset did not always result in reliably running code without power cycle (may have cause lock up during reboot)**

AT91SAM9G20 SBU/MBU

- **Observed upsets in the on chip memory (OCM) – with MBUs being obvious, but not in the same data word**
  - **Multiplicity of 1.1, 1.5, and about 5, at LET 2.3, 8.3, and 85, respectively.**



Intel Atom E620

- Test Approaches considered
  - Operating system crash rate
  - Scan chain/register error rate
  - Cache bit sensitivity
- Focus has been on cache bit sensitivity
  - This is expected to enable worst case predictions for system errors
  - Can be compared to operating system crash rate easily, though our test operating system does not correlate to a flight-like system
- Capturing cache bit sensitivity has been elusive
  - Test system has been based video output
  - Have verified:
    - simple machine check handler does not report cache errors
    - machine check status register report not visible before crash
    - - exploring improved machine check handler
- SEE Summary:
  - Verified no SEL, measured crash cross section for minimal test code

Conga Test Board/Approach

- **Test System**
  - **Conga QA6/E620 processor cards**
  - **Mounted in a Conga MCB/Qseven board**
- **Processor is easily thinned (we have two at ~80 um)**
- **But board does not support UART**
  - **Problem for debug efforts**

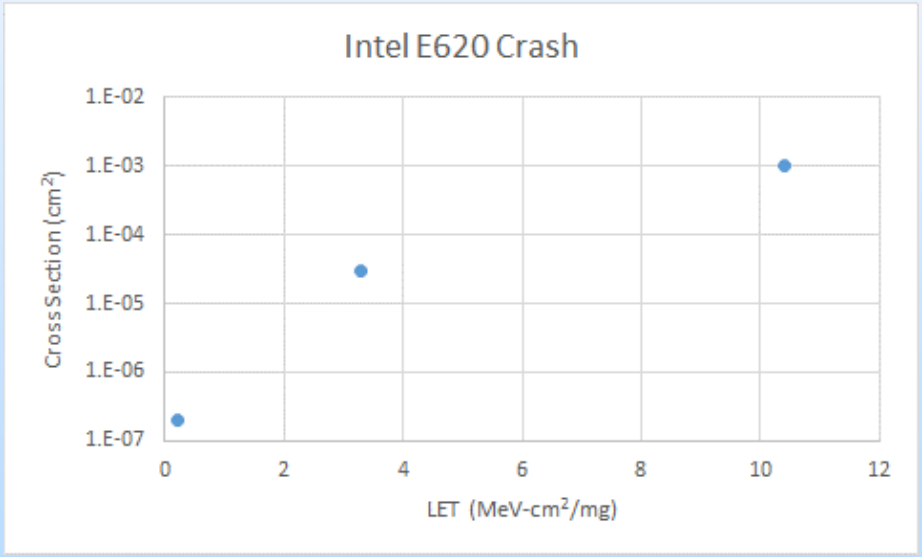
Test Software Effort – E620

- Working on approach using boot-loader (GRUB) to place custom code.
  - Custom code, using inline assembly and a limited amount of the c-code base for GRUB
- Have level 0 privilege
- Have been able to reroute exception handlers
- Have been able to read the Machine Check Status registers and clear them
- Our test board does not provide UART, so only IO thus far is keyboard & screen (working on this)

- Also working other approaches with collaborators

E620 SEE Test Results

- **No SEL with effective LET of ~75 MeV-cm^2/mg (room temperature, with >1x10^7/cm^2)**
- **Have observed crashes when testing with a couple beams**
  - **Have established functionality of primary approach, but thus far testing has only shown crashes/resets.**



  - **Also tested by just going to BIOS screen.**
    - **Cross section for lockup in BIOS: ~<1x10^{-4}cm^2 LET 30 MeV-cm^2/mg**

E620 SEE Test Concepts/Efforts/Results

- **Cache Testing**
  - Caches are nominally operated in write-back mode
  - Have operated write-dwell-read of caches
  - No upsets observed in cache testing (just crashes)
- **Machine Check Handling**
  - Have implemented the machine check exception
  - If machine check taken, code is restarted with a flag set to report the machine check
  - No machine checks observed
  - Machine checks for SEE upset modes may not be enabled
- **Machine Check Reporting Registers**
  - Tried polling of these registers
  - Unfortunately our test system has yet to report these before crashing – still working

Snapdragon APQ8064 Overview

- Using IFC6410 board
- Test Approaches considered
  - Operating system crash rate – takes too long to boot
  - On-chip memory test
- Has been very difficult to obtain data on how to operate
  - Best material seems to be source code for open source OS
- On-chip memory test
  - We think the device has between 4 and 64kB of on chip memory
  - Trying to verify we have the right physical address… this work is on-going
  - We do have working control of the UART and can run more general codes
- Interesting tid-bit: the APQ8064 has an ARM7 helper processor that is part of the boot sequence
- SEE Summary:
  - Have verified no SEL, and have observed exceptions during Android boot (leading to restart and/or crash)
  - (WiFi only chip)

Future Work

- **We are continuing test development on Atom and ARM device types**
  - **Have viable approach for inserting test code**
  - **May need to target different Atom board due to lack of UART**
  - **Video on Atom comes direct from part – may be a cause of crash**

- **Planned Tests**
  - **TID test of MSP devices without reloading of test code**
  - **TID test of MSP430FR5379**
  - **TID of ATM91SAM9G20**
  - **SEE test of Intel Atom E620 (targeting cache performance)**
  - **SEE test of Qualcomm APQ8064 (targeting on-chip RAM and/or caches)**

Conclusion

- NEPP is moving forward to identify current and potential future microcontrollers an microprocessors
  - Developing SEE and TID data to support various missions
  - Creating a basis of device response data for different families of devices
- Have tested several different devices to date
  - TID and SEE on TI MSP430 – older 1611/12/18; and newer devices like FRAM/Epi MSP43FR5739
  - TID and SEE on PIC24 and dsPIC33
  - SEE testing on AT91SAM9G20
  - SEL and very limited SEE testing of Intel E620 and Qualcomm APQ8064
- Several tests coming up – building general data around various architectures AT91SAM9G20 TID; more PIC TID, and SEE tests of Intel E620 and Qualcomm APQ8064
- Data workshop at NSREC in Boston 2015

End

Cubesat Controller Survey

- **Reviewed many Cubesat system architectures**
  - **Primary devices on this list: MSP430F1611, 1612, 1618; PIC24, dsPIC33; AT91SAM9G20; ATMEGA1281; C8051; AT91SAM7**

CubeSat Provider	Processor	Availability	Development Board
Pumpkin	TI MSP430F1612	Yes	Yes
	TI MSP430F1611	Yes	Yes
	TI MSP430F1618	No	No
	Silicon Labs C8051F120	Yes	Yes
	Microchip PIC24FJ256GA110	Yes	Yes
	Microchip dsPIC33FJ256GP710	Yes	Yes
Tyvak (Intrepid)	AT91SAM9G20 (ATMEL, ARM9 Based)	Yes	Yes

CubeSat Provider	Processor	Availability	Development Board
GOMspace (NanoMind)	AT91SAM7 series (ATMEL, ARM7 Based)	Unknown	Unknown
	ATMEL ATMEGA1281	Yes	Unknown
Gaussteam (ABACUS)	TI MSP430 series	Yes	Yes
ESL/ISIS (Cube Computer)	ARM Cortex-M3 MCU	Unknown	Unknown
ISIS (OBC)	AT91SAM9G20 (ATMEL, ARM9 Based)	Yes	Yes
Clyde Space	Use Pumpkin CubeSat OBC	Yes	Yes

Microcontrollers from NEPP Review

- Atmel Microcontrollers
  - ATMEGA164P
  - ATMEGA32U4-(MU,RC-MU,RC-AU), ATMEGA328P(-PU), ATMEGA16U2
  - ATMEGA2560
  - Other ARM9?

- TI MSP430 16-bit Microcontroller
  - MSP430F2619, MSP430FR5739
- TI Other
  - OMAP3503/ARM Cortex-A8 (TI Sitara AM3505)
  - TI Sitara AM3703

- Microchip 32-bit Flash & Non-Flash Microcontroller
- Stamp9G20 processor
- ColibriPXA270 (Intel/Marvel ARM PXA270)

- Others:
  - Parallax PX32A

A Packaging Example

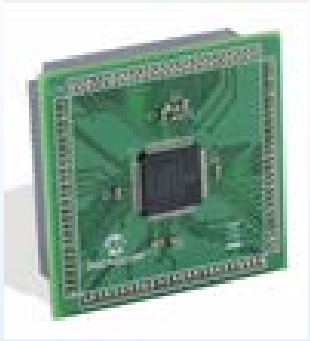
- **We are finding some significant problems with some test boards, in terms of preparation for test…**

A Packaging Example

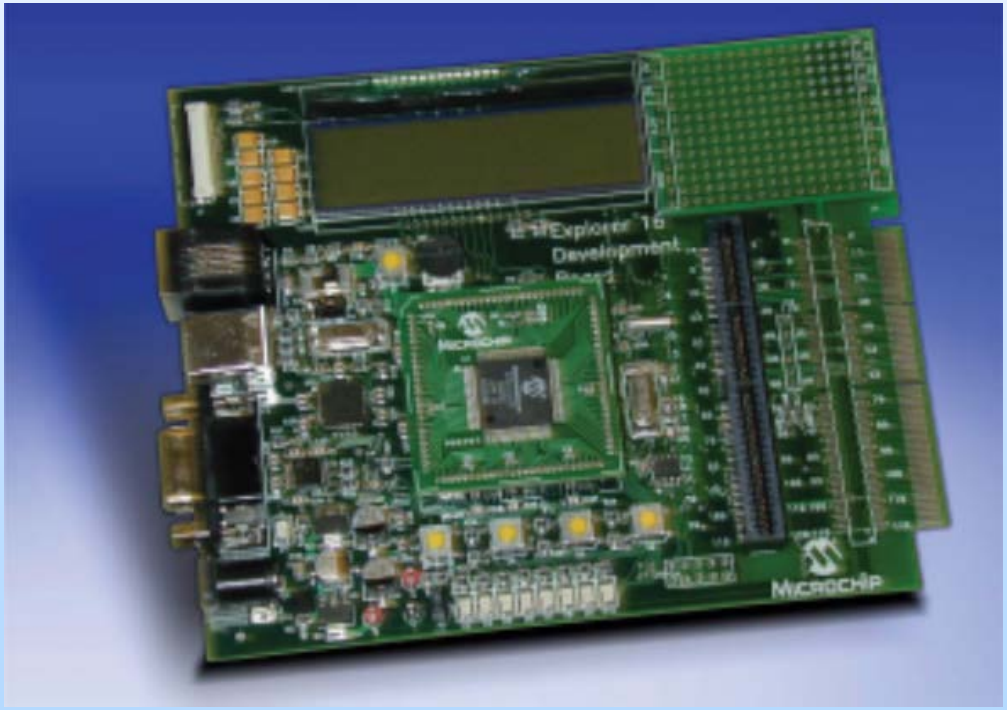
- We are finding some significant problems with some test boards, in terms of preparation for test…
- We're also seeing this with TI Sitara eval kits

SEE Testing – PIC

- Used Explorer 16 board from Microchip
- Test Devices:
  - PIC24FJ256GA110
  - dsPIC33FJ256GP710
- Using on-board regulators
- Two test programs
  - RAM write/read
  - Flash read/dwell

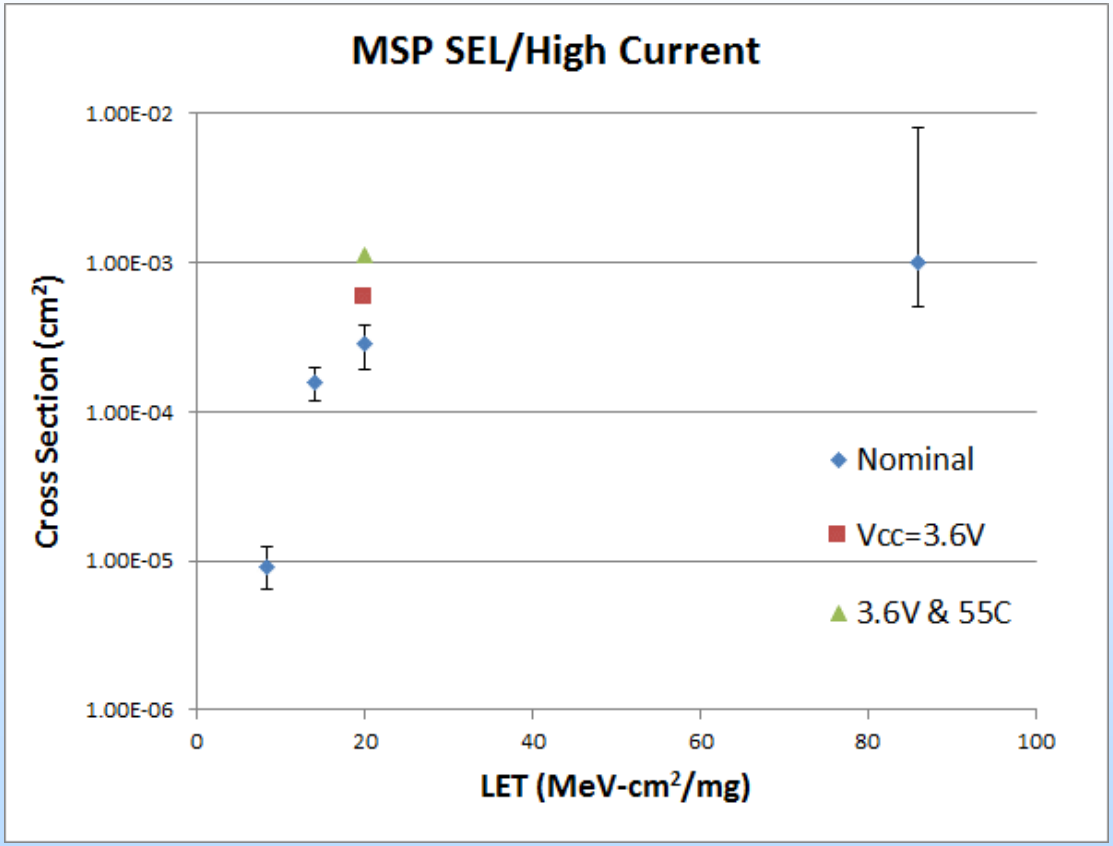


–Plug-In-Module
– - PIC24
– - dsPIC33



SEL/SEE Results – MSP430 – 1611 and 1612

- SEL Characterization
  - 0.05 A threshold
  - LET_{TH}~8 MeV-cm^2/mg
  - Large σ by LET 20
- Not recovered by reset
- ISS event rate estimated between $2x10^{-5}$ and $4x10^{-4}$/day
  - ~10x higher for GCR
- SRAM SBU (limited eval)
  - σ~$4x10^{-8}$cm^2/bit @ LET 20 MeV-cm^2/mg
  - Testing 2048 bytes



- Error bars (nominal only) ~2σ,
- and include beam uncertainty

SEL in APQ8064

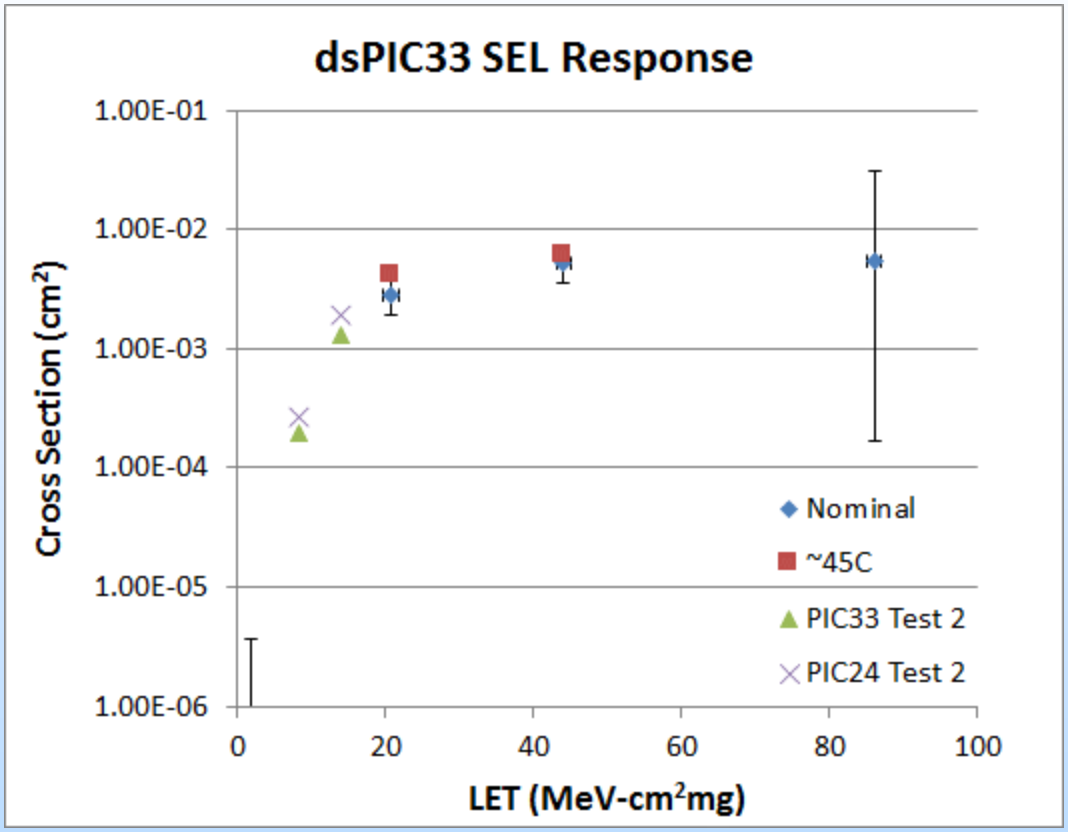
- Thinned parts to 80 μm
- Tested at TAMU with 25 MeV/amu Kr
  - 60° Tilt – LET_{eff} = 57 & 75 (at sensitive region)
  - 3e7 exposure at LET 57, 4e7 exposure at LET 75
- Tested during booting of Android
  - Almost all SEL runs resulted in a "rebooting in 5 seconds" – but reboot never succeeded
  - Reset worked in 9 out of 10 runs – resulting in nominal operation (this rules out an SEL behavior).
- Board current @5.1V:
  - At start of run 330-350 mA
  - At end of run 160-500 mA (never above 350 for high exposure runs)
  - No significant increase

SEE Testing of Snapdragon

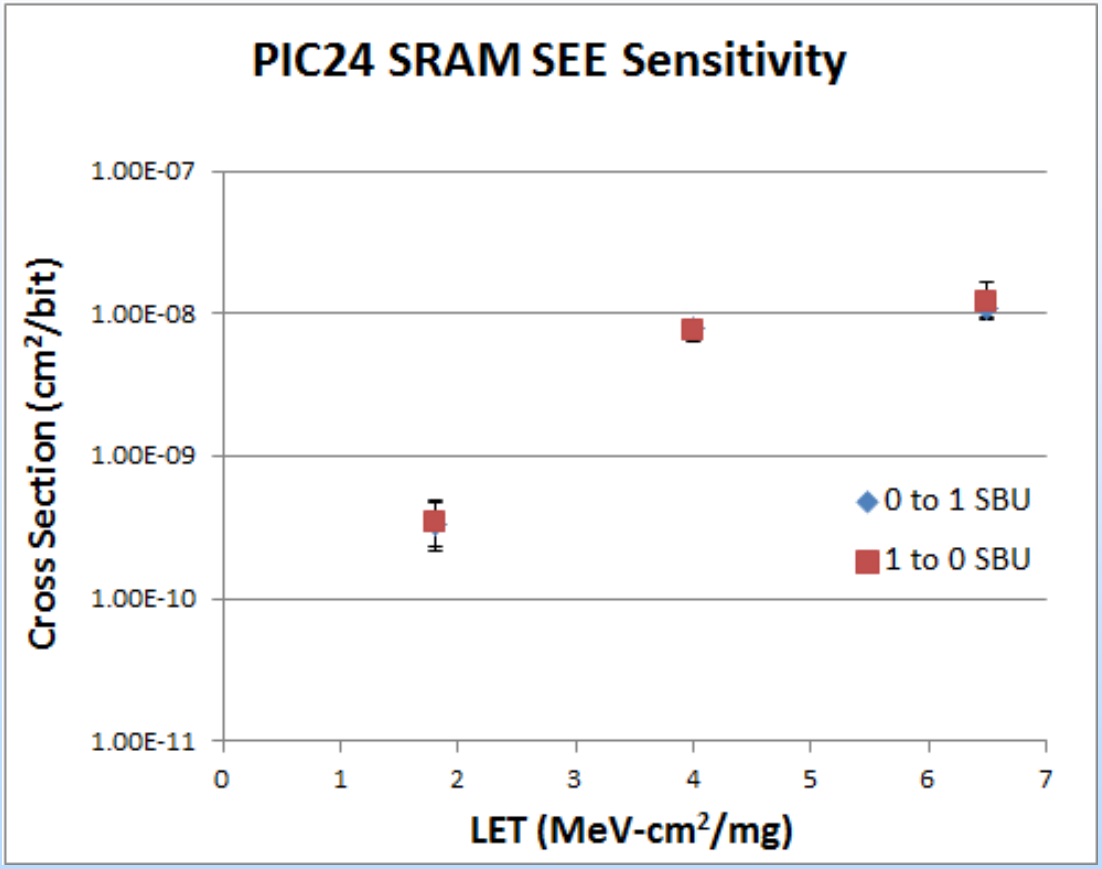
- Exposed IFC6410 board to Ar @ LET = 7 MeV-cm^2/mg
- Test software was to monitor Android boot
  - Observed through UART error output
  - Provides information about boot behavior for first ~90 seconds
  - Takes ~5 seconds after power up to be activated
  - Provides interrupt/exception reporting
- Total exposure was 3e6 #/cm^2
  - No damage observed
  - No evidence of high current modes (but LET was low)
  - But system had a hard time, and crashed often

SEL Cross Section

- Used 0.25 A as threshold for SEL
- When heated, the SEL current trips on-board regulation
- Both points (slightly) higher σ for high T
- ISS event rate estimated between $2x10^{-4}$ and $4x10^{-3}$/day
  - ~10x higher for GCR
- dsPIC33 and PIC24 devices very similar



PIC SEE Results



- **Flash Results**
  - **No upsets observed with $6x10^5$ /cm^2 ions at LET = 86**
  - **Limiting cross section of ~$6x10^{-12}$ cm^2/bit**
- **SRAM Results**
  - **SEL behavior interfered at higher LETs**