Jet Propulsion Laboratory
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A Good Idea That Didn't Pan Out – Single Event Test Results of Altera MAX10

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To be presented by Gregory R. Allen at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 13-16, 2016 and published on nepp.nasa.gov.

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Altera MAX10 FPGA Task Overview

- **Task Description—perform initial SEL and TID characterization of Altera's CPLD Based MAX10 FPGA.**

- **General Test strategies based on *Field Programmable Gate Array (FPGA) Single Event Effect (SEE) Radiation Testing* [Berg, 2012], and *SoC SEE Test Guideline Development* [Guertin].**

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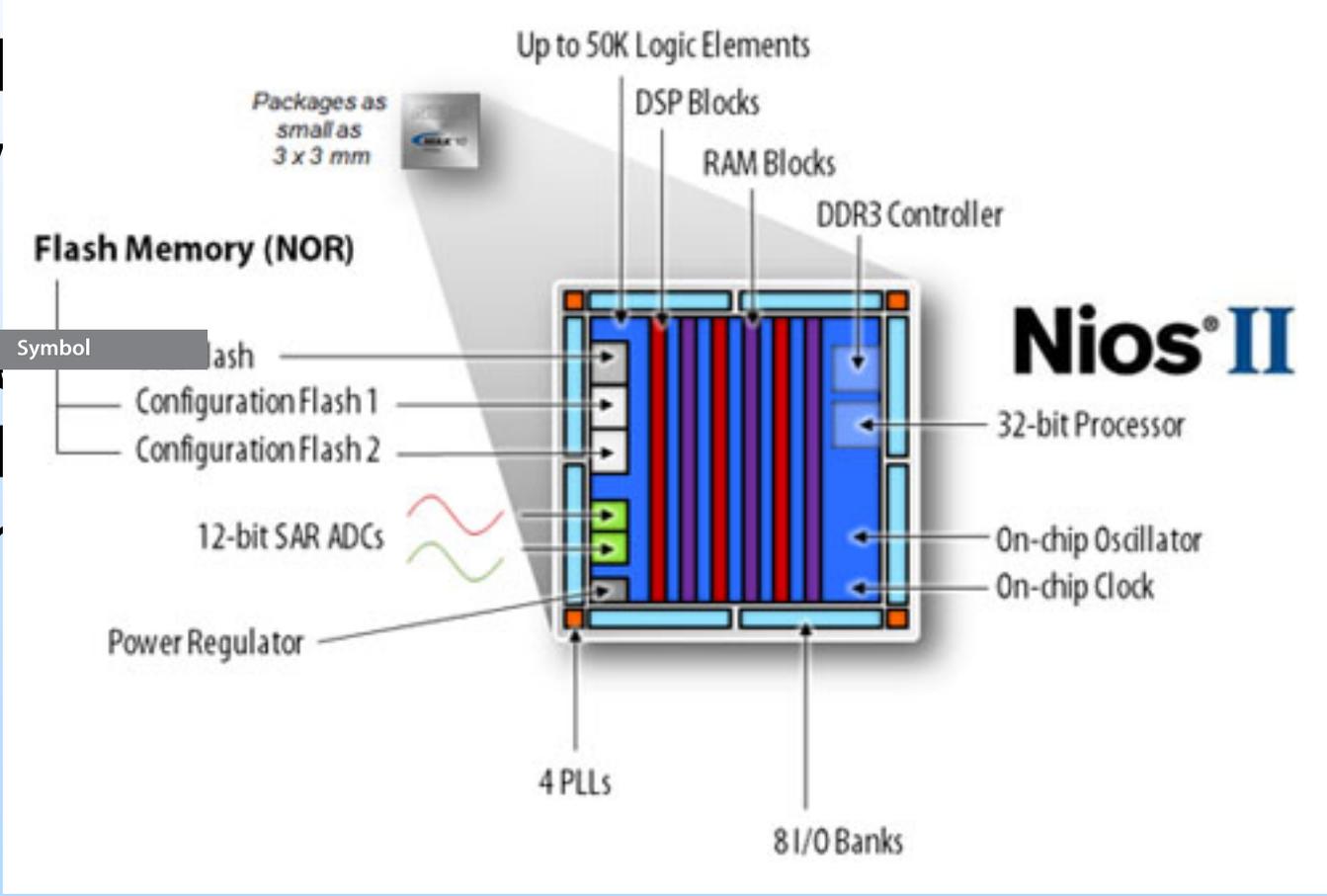
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Altera MAX10 Architecture Overview

- **Flash-based/SRAM-based FPGA based on TSM**
- **1.2V devi**
- **Have flash, 18x1 mem**

Packages as small as 3 x 3 mm

Flash Memory (NOR)

- Symbol lash
- Configuration Flash 1
- Configuration Flash 2
- 12-bit SAR ADCs
- Power Regulator
- 4 PLLs

Up to 50K Logic Elements
DSP Blocks
RAM Blocks
DDR3 Controller

Nios® II
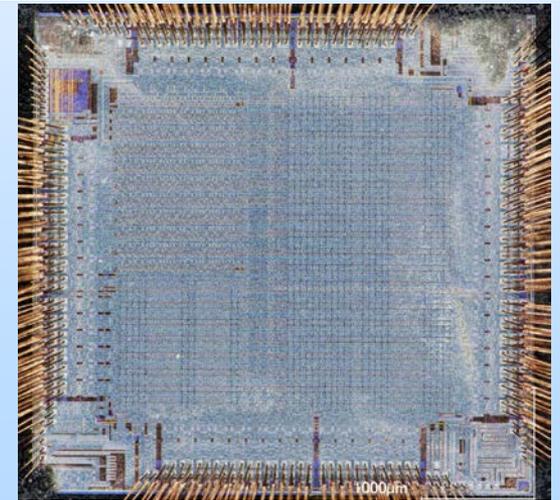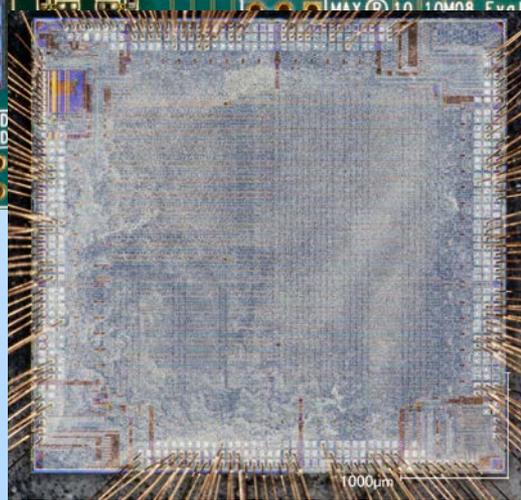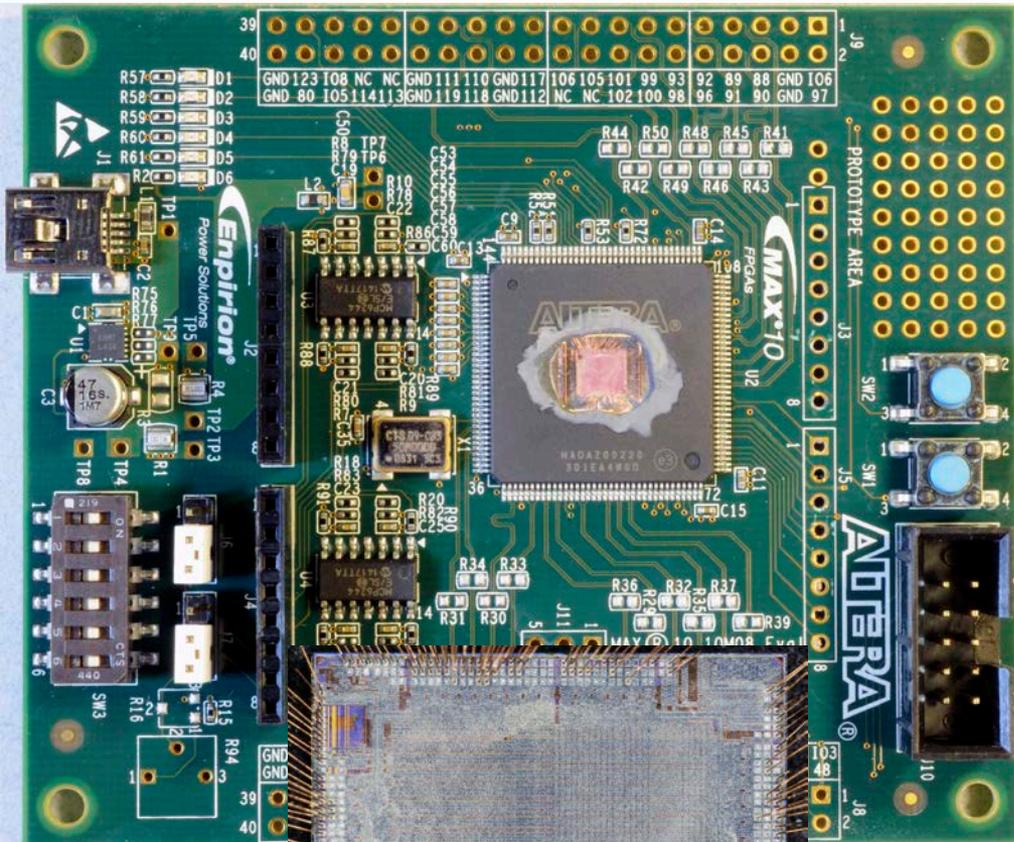
32-bit Processor
On-chip Oscillator
On-chip Clock

8 I/O Banks

FY16 Major Accomplishments-MAX10

- **Performed SEL characterization test on MAX10 devices**

# Test Boards

TID Test Plan

- **Phase 1 Test (Completed)**
  - **Initial test structures:**
    - **Simple shift register with combinatorial logic**
    - **Inverter chain**
  - **Single Supply (*VCC_ONE)***
  - **Biased, no-refresh mode**
- **Phase 2 Test (Cancelled due to SEL results)**
  - **Full processor implementation, ADC, PLL, etc.**
  - **Both FPGA types to be tested (single and dual supply).**
  - **Initially biased only, using both program refresh mode and no-refresh mode.**

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Initial TID Results (FY15)

- **Tested at Co-60 facility at JPL.**

- **Tested MAX10 VCC_ONE device at 25 rad(Si)/second, biased, no-refresh.**

- **No timing degradation observed. Functional failure between 100 and 150 krad(Si).**
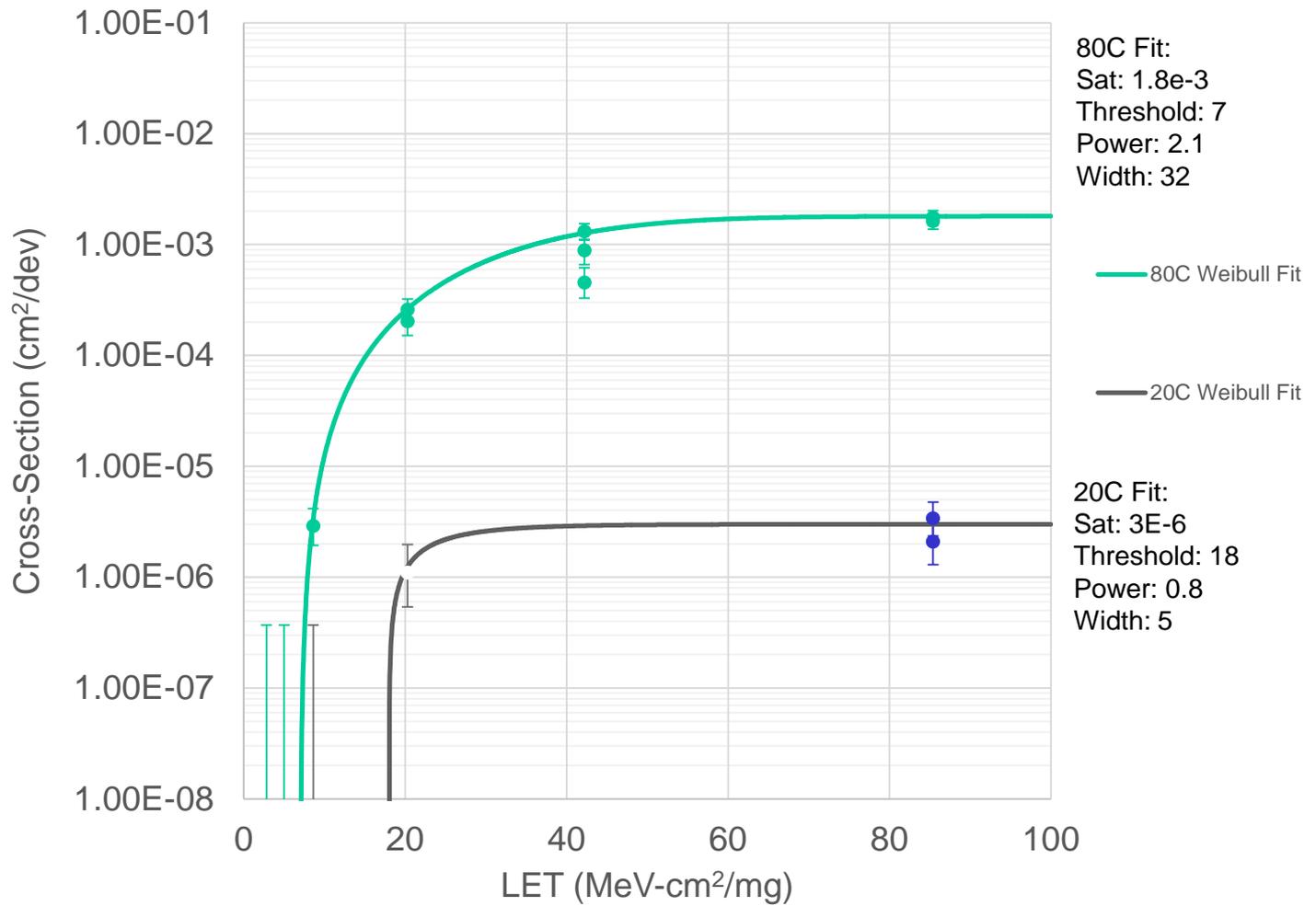
ICC_ONE vs. TID
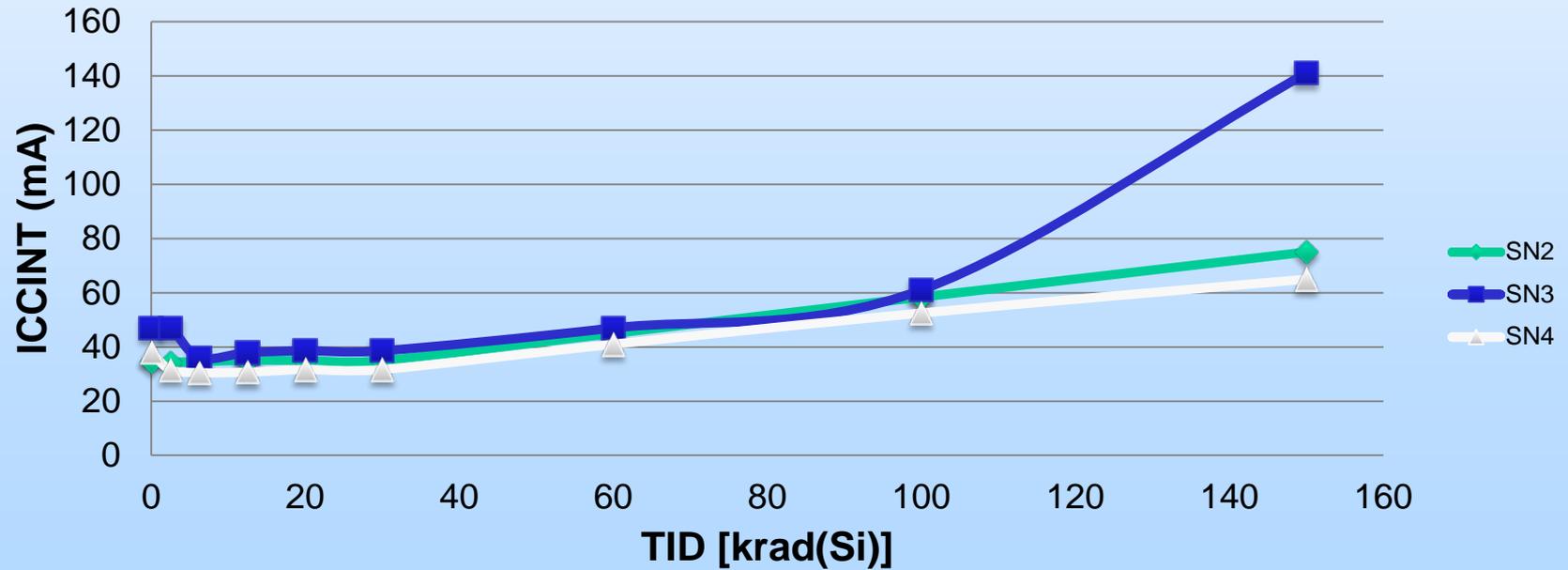
SEL Test Plan

- **Basic SEL test (6 devices, three of each supply type), worst-case datasheet bias and temperature, 1×10^7 ions/cm^2 per DUT or statistically significant events**

- **Simple functional design**

- **Regulators removed from evaluation board and power directly supplied**

- **Custom software used to monitor and strip chart power, and automatically power cycle in the event of an SEL**

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SEL Test Results

Altera MAX10 SEL Cross-Section vs. LET

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Representative SEL Rates
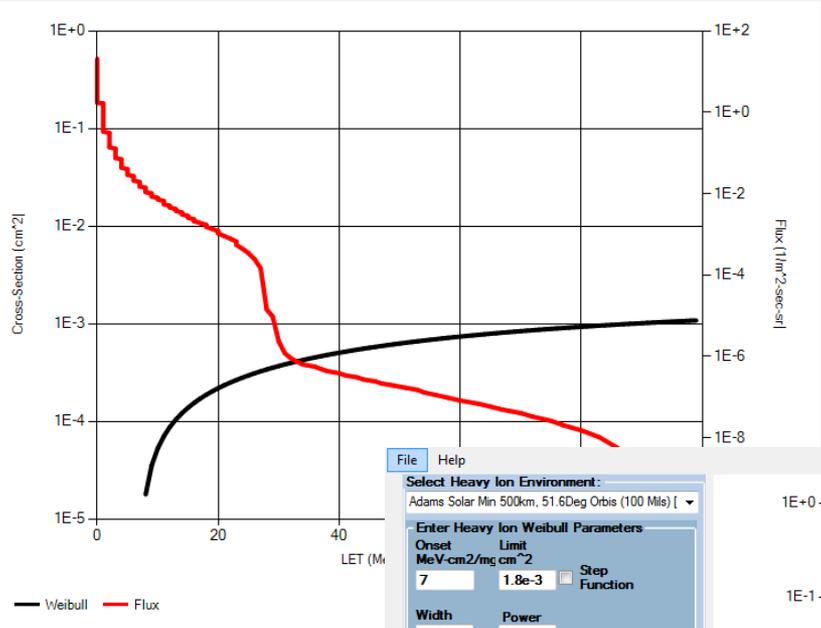
—*Deep Space: Solar Min, 100mils: 4.8E-4 SEL/dev-day @80C*

—*Deep Space: Solar Min, 100mils: 1.1e-6 SEL/dev-day @20C*

—*ISS, Solar Min, 100mils: 2.1E-5 SEL/dev-day @80C*

—*ISS Proton estimate: 8.5E-4 SEL/dev-day @80C*

—*ISS, Solar Min, 100mils: 3.8E-8 SEL/dev-day @20C*

—*ISS Proton estimate: 0.00 SEL/dev-day @20C*

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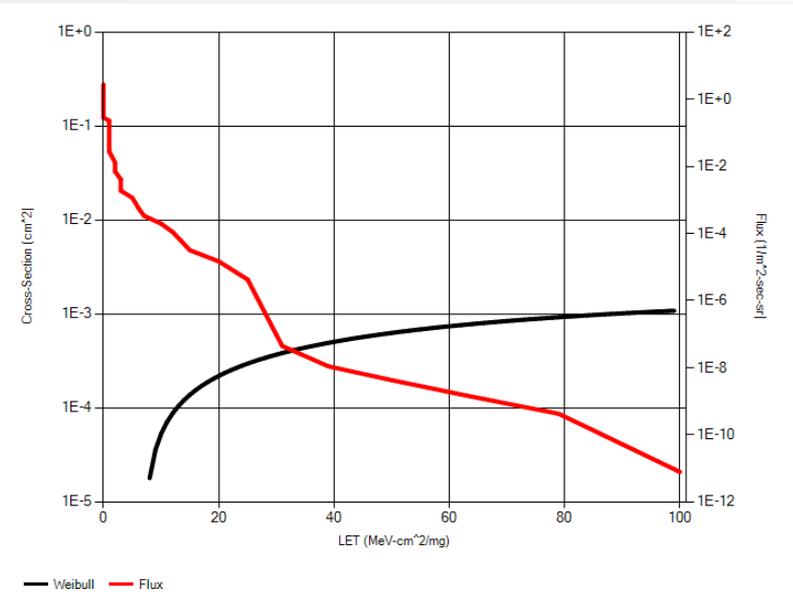
Other SEL Test Notables

- **SEL only occurred while in a configured state**
  - **e.g. if the DUT was held in an unconfigured state, the effect was not observed.**
  - **Indicates ADC unpowered during un-configured state**
- **With Au, the configuration was knocked out instantly and required reprogramming.**
- **With Ag and below, both devices maintained configuration**
- **Opened power supply clamps and SEL maintained ~1.1A**

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Conclusions

- **Lower budget missions (e.g. class D) will often select commercial devices**

- **Methodologies for determining baseline SEE/TID susceptibility can be scaled to mission budgets**

- **Altera MAX10 is susceptible to SEL and not recommended for use in space**