SUNY POLYTECHNIC INSTITUTE

New York Power Electronics Manufacturing Consortium:

Capabilities and SiC Electronics

Alexey Vert on behalf of NY-PEMC team

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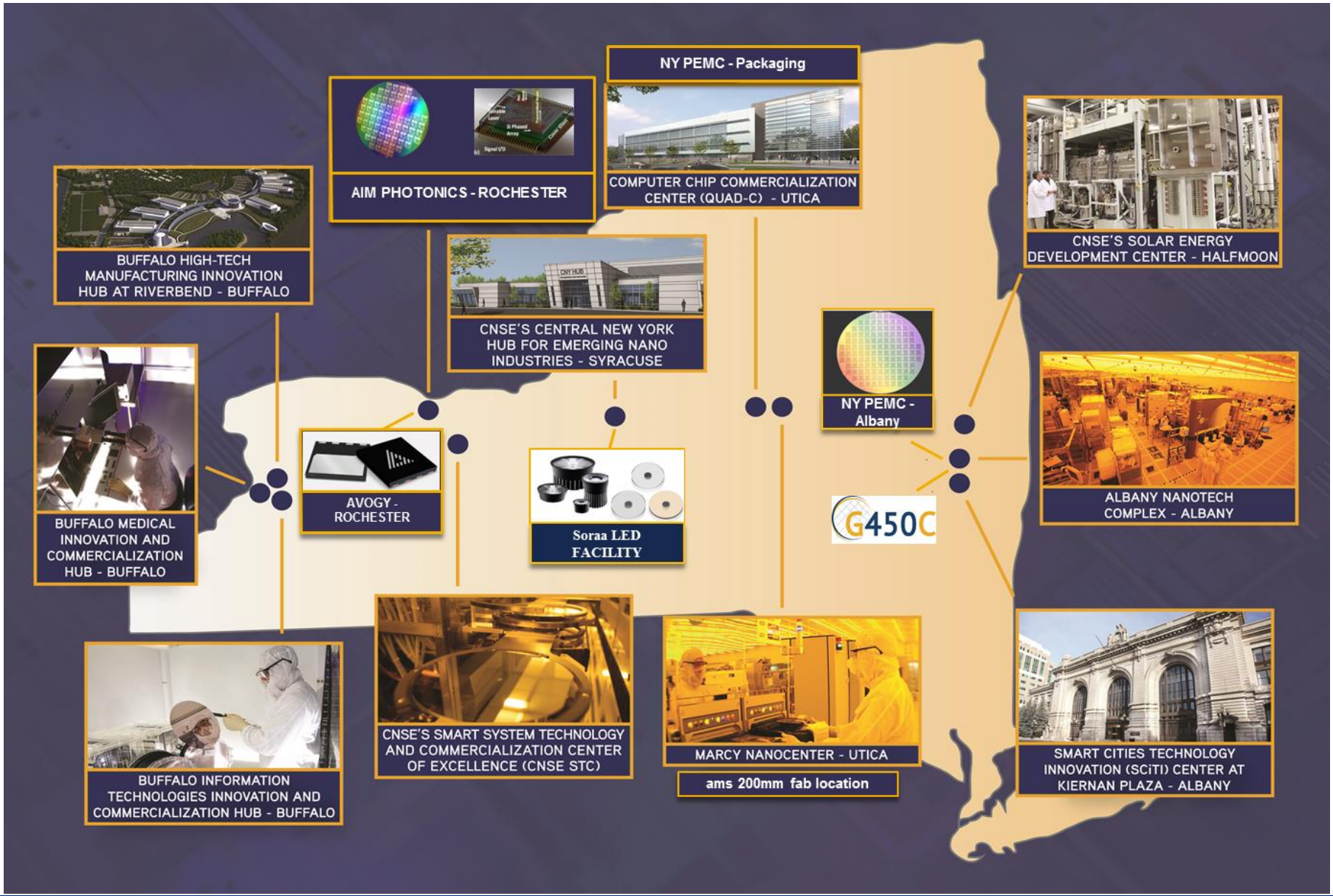
NASA Electronic Parts and Packaging (NEPP) Program
2016 Electronics Technology Workshop

NEW YORK POWER ELECTRONICS MANUFACTURING CONSORTIUM

Outline

- Technology and Manufacturing Innovation in NYS
- NY-PEMC Overview
- SiC Line Capabilities and Timeline
- SiC Materials and Devices
- Power Electronics Packaging
- Emerging SiC Electronics

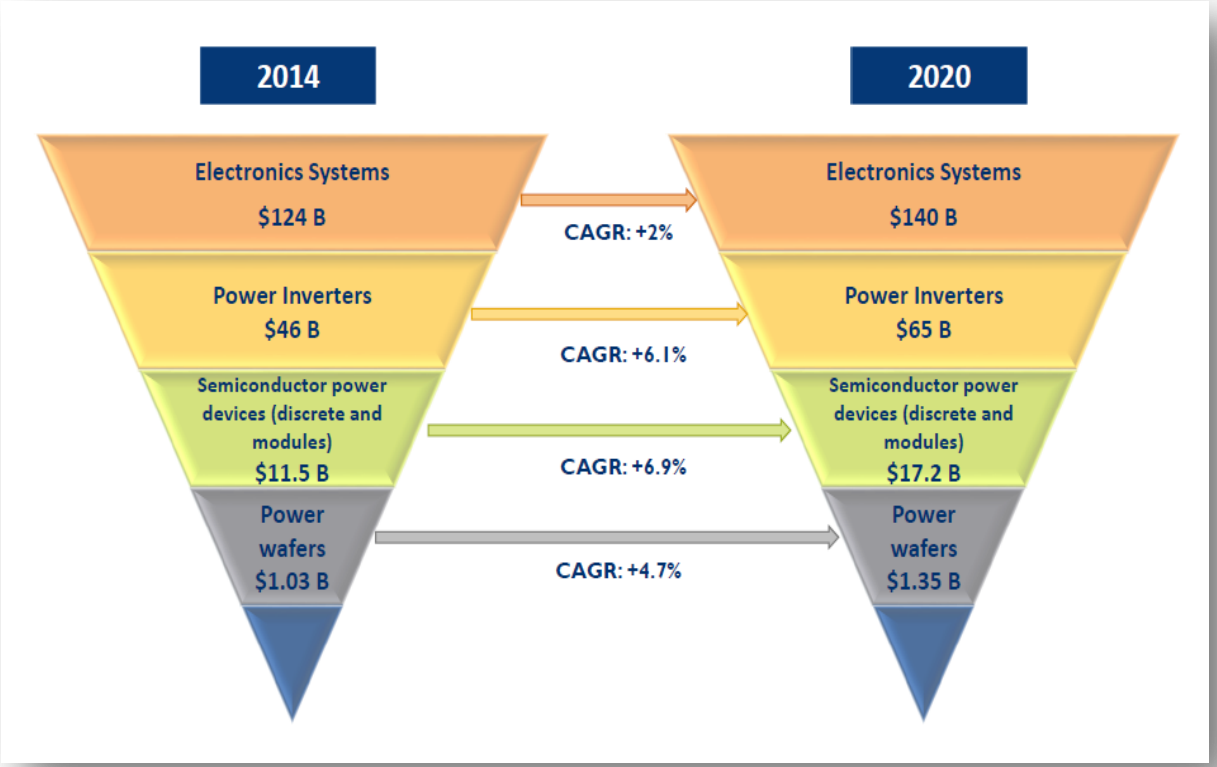
Innovation in NYS



SiC & Market Acceptance

- Despite over 20 years of R&D globally, SiC power devices' market penetration is limited
- Estimates from Yole Developpement marketing firm, include >$10B/yr for power devices, with WBG growing to an est. $1.4B in 2020
- Despite this potential, SiC market adoption was only about $130m in 2014*
- Key challenges:
  - Performance,
  - Reliability, and;
  - Cost

Power device and system market to 2020



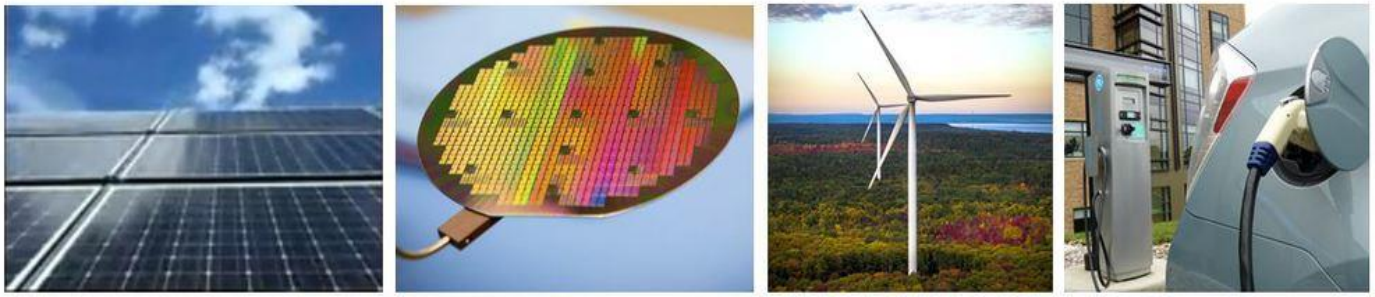
*Above figure and reference: Yole Développement reports from ISiCPEAW meetings (2014 & 2015)

New York Power Electronics Manufacturing Consortium (NY PEMC).

A public-private partnership producing the next generation of power electronics at SUNY Polytechnic Institute's 150mm SiC fab and world-class research and development resources to drive tremendous advances for businesses, the power electronics technology and academic communities.

- Membership:

Founding Member is General Electric



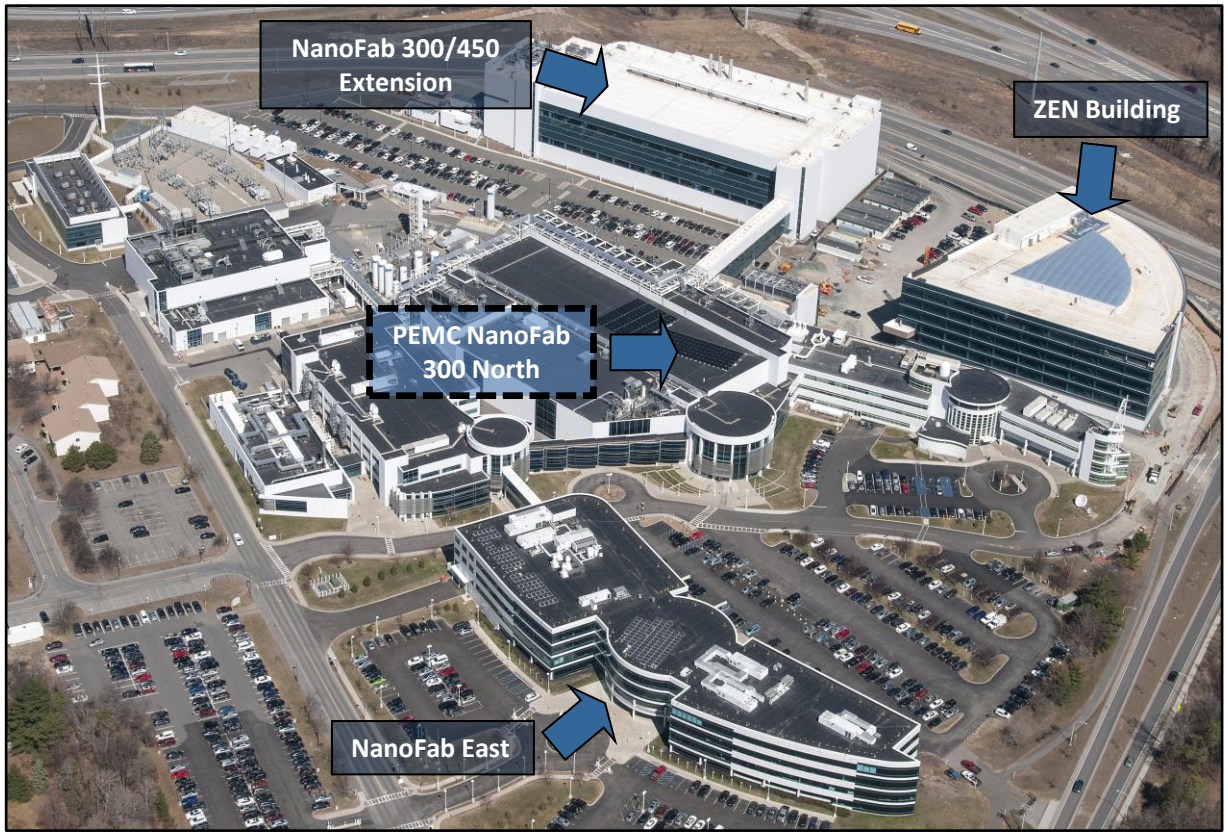
PEMC Capabilities

- 2 locations within SUNY Polytechnic Institute
  - SiC Wafer Fab: SUNY Poly Albany
  - Packaging: SUNY Poly Utica

- Types of activities under PEMC
  - Wafer production
    - 150mm SiC MOSFET and Diode
  - Packaging
    - Modules and power blocks for Industrial, Transportation and Aerospace applications
  - Foundry Services
  - R&D

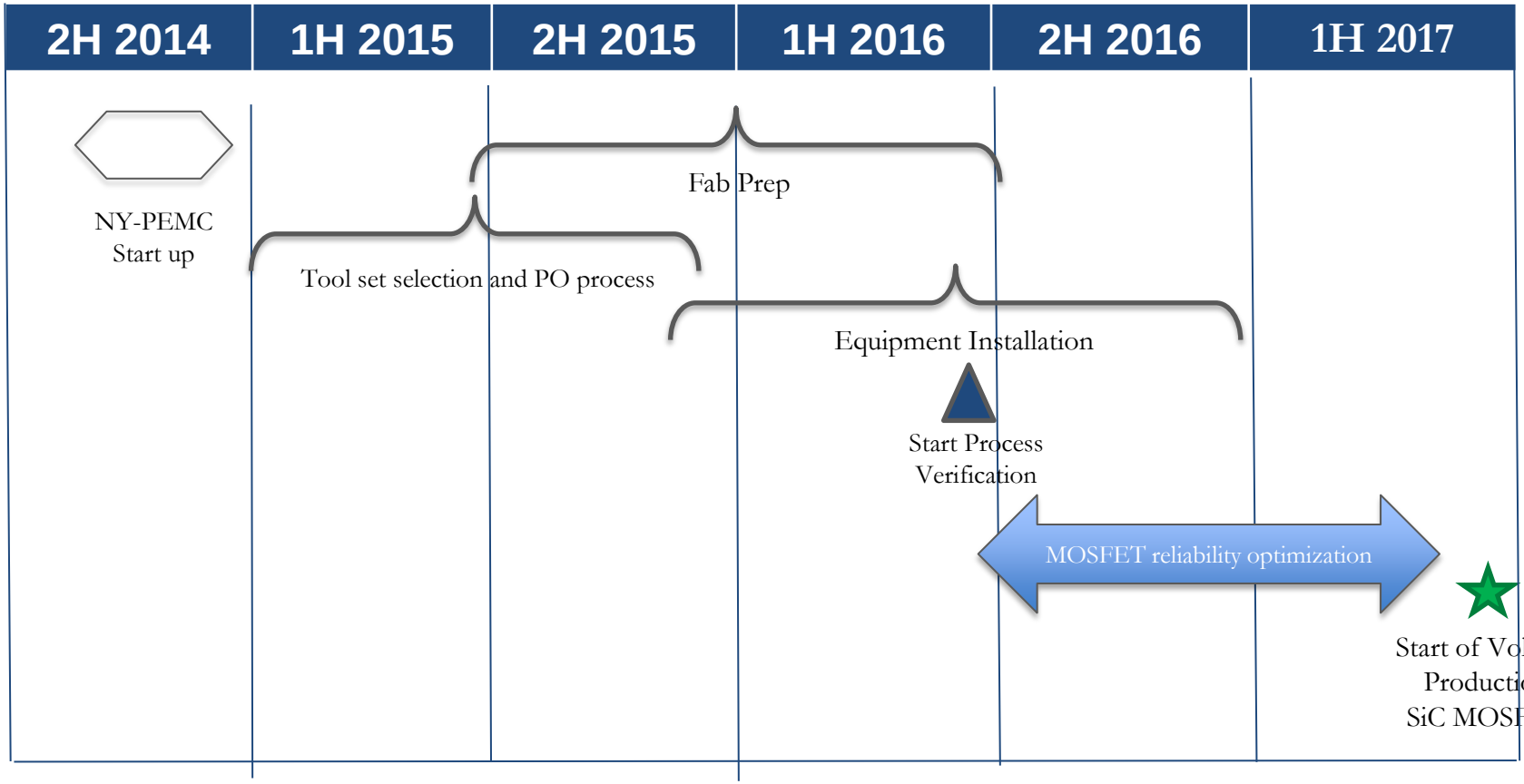
Phase 1 -- SiC wafer fab located at SUNY Poly Albany:

- Production capabilities yielding between ~10,000-15,000 wafers/year
- MOSFETs initially with Diodes added later
- Integrated team of SUNY Poly and GE engineers installing and running the Consortium's 6" SiC line
- Expected on-line by 2Q17



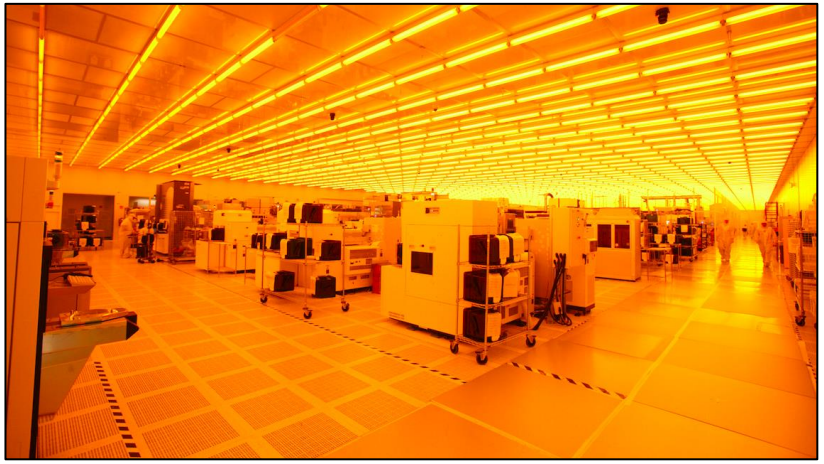
NY-PEMC SiC Timeline

NEW YORK POWER ELECTRONICS MANUFACTURING CONSORTIUM



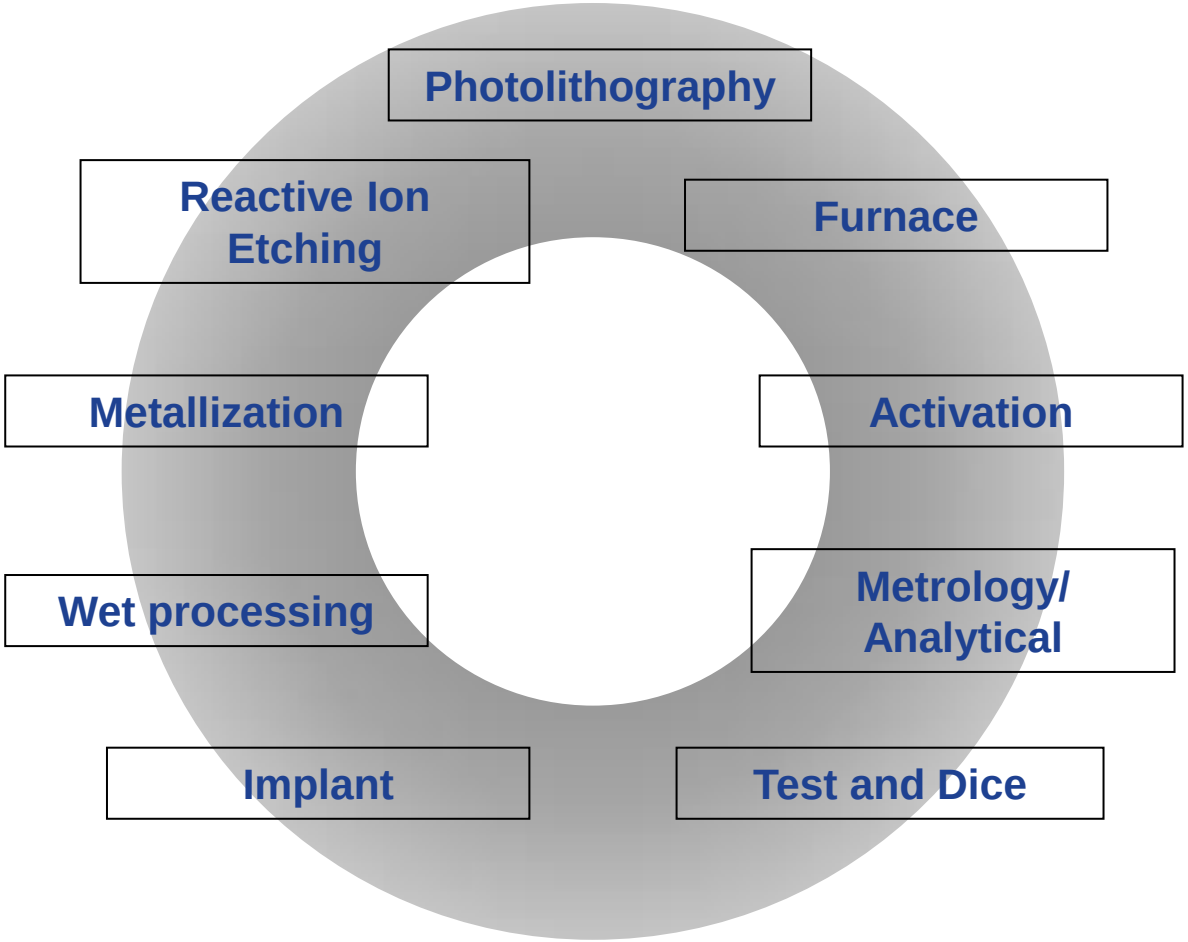
PEMC SiC Wafer Line:

- SiC dedicated 200mm tools capable of processing 150mm wafers
- Class 100 Cleanroom with proper ESD controls
- MES managed processing facility under ISO 9001 Quality system
- Full complement of metrology and analytical equipment



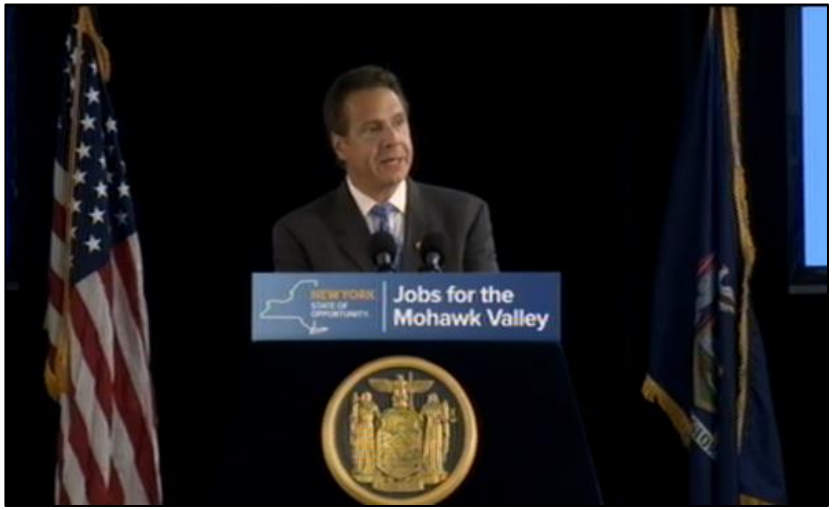
February, 2016

State-of-the-Art 6” SiC Facility



- Qualified 1.2kV MOSFET baseline SiC process capability
- Parametric Test and Dice capability

Power Electronics Packaging



- August 2015, Gov. Andrew Cuomo announced the expansion of the NY-PEMC which now includes packaging as part of the Consortium at Quad-C on the SUNY Polytechnic Institute campus

- GE and SUNY Poly expand their partnership in Power Electronics and include a packaging partner which will operate at the Quad C: Computer Chip Commercialization Center

Phase 2 -- SiC packaging fab located at SUNY Poly Utica:

- $70M investment for power electronics packaging
- Initial focus areas: industrial, transportation, aviation with automotive to follow
- R&D line for advanced prototyping and development

PEMC Packaging Fab

Total 185,000 ft^2 with 52,000 ft^2 cleanroom in Utica (Quad-C facility)

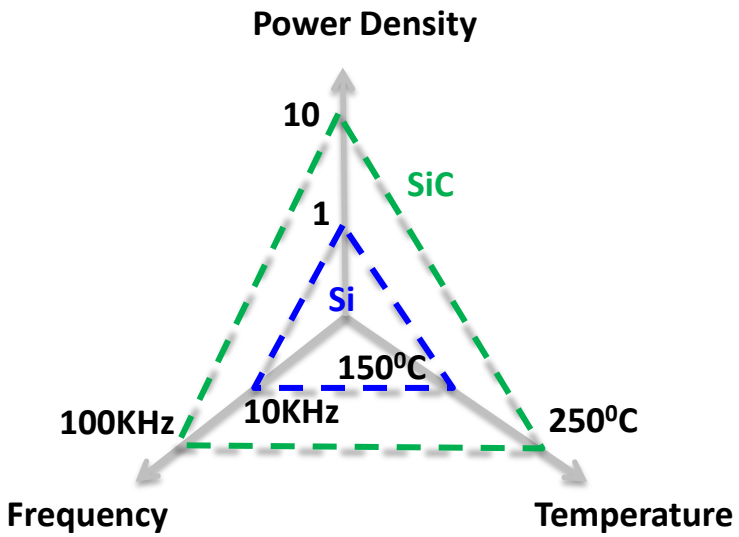
SiC Power Electronics

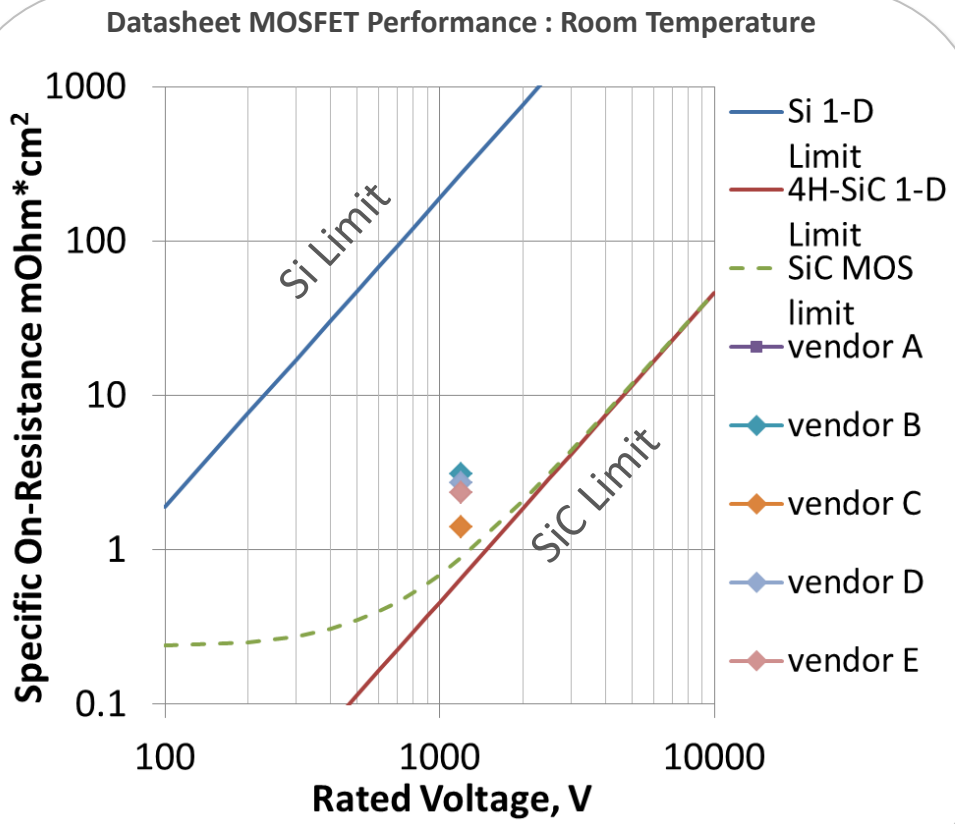
Higher max. temperature: $T_{SiC} \geq 200^{o}C$ *vs.* $T_{Si} \leq 150^{o}$	*Reduced power losses… by more than 50%*	*2X higher power density… more compact / powerful*	More reliable in high temperature environments

Driving the next power revolution

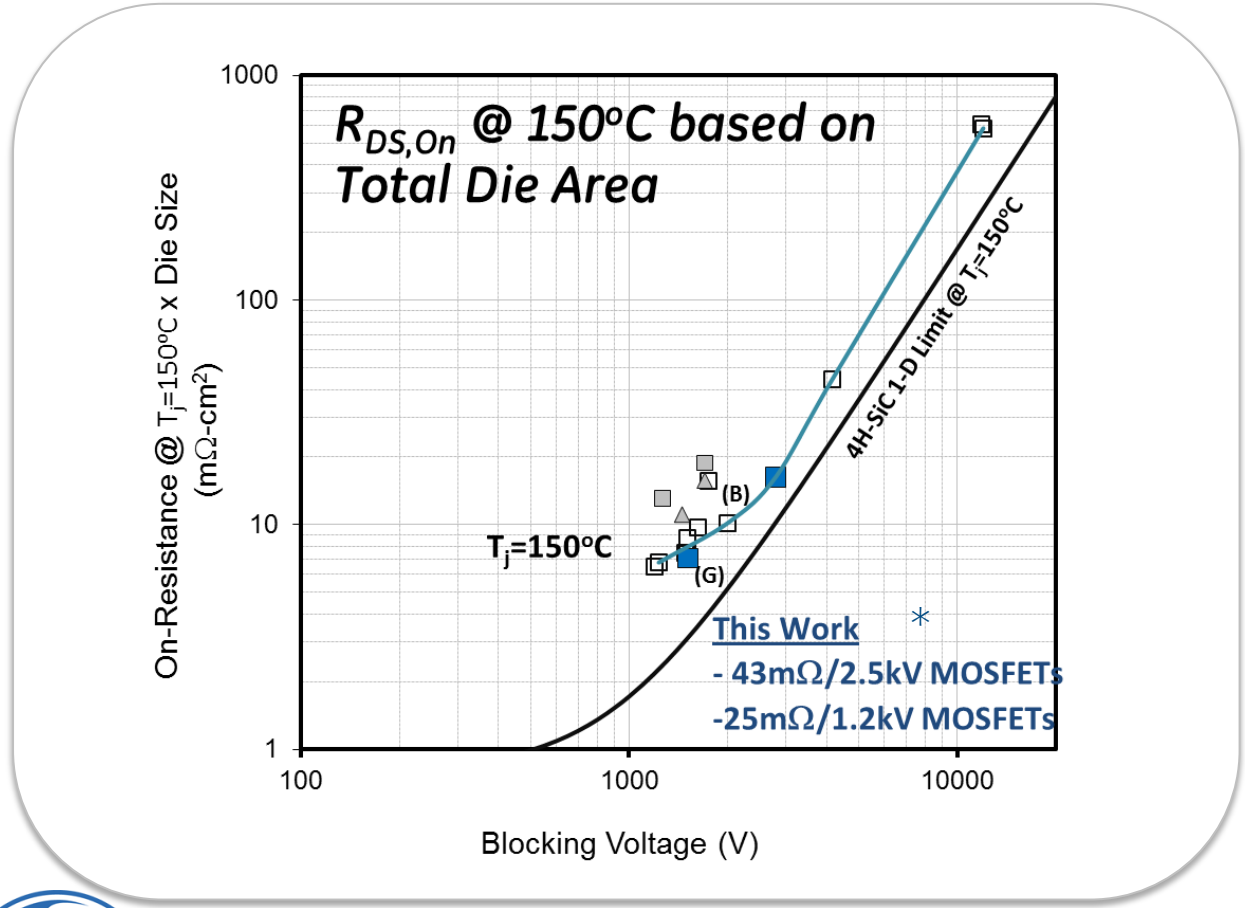
Advantages of SiC

Advantages of SiC power MOS technology over traditional Si





Driving to Low ON-resistance and High Temperature performance with SiC



Product Focused Metrics: 1.2kV and 2.5kV GE' MOSFET Technology

* Losee et al., ICSCRM 2015, Giardini Naxos Italy

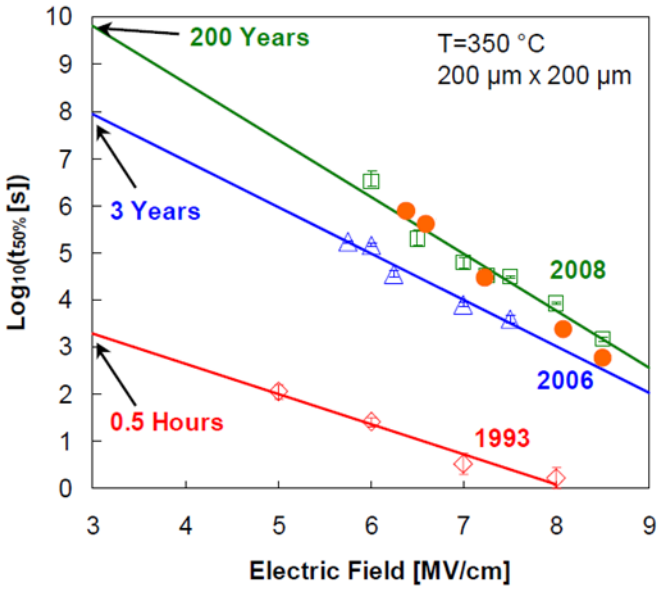
All data courtesy of PEMC Founding Member General Electric

Historical SiC MOS Reliability

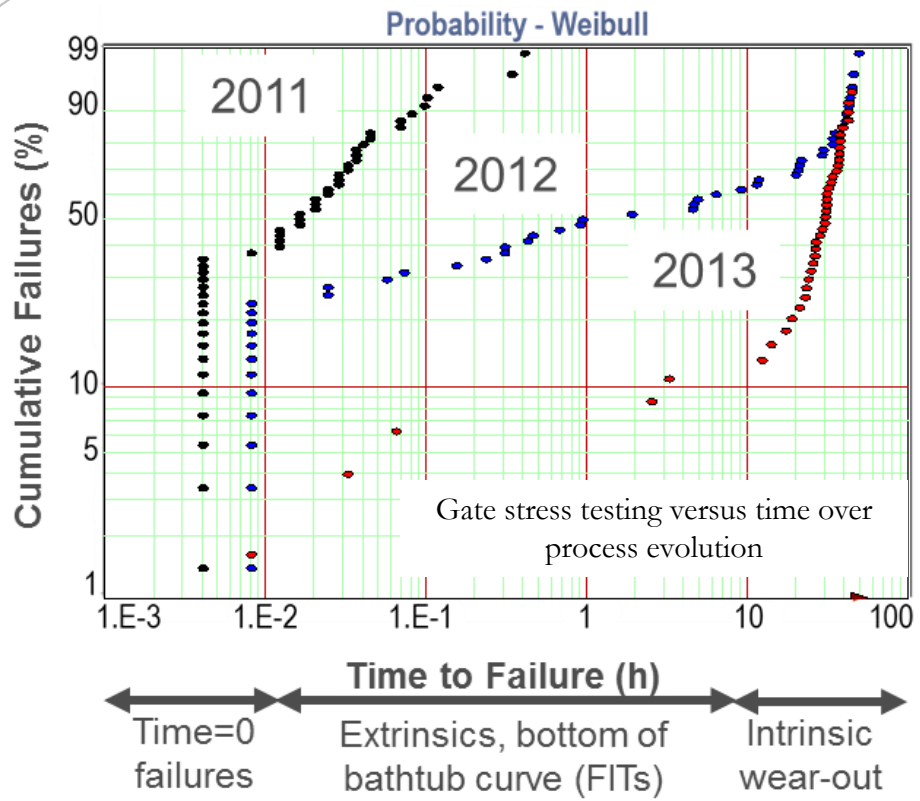
Historical improvement of SiC MOS quality and reliability

Small MOS capacitors:

Area: 200 µm×200 µm, t_{ox}: 47 nm



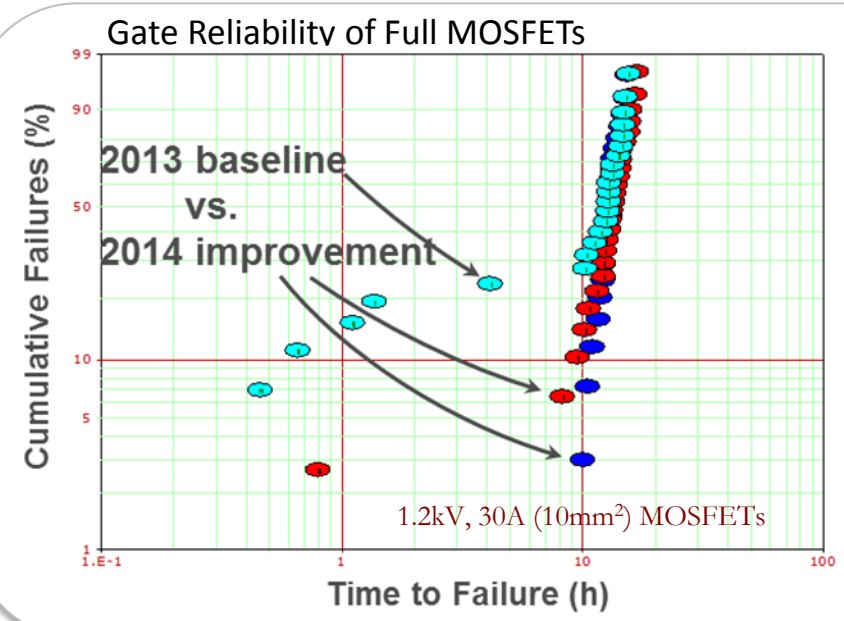
Yu et al., Rutgers/GE, May 2010

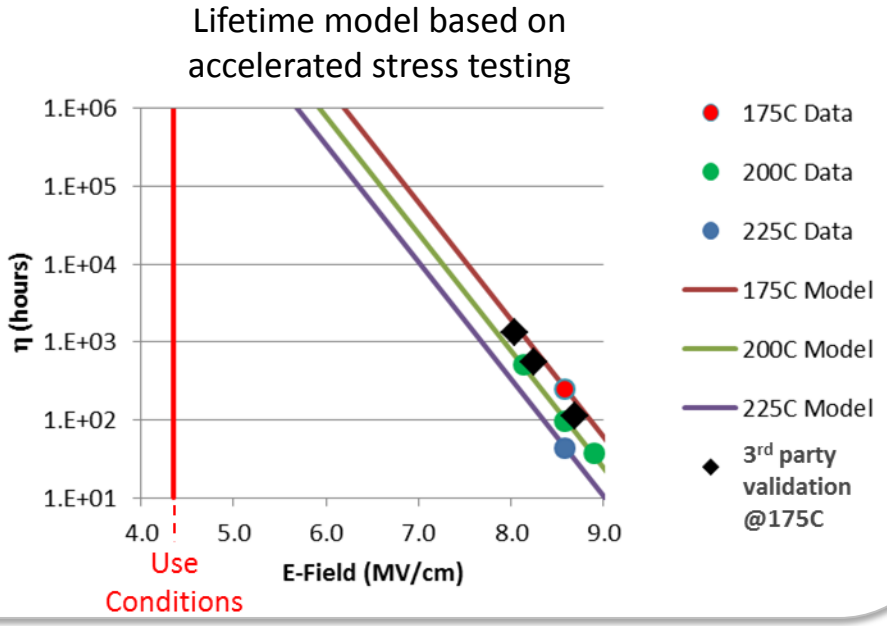


ICSCRM 2015, Giardini Naxos Italy

All data courtesy of PEMC Founding Member General Electric

Gate reliability studied and accurate Lifetime models extracted

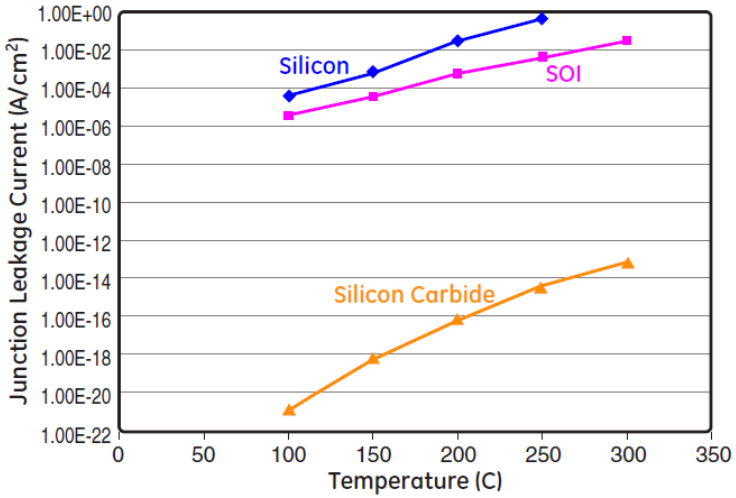




- Lifetime: $T_{LIFE,63\%} = e^{\alpha_0+\alpha_1\times E_{FIELD}+\alpha_2/kT}$
- $T_{LIFE,63\%}$ relates stress test to use conditions
- Acceleration factor: $AF = \frac{T_{LIFE,63\%\ @\ use\ conditions}}{T_{LIFE,63\%\ @\ test\ conditions}}$
- **Model predicts MOSFET intrinsic life >30 years**

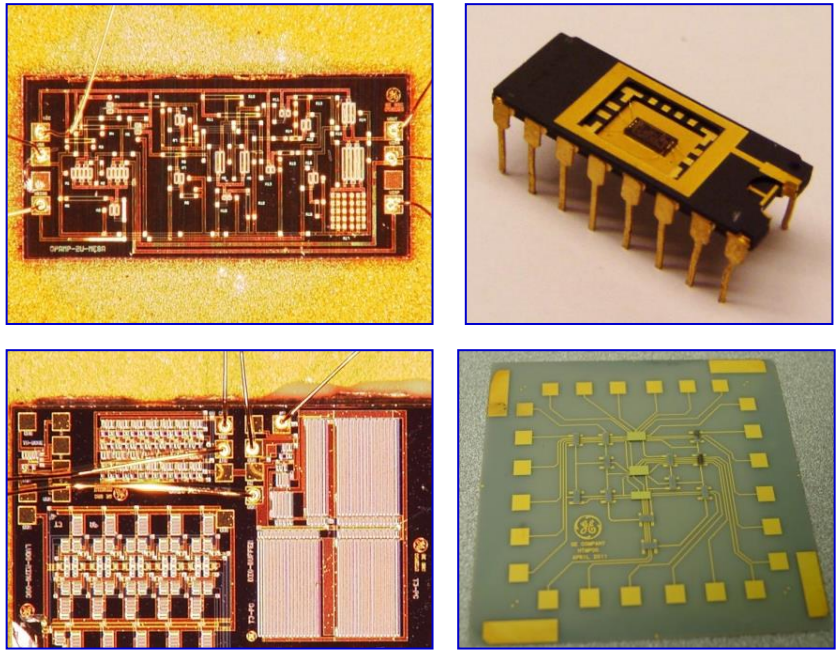
All data courtesy of PEMC Founding Member General Electric

Demonstration of High Temperature Integrated Circuits



Silicon, SOI and SiC junctions leakage comparison

300^{0}C SiC-based Analog and Digital Circuits



DOE Geothermal Technologies Review
2012, Westminster, CO

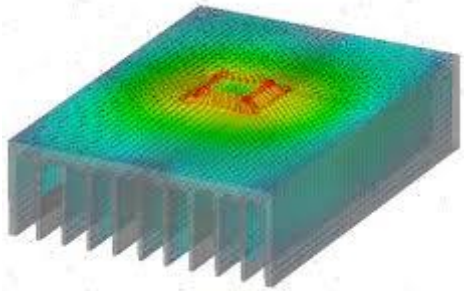
U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

All data courtesy of PEMC Founding Member General Electric

Emerging SiC Electronics

Advanced SiC Device Manufacturing and Packaging: High Temperature Power Systems and Electronics

- High Density and High Frequency Power
- High Temperature Electronics
- Efficient, Heat Sink Cooled Systems
- Radiation Hard Optimized Electronics



Advanced Thermal Management

Electric Propulsion Power Systems

Questions & Discussion