

NEPP The Changing Tide June 15, 2016 GSFC



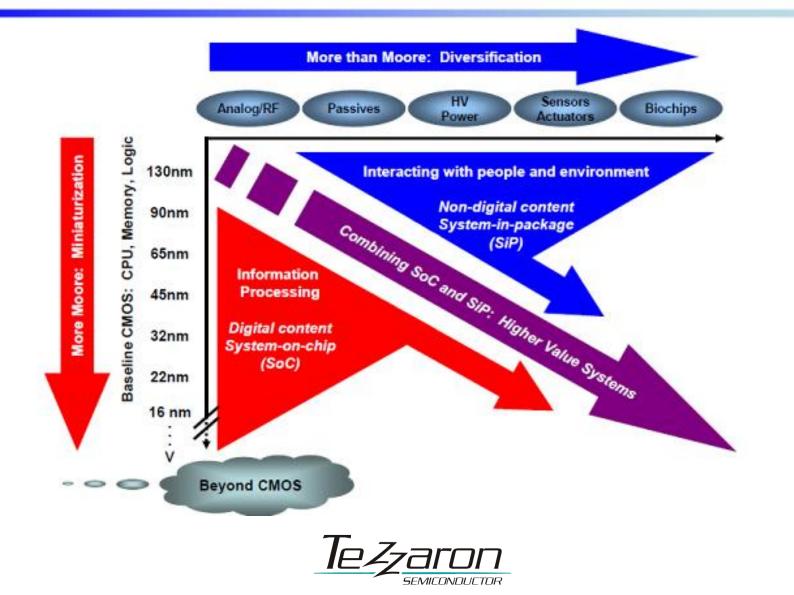


MOORE'S LAW

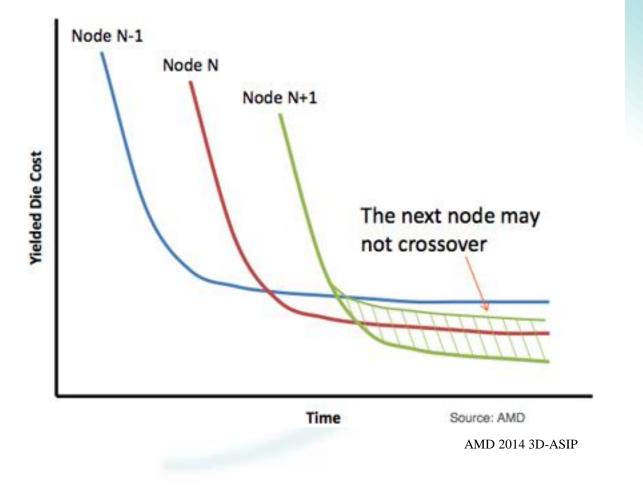




Moore's Law & More than Moore (MtM)

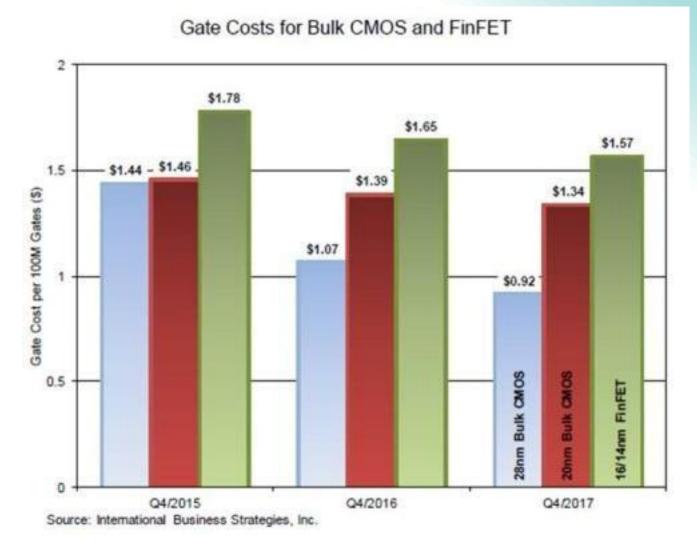


Expiring Economics





Cost Trend Reversal





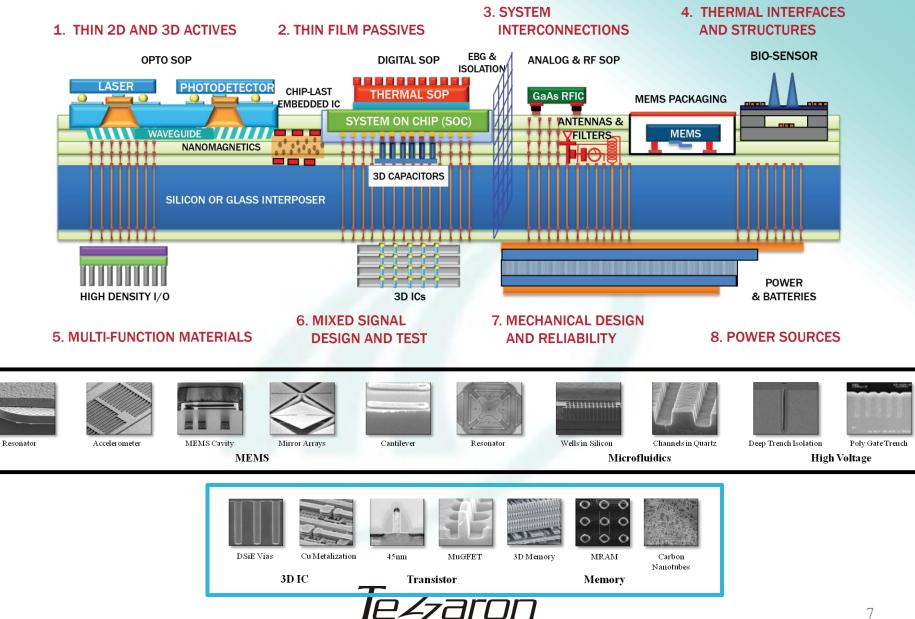
More Moore

- The end is near...
 - 16nm, 14nm, 10nm, 8nm, 6nm, 5nm ...
 - Maybe its now. Maybe it's in 3 years or 5 years, but the end of scaling is going to happen within the next decade
- Most cost effective node for years...28nm?



More Than Moore

GEORGIA TECH PRC



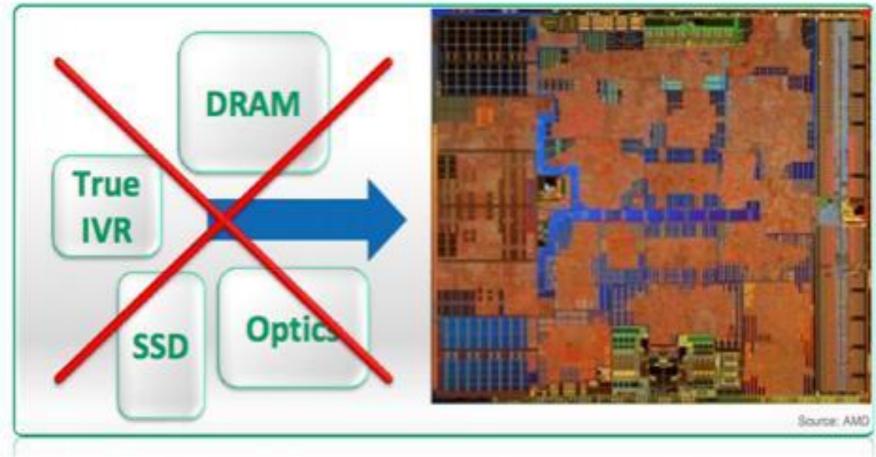
SEMICONDUCTOR



WHAT ARE THE DRIVERS OF CHANGE?



The Apples & Oranges of SOC



AMD 2014 3D-ASIP



Internet Of Things



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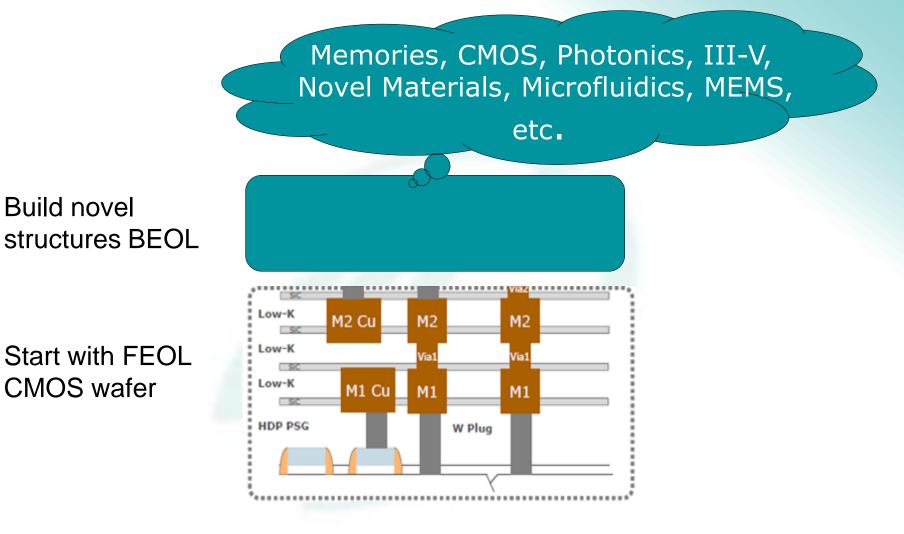
ImpactLab.net



MORE THAN MOORE



The Fabrication Road to More Than Moore





Integration Paths: Additive Silicon and 2.5/3D

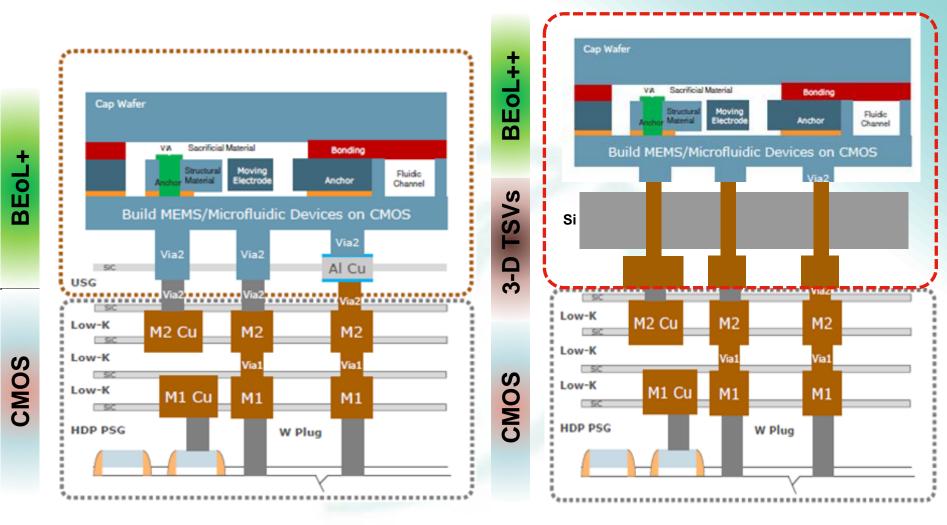
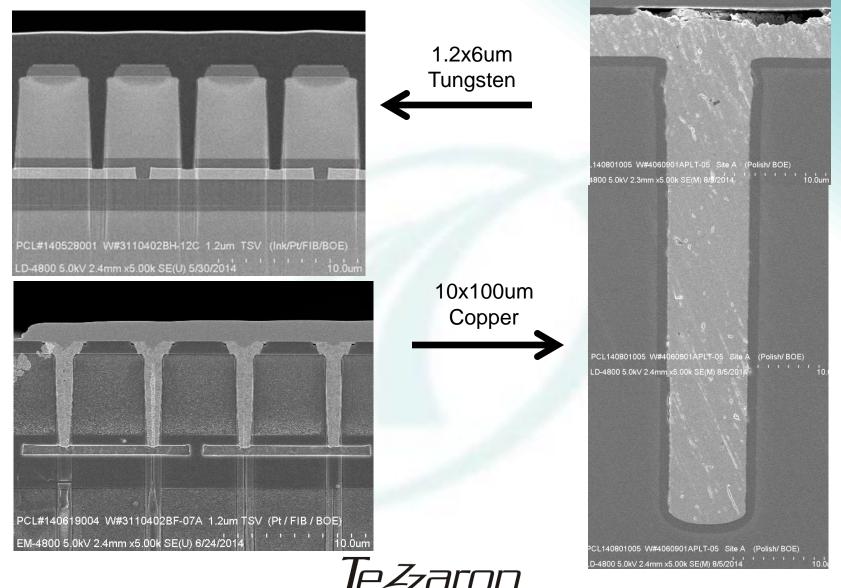


Figure 1: Non-digital devices built directly on CMOS (left), or built separately and joined through 3-D TSVs

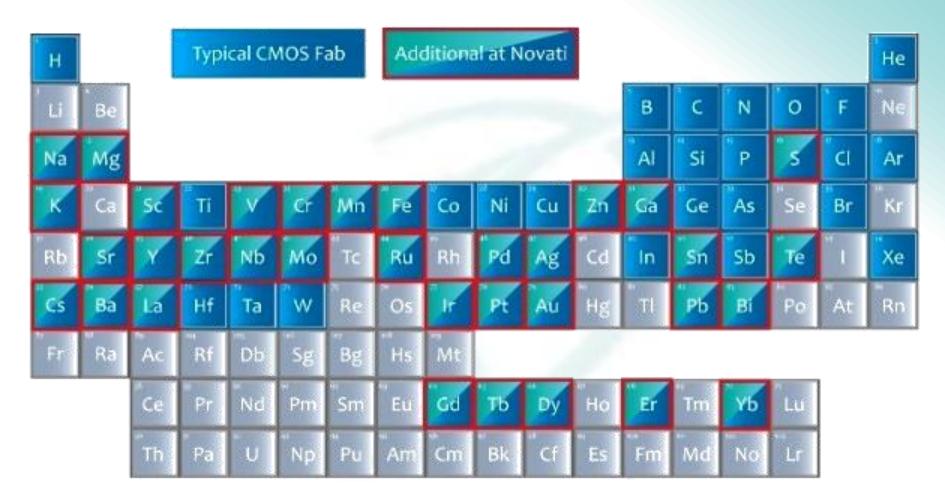


TSV Insertion to Create 2.5/3D Assemblies



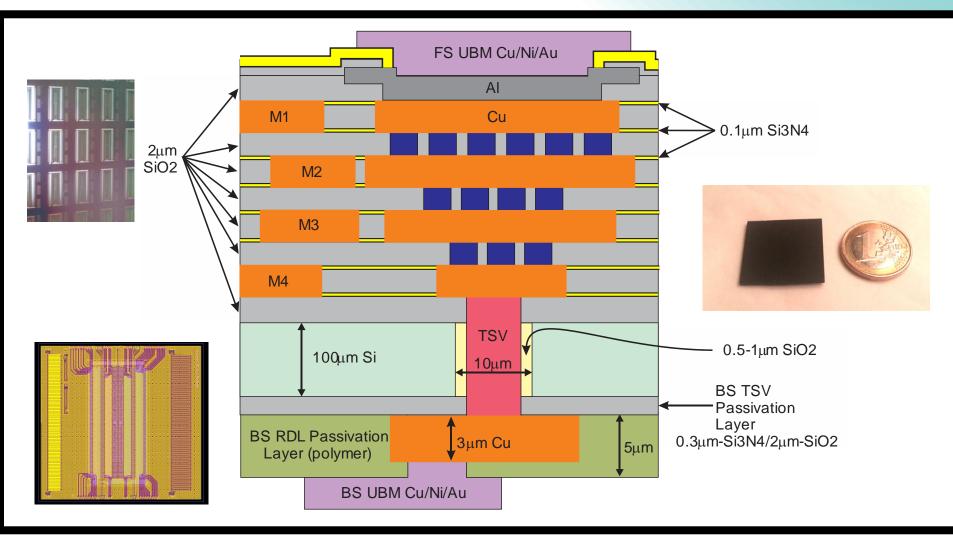
SEMICONDI ICTOR

New Elements Introduced to Fabrication





Si Interposers





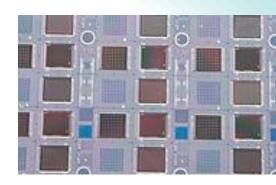
Interposer Parameters

Layer	Metal thickness	R(m Ω/□)	at DC	W	L	Cg (fF)
M1	2µm	9.2		10	2	2.94
		9.2		200	10	58
M2	2µm	9.2		10	2	1.83
				200	10	21.0
M3	2µm	9.2		10	2	1.4
IVIO				200	10	19.7
M4	2µm	9.2		10	2	0.919
1014				200	10	13.9
	TSV Diameter	TSV Height	Resi	stance Cg (fF)		(fF)
Filled	10µm	100µm	$\mathbf{21.2m}\Omega$		180	
Conforma	al 80µm	300µm	~15m Ω		~600	



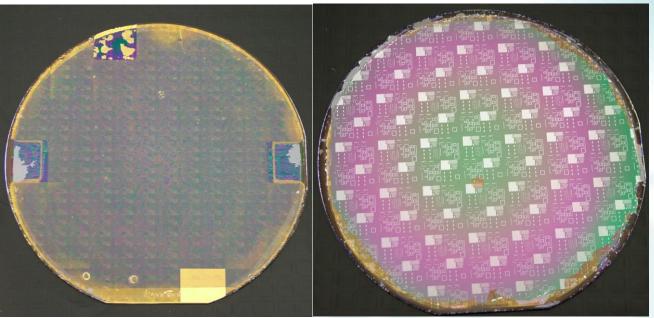
Die on Wafer and Wafer-scale FPA

- •Waferscale integration
- •Up to 85 die assembly
- •10um die space
- •2um placement
- •150/200/300mm

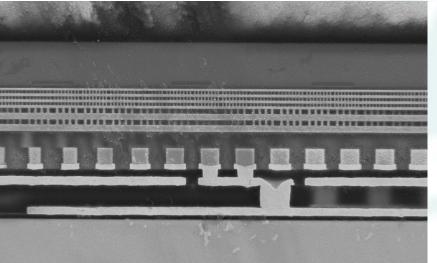


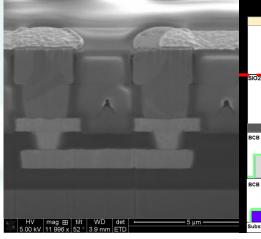


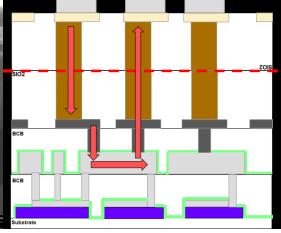
Mixed CMOS-3/5 100mm InP/CMOS



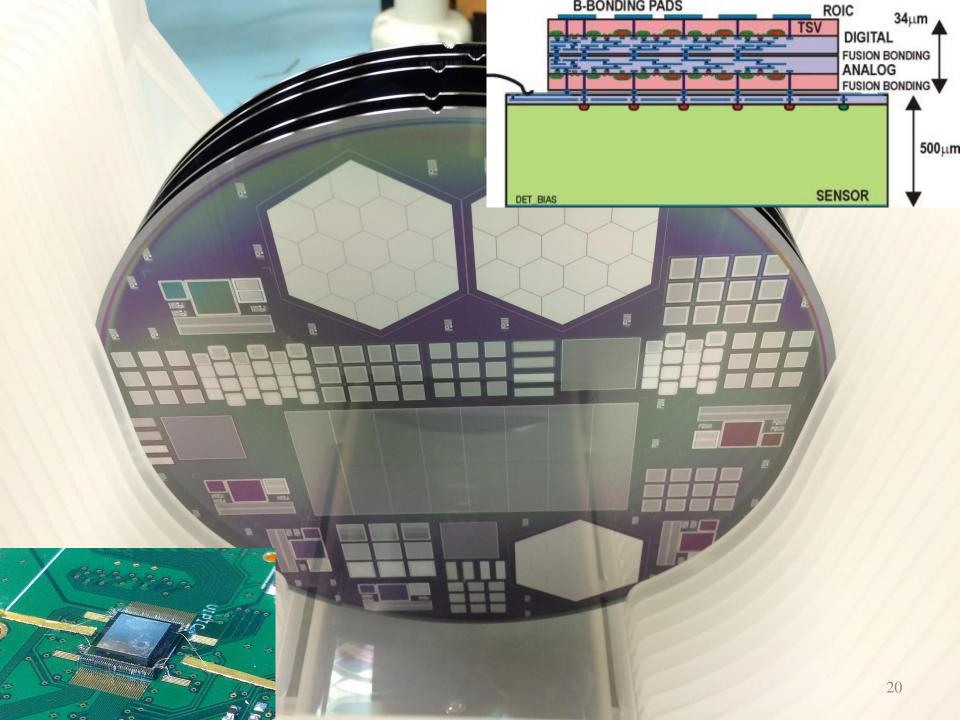
- GaN
- 3D CMOS/InP/GaN
- GaAs
- Graphene



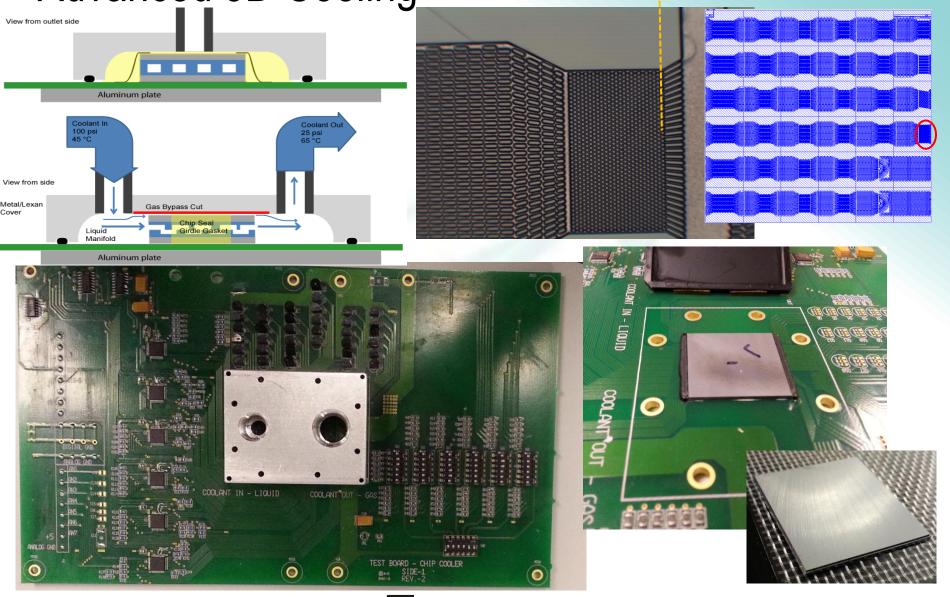






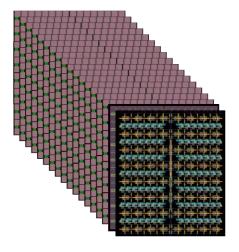


Advanced 3D Cooling





DiRAM4 "Dis-Integrated" 3D Memory



2 million vertical connections per lay per die

I/O layer contains: I/O, interface logic and _____ R&R control CPU. 65nm node _____ Rett

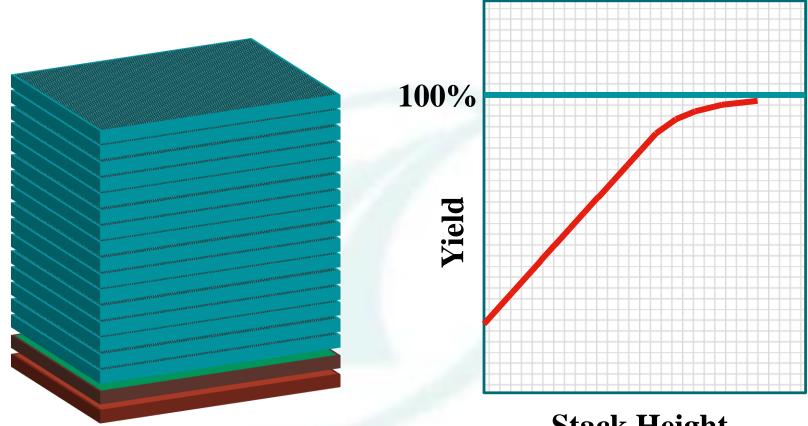
Better yielding than 2D equivalent!



DRAM layers 4xnm node

Controller layer contains: sense amps, CAMs, row/column decodes and test engines. 40nm node

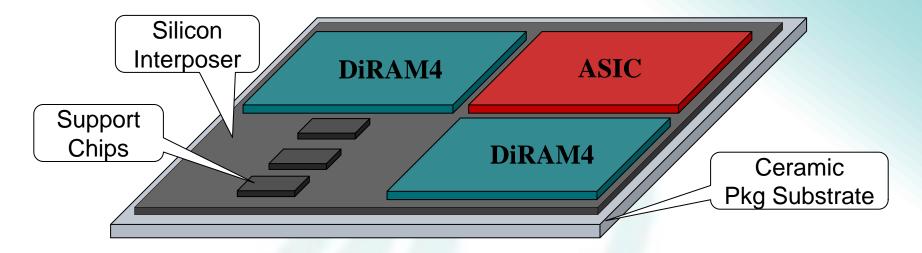
Bi-STAR Repair Improves Yield



Stack Height



HPC Processor Modules

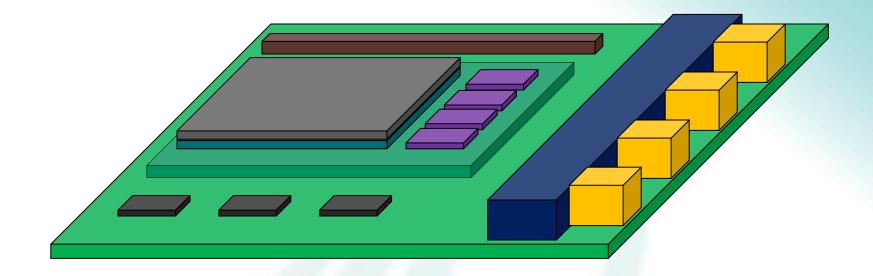


Si Interposer-based Ceramic Package e.g. DiRAM4 plus Custom Processor

50 μ - 100 μ pitch Copper Pillar Die-to-Interposer-to-Die Interconnect
 ~ 10000 Connections – Mostly die-to-die inside package
 ~250 μ pitch C4 Bump Interposer-to-Ceramic Package Substrate Interconnect
 ~ 2000 Connections – Lots of replicated power connections
 I mm pitch Solder Bump Package Substrate-to-Customer PCB Interconnect
 Several Hundred of Connections



And Full Subsystem Modules



Sub-system Modules

e.g. (Tezzaron / Luxtera Optical Memory Module)

Multiple Packages and /or Die on High Performance PCB with System Connectors (Electrical: Card edge or Plugs, Optical: Fiber-optic Cable connectors)

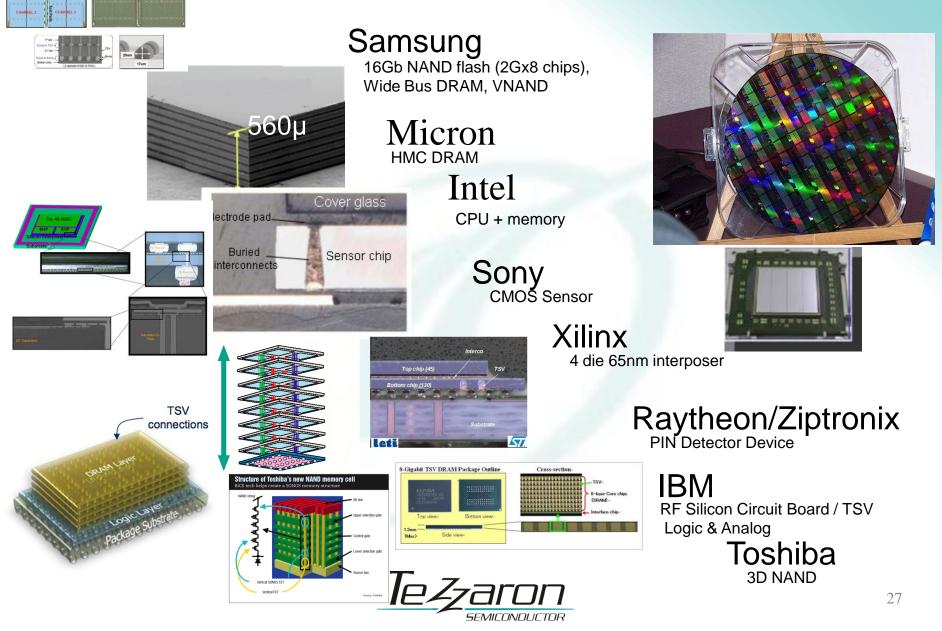




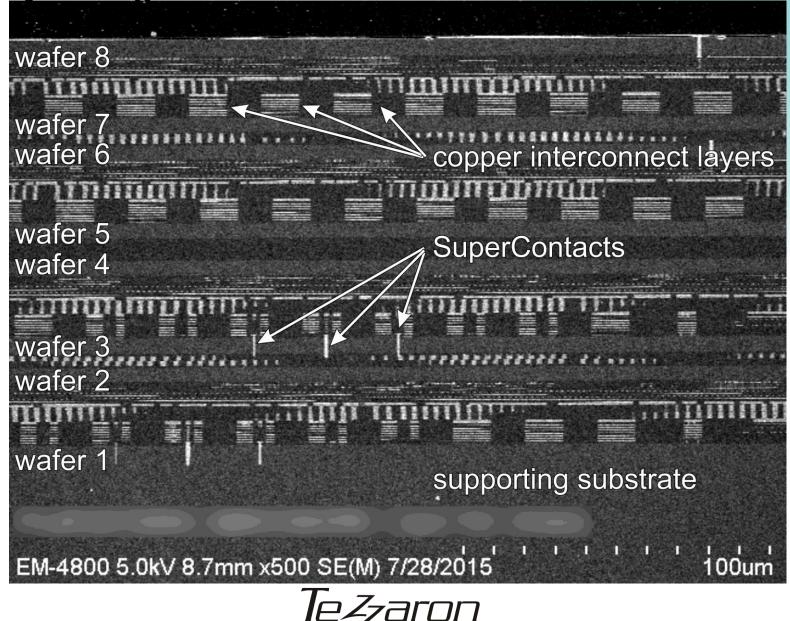
2.5/3D CHANGE IS AT HAND



The Silent Revolution

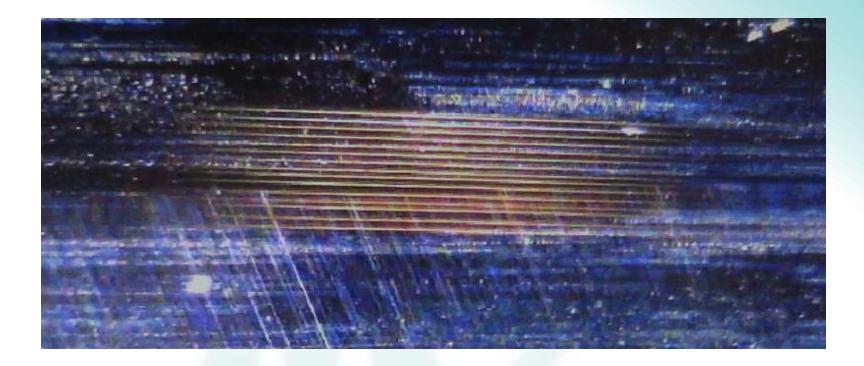


8 Layer Logic Stack



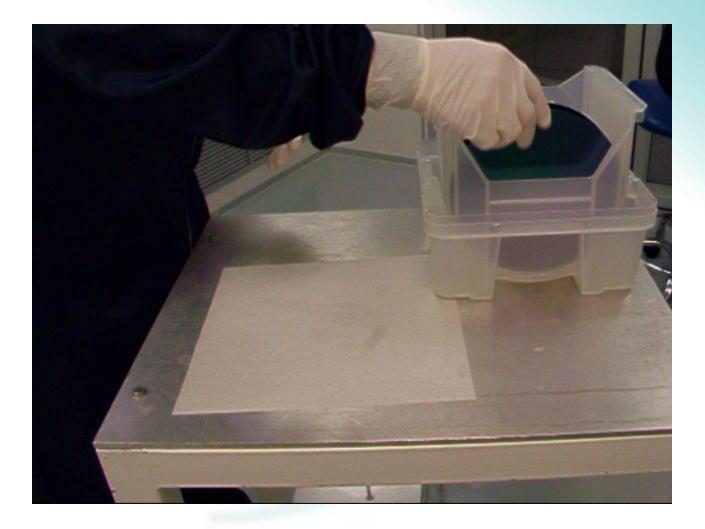
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16 Layer Mechanical Device Stack





Bonding in Action

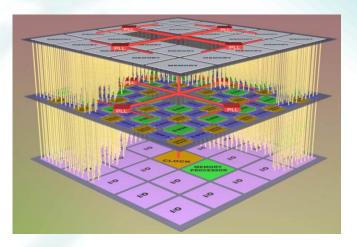




Summary

- 2.5/3D market is in the adoption cycle
 - Moving from novelty to mainstream
- Drivers are:
 - Heterogeneous integration
 - SWaP
 - Increasing performance
 - Lower system costs
- First markets are:
 - Logic Memory
 - Sensors
- Significant industry shifts will happen
 - Silicon circuit cards with "Lego" blocks





Backup



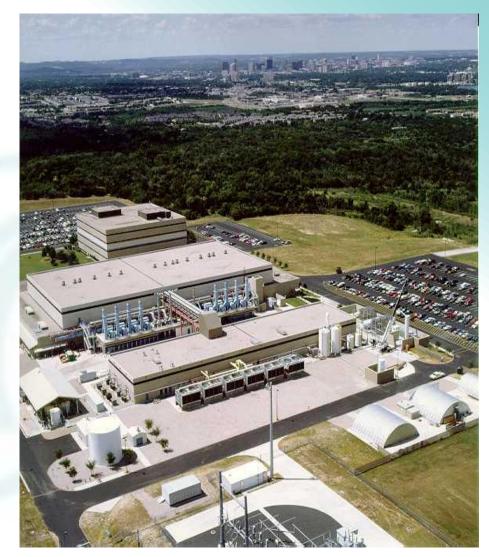


NOVATI OVERVIEW



Austin Facility Overview

- 110 Employees: 90 in Ops and Engineering
- Over 150 production grade tools
- 68,000 sq ft Class 10 clean room
- 24/7 operations & maintenance
- Manufacturing Execution Systems (MES)
- IP secure environments, robust quality systems
- ISO certified/ITAR registered
- Full-flow 200mm silicon processing, 300mm back-end (Copper/Low-k)
- Process library with > 25000 recipes
- Novel materials (ALD, PZT, III-V, etc)
- Copper & Aluminum BEOL
- Contact through 193nm & IR lithography
- Silicon, SOI and Transparent MEMS substrates
- Electrical Characterization and Bench Test Lab
- Onsite analytical tools and labs: SIMS, SEM, TEM, Auger, VPD, ICP-MS, etc

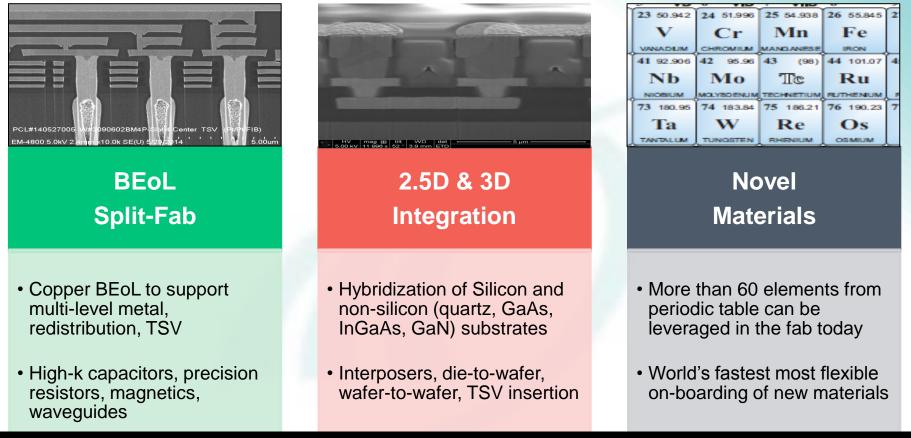




Our Technology Platform



Focused on Convergence of Three Critical Areas



Enabling Advanced Processing, Smart Sensors, Advanced Imagers, RF/Power Electronics



ISO, ITAR and Trust Accreditation



ISO 9001:2008 & ISO 13485 Certified ITAR Registered US Trusted Foundry



ISO 9001:2008

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HEAT OFFICE