Results from Daisy Chain Package Tests on Area Arrays

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June 18, 2016

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Background

- This is a review of the Column Grid Array (CGA) data taken at JPL as part of the FY16 NEPP task.
- This is a follow on to a FY15 task.
- This task will compare two new CGA packages, both FPGA based. One from Xilinx, CN1752, and the other from Microsemi, CGA 1657.
- The packages will have daisy chain die inside them.
- These daisy chains will be used to measure resistance as a function of environmental exposure, mostly temperature cycles.
- Changes in resistance of the daisy chains (>10% of nominal) will be interpreted as a failure and counted as a parts of a statistical analysis.
- The CN1752 is the new standard Xilinx CGA for the V5QV and the CGA1657 is the new standard for the RTG4
- The goal of the task is to understand the possible failure mechanisms of these CGA packages and help determine if that can meet NASA requirements.

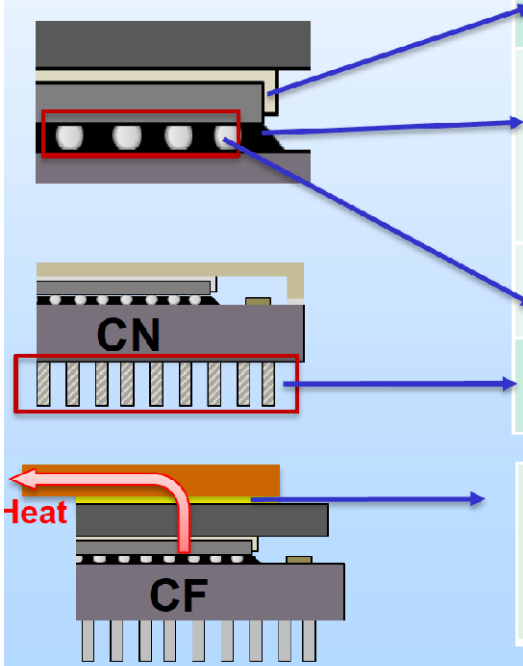
Package vs. Board Testing

- Package level (or 1st level) reliability stress tests are dedicated to the robustness of the packaging materials and design to withstand extreme environmental conditions.
- 1st level testing does not consider solder interconnect reliability when it is board mounted.
- Board level (or 2nd level) reliability tests, stresses are concentrated on the solder joint interconnect performance of the surface mount package when it is board mounted.
  - Temp cycling, bending, drop, vibration are all different 2nd level reliability tests

Board Level Temperature Test Requirements (ED-4702A and IPC-9701)

Factor	Requirements		
	ED-4702A		IPC 9701
Temperature condition (Top – operating temp)	TCA: -30°C ←→ +80°C		TC1: 0°C ←→ +100°C (preferred)
	TCB: -25°C ←→ +125°C		TC2: -25°C ←→ +100°C
	TCC: -40°C ←→ +125°C		TC3: -40°C ←→ +125°C
	TCD: -65°C ←→ +125°C		TC4: -55°C ←→ +125°C
	TCE: Top_{min} ←→ Top_{max} (usually 25°C←→70°C)		TC5: -55°C ←→ +100°C
Duration	5 years equivalent	10 years equivalent	Test until 50% (or 63.2% preferably) cumulative failures on samples or
	TCA: 1217 cyc	TCA: 2433 cyc	200 cycles
	TCB: 435 cyc	TCB: 869 cyc	500 cycles
	TCC: 365 cyc	TCC: 730 cyc	1000 cycles (preferred for TC2, TC3 & TC4)
	TCD: 277 cyc	TCD: 553 cyc	3000 cycles
	TCE: 1825 cyc	TCE: 3650 cyc	6000 cycles (preferred for TC1)

History of NEPP Sponsored CGA and Related Technologies Tasks



	FY	Title
CF heat spread adhesive material (TIM1) (IBM ATI material)	2012	Physics of Failure Analysis of Xilinx Flip Chip CCGA Packages
CF underfill material (IBM LP2 material)	2011	Underfill Materials for Reliable Flip chip Packaging
	2012	Physics of Failure Analysis of Xilinx Flip Chip CCGA Packages
Flip chip solder joints/ Underfill	2012/ 2013	Aeroflex technology as class-Y demonstrator
CN package's Six Sigma Columns	2015	Virtex 5 CN Daisy chain evaluation
Thermal management (TIM2/heat transfer device)	2014	Thermal Interface Materials Selection and Application Guidelines

- NEPP has been investigating all aspects for CGA technologies for several years.

Comparison of the CGA from Xilinx and from Microsemi

	Xilinx V5	Microsemi
# of columns	1752	1657
Package size	45x45 mm	42.5x42.5 mm
Ceramic thickness	4.11mm	2mm
Column type	Six Sigma	Six Sigma
Column height	2.20 mm	2.21 mm
Column diameter	0.51 mm	0.51 mm
Column pitch	1 mm	1 mm

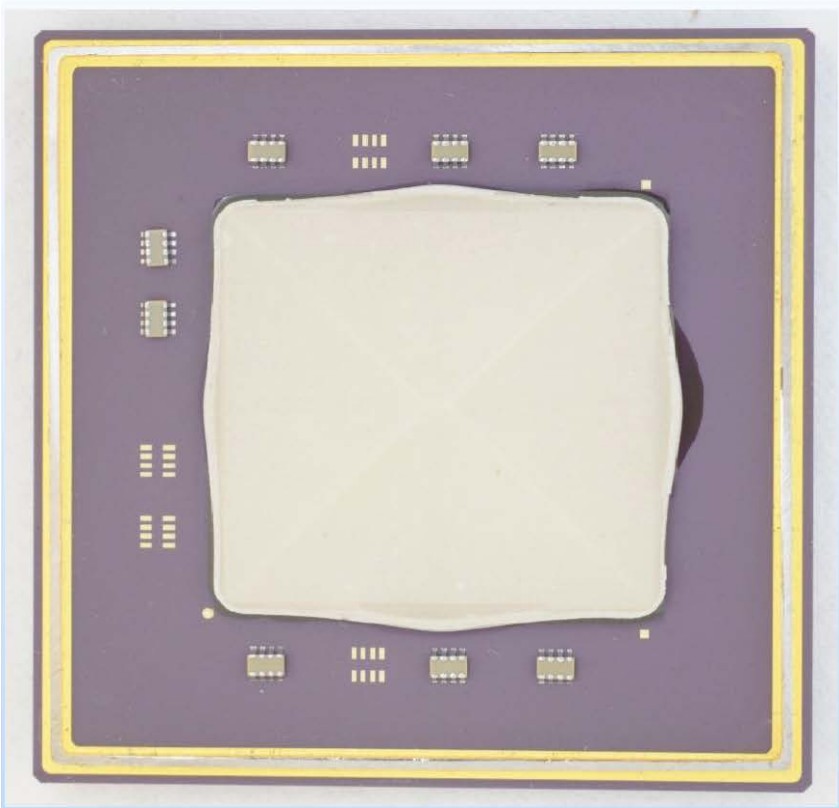
- The parts are very similar in size and identical in column specifications

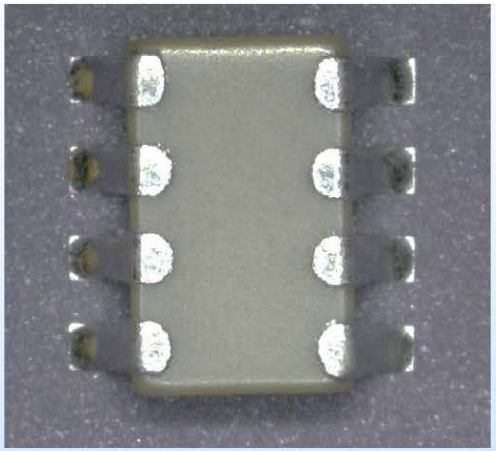
Experiment Description

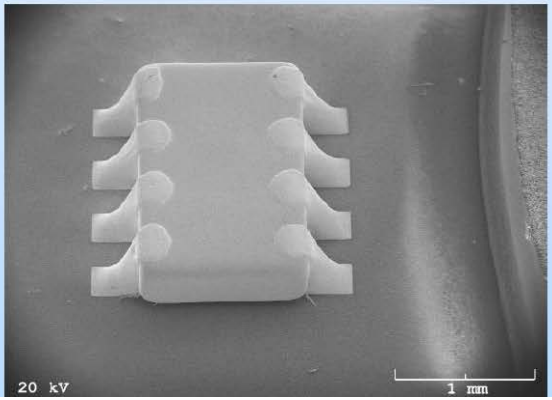
1. Visual examination of CGA parts
2. Elemental and cross sectional analysis of columns and bypass capacitors
3. Thermal Shock testing of one individual DUT
    1. Visual check
    2. Two-terminal resistance measurement of columns
4. Board level reliability test of daisy chain parts
    1. Two different types of board material and two different temperature cycle ranges are the experimental splits

- *Items 1-3 are FY15 and Item 4 is FY16*

Visual analysis of Microsemi CGA 1657







- With the top off the part, the epoxy covering the die is now exposed
- SEM photos of the BME capacitors are all shown.
- All capacitor sites are not populated. Daisy chain do not require capacitors to function.

Elemental analysis of Columns on Microsemi CGA

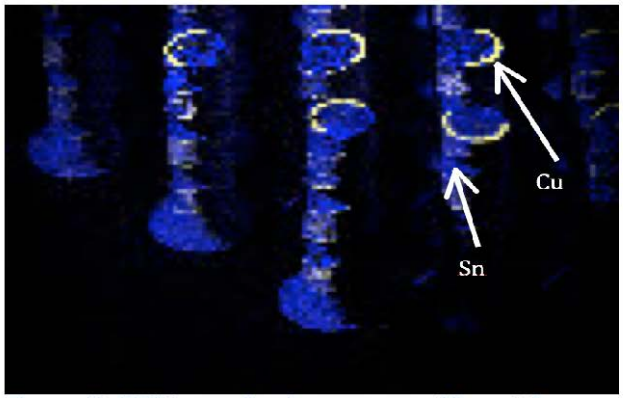


Figure 13: EDX image for the presence of Sn and Cu

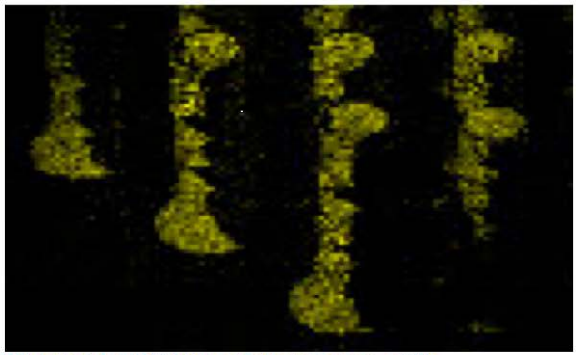


Figure 14: EDX image for presence of Pb

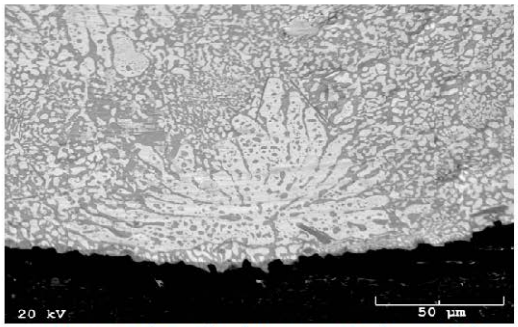


Figure 15: SnPb phases on the base of the columns

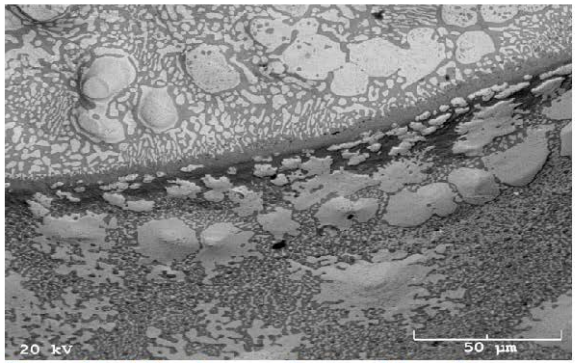


Figure 16: SnPb phase on the top of the column

- EDX (Energy Dispersive Xray Spectroscopy) analysis uses each atoms unique signature to identify constituent elements.
- The copper coils used by Six Sigma are clearly visible
- Variation in SnPb phase across the column is visible

Capacitor Analysis

	Current Cap	Revised Version
Manufacturer	AVX (X7R)	Presidio (X7R)
Electrode	BME (Nickel)	PME (Silver Palladium)
Voltage	6.3V and 4V	6.3V
Capacitance	2.2 ± 20% 0.68 ± 20%	0.18 uF ± 10%
Dissipation Factor	5% max. (for 10V)	7.5% (MIL-PRF-Thin)
Thermal Conductivity	4-5 W/m K	6W/mK
Terminations	Plated Ni and Solder	NT9 (Ni + 90%Sn-10%Pb)
L x W x T (mm)	2.03 x 1.27 x 0.96	0.05 x 0.08 x 0.017
Inductance	55 to 65 pH	110 to 130 pH range
Metallization Band	0.004 mm min band	0.005 mm min band

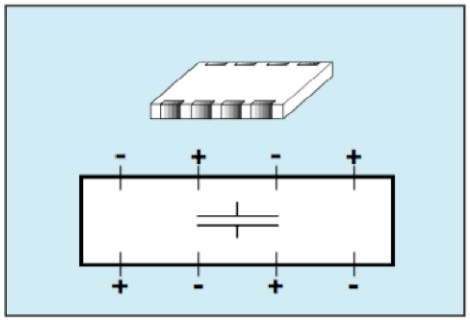


Figure 17: Schematic of AVX BME interdigitated capacitor (IDC)

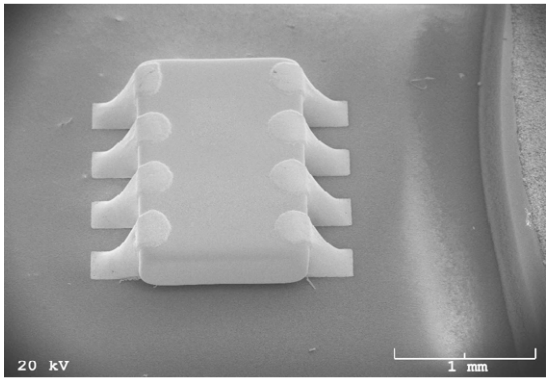


Figure 18: SEM image of capacitor

- BME capacitors were initially provided
- PME capacitors will be used as well

Capacitor Cross Section - AVX (BME) vs Presido (PME)

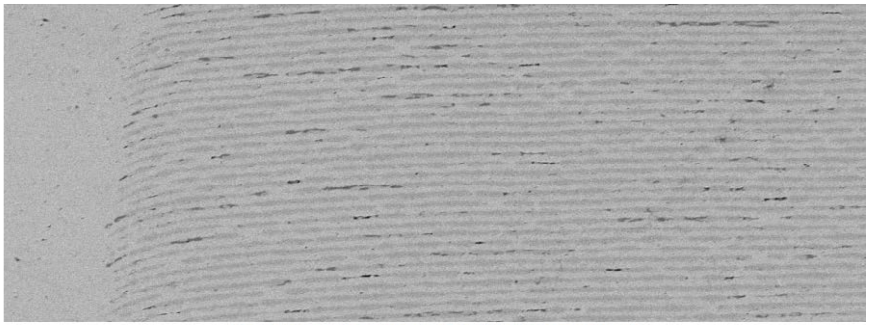


Figure 19: X-section of AVX BME capacitor

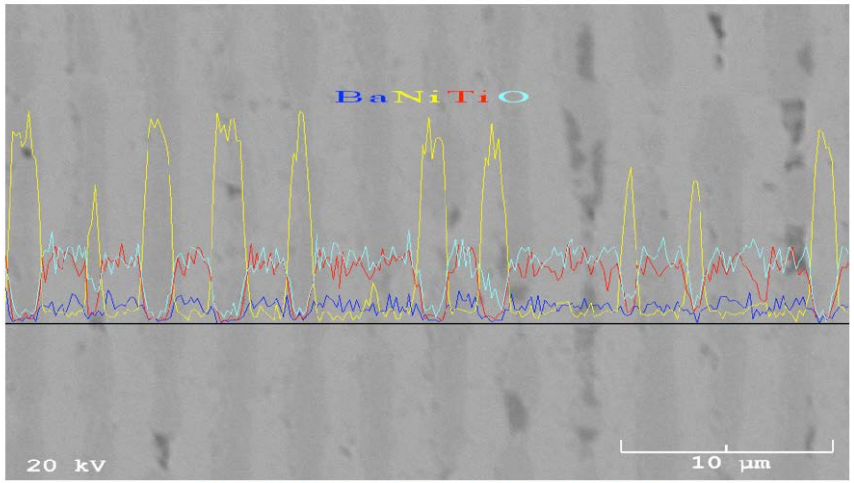


Figure 20: Elemental analysis of capacitor body

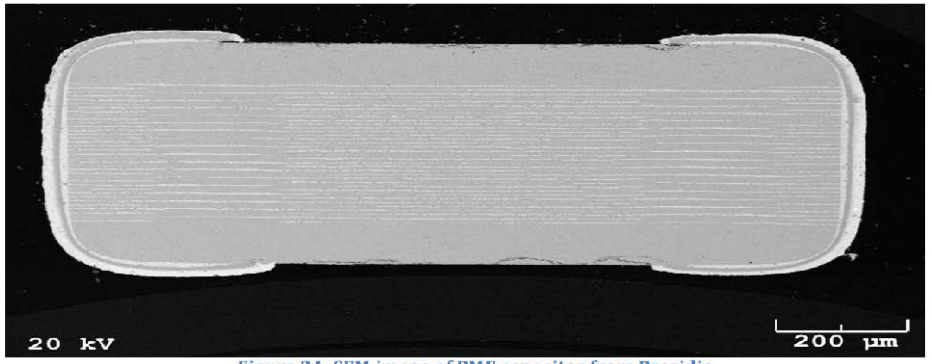


Figure 24: SEM image of PME capacitor from Presidio

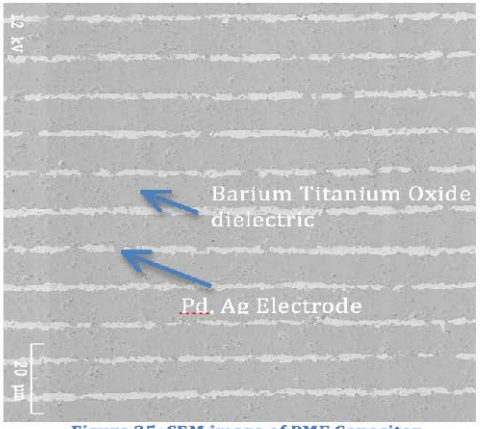


Figure 25: SEM image of PME Capacitor

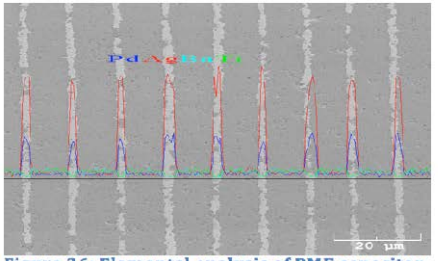
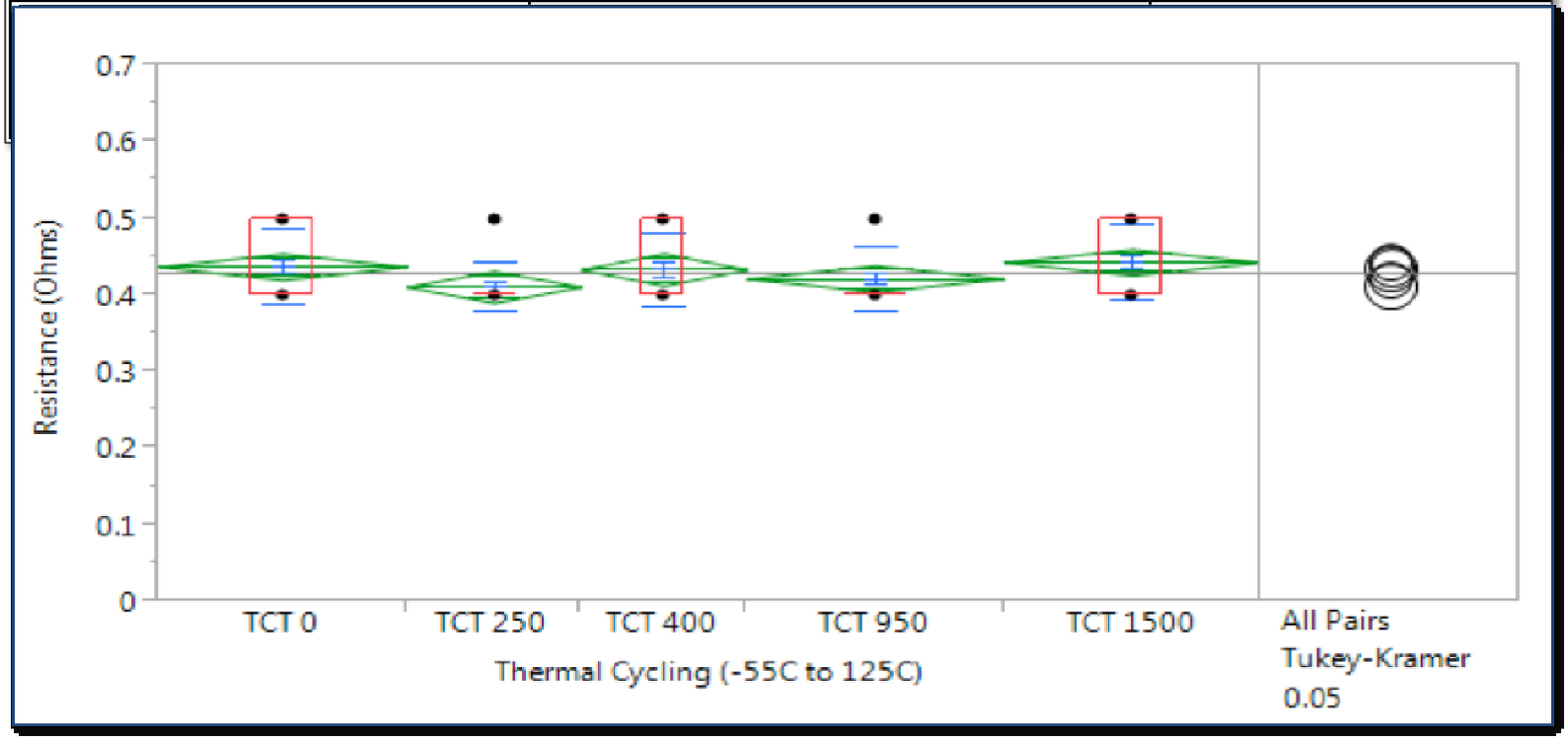


Figure 26: Elemental analysis of PME capacitor

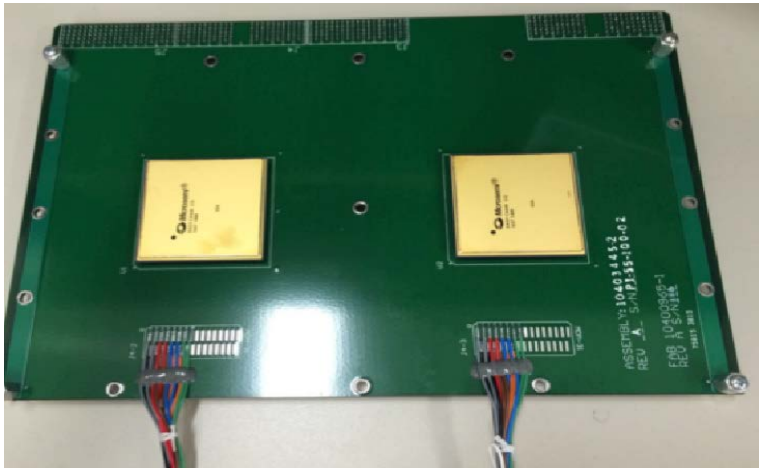
- BME capacitors were initially provided
- PME capacitors will be used

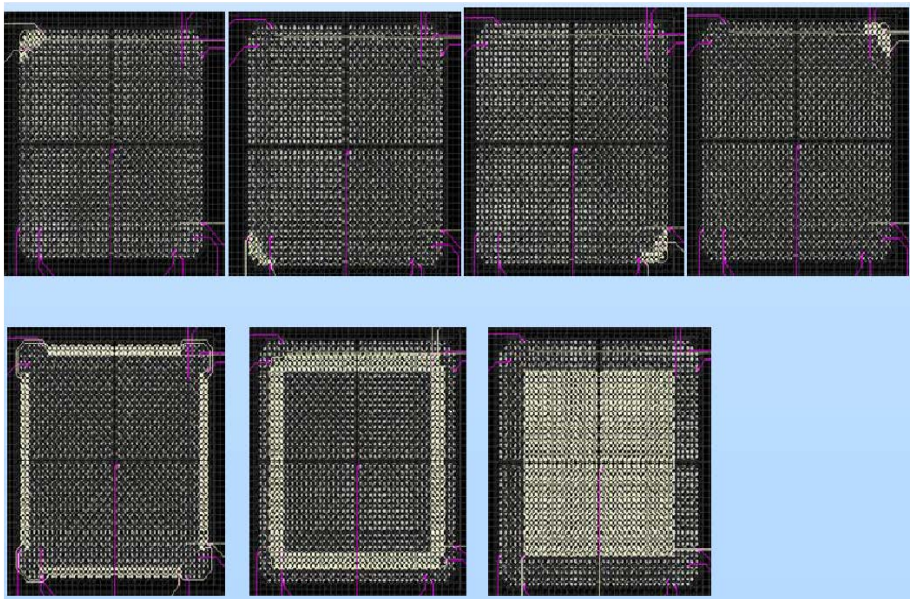
Microsemi CGA DUT Testing

Test	Results	Status
Visual Inspection	Optical, SEM Images	PASS, Complete
Gross leak test	Pass – Mil Std 883 1014.14	PASS, Complete
Fine leak test	Pass – Mil Std 883 1014.14	PASS, Complete
Component level TCT	-55 C to 125C	1500 cycles PASS



Xilinx and Microsemi Daisy Chains





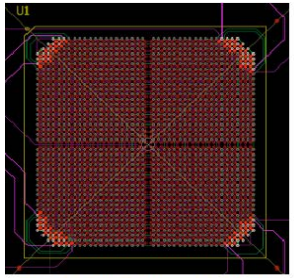


Figure 34: Daisy Chain corners (4 chains)

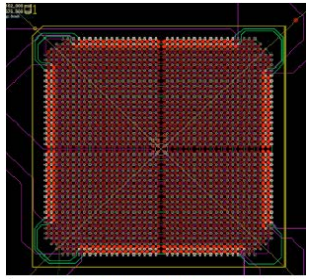


Figure 35: Daisy chain edges (1 chain)

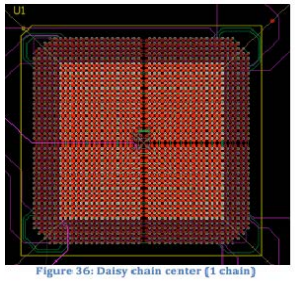


Figure 36: Daisy chain center (1 chain)

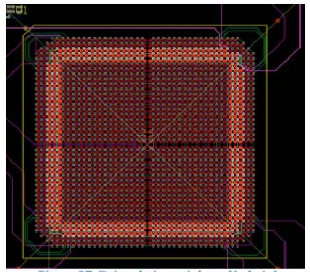


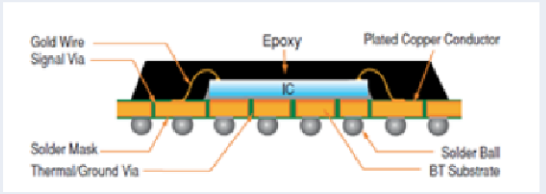
Figure 37: Daisy chain periphery (1 chain)

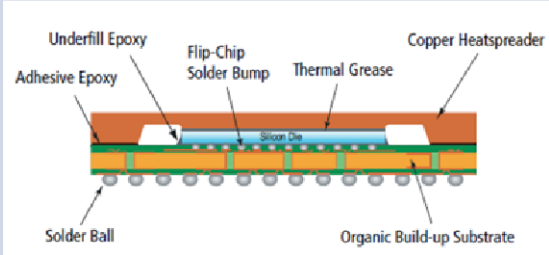
Xilinx Daisy Chain Test Board Matrix

Part S/N	Test	Test Details	Board SN	Status
01		Capacitor exposure, -55/100 dual zone temp cycling (72cyc /day)	SN009	No Cap solder degradation @ 100 cyc
02		Part level reflow --> SMT Process optimization --> capacitor evaluation etc	SN001	
03	FR4 Board	0 to 100°C TC 10C/min ramp, 10 min dwell	SN101	No failure 6586 cycles
04				No failure 6586 cycles
05			SN102	No failure 6586 cycles
06				No failure 6586 cycles
07		-55 to 100°C TC 3.3C/min ramp, 10 min dwell	SN103	No failure 1705 cycles
08				No failure 1705 cycles
09			SN104	No failure 1705 cycles
10				No failure 1705 cycles
11	PI Board	0 to 100°C TC 10C/min ramp, 10 min dwell	SN002	No failure 6586 cycles
12				No failure 6586 cycles
13			SN003	No failure 6586 cycles
14				No failure 6586 cycles
15		-55 to 100°C TC 3.3C/min ramp, 10 min dwell	SN004	No failure 1705 cycles
16				No failure 1705 cycles
17			SN005	Internal daisy chain Failure @ 1236 cycles
18				No failure 1705 cycles
19		Dual zone chamber cycling (-55 to 100C, 10 min dwell (72cyc/day)) & Impedence monitoring tool development	SN006	No failure 3389 cycles
20				Internal daisy chain Failure @ 2097 cycles

Xilinx Commercial FPGA Packages*

Package code	Dimension (mm)					Shape param.	Char. Life	Package construction
	Body size	Pitch	Ball Size	Substrate Thickness/#layer	Die Size			
FG676	27x27	1.0	0.60	0.56 /4	17.8x17.8x0.3	11.01	6013	
FG900	31x31	1.0	0.60	0.56 /4	17.0x17.0x0.3	8.46	5344	
FG1156	35x35	1.0	0.60	0.56 /4	23x21x0.3	6.713	4892	
FF896	31x31	1.0	0.60	1.152 /6	10x10x0.7	14.53	6784	
FF1152	35x35	1.0	0.60	1.152 /6	22x20x0.7	11.9146	3822	
FF1704	42.5x42.5	1.0	0.60	1.152 /6	26x22x0.7	19.1835	3389	
BF957	40x40	1.27	0.75	1.1152 /6	22x20x0.7	7.33	3663	
SF363	17x17	0.8	0.50	0.6 /4	10x10.0.3	14.9811	2048	

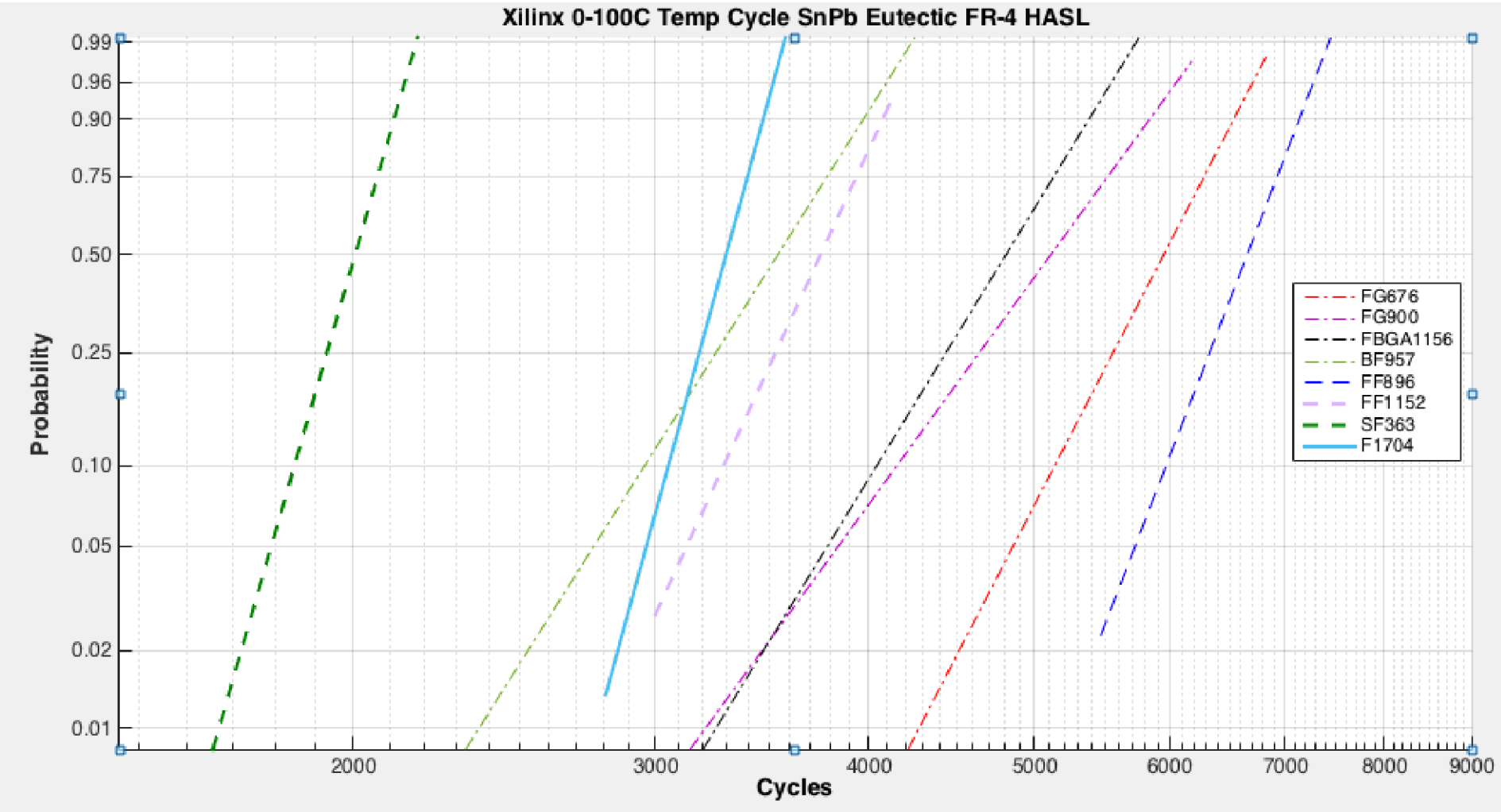




- This data represents the current COTS package options from Xilinx.
- Its used here to provide a reference comparison and benchmark for the CGA data

*Xilinx Device Reliability Report UG112 2015

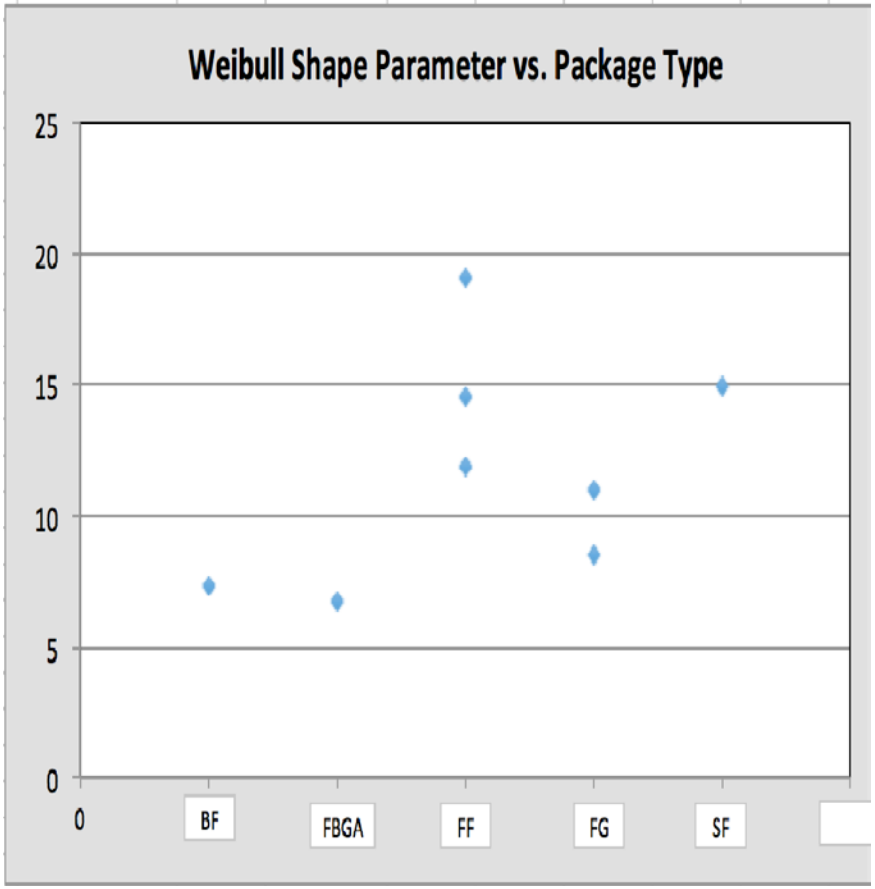
Xilinx Provided Weibull Data – Commercial Packages

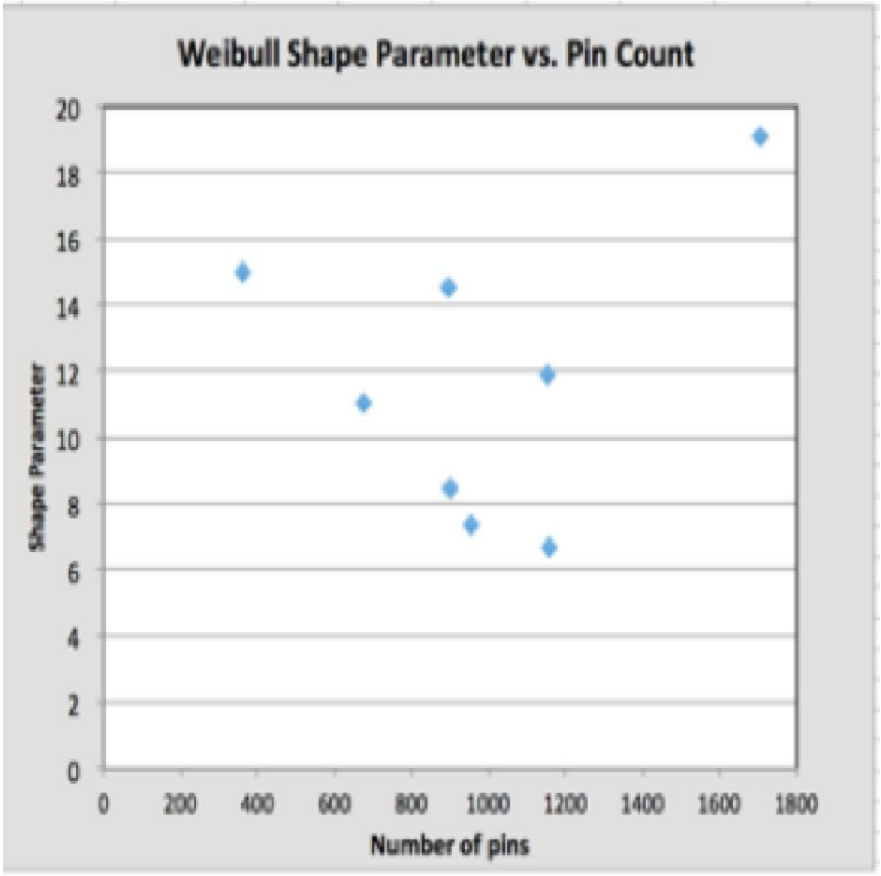


Wide range in number of cycles and time to first fail but all >1000 cycles

*Xilinx Device Reliability Report UG112 2015

Analysis of Xilinx Weibull Data

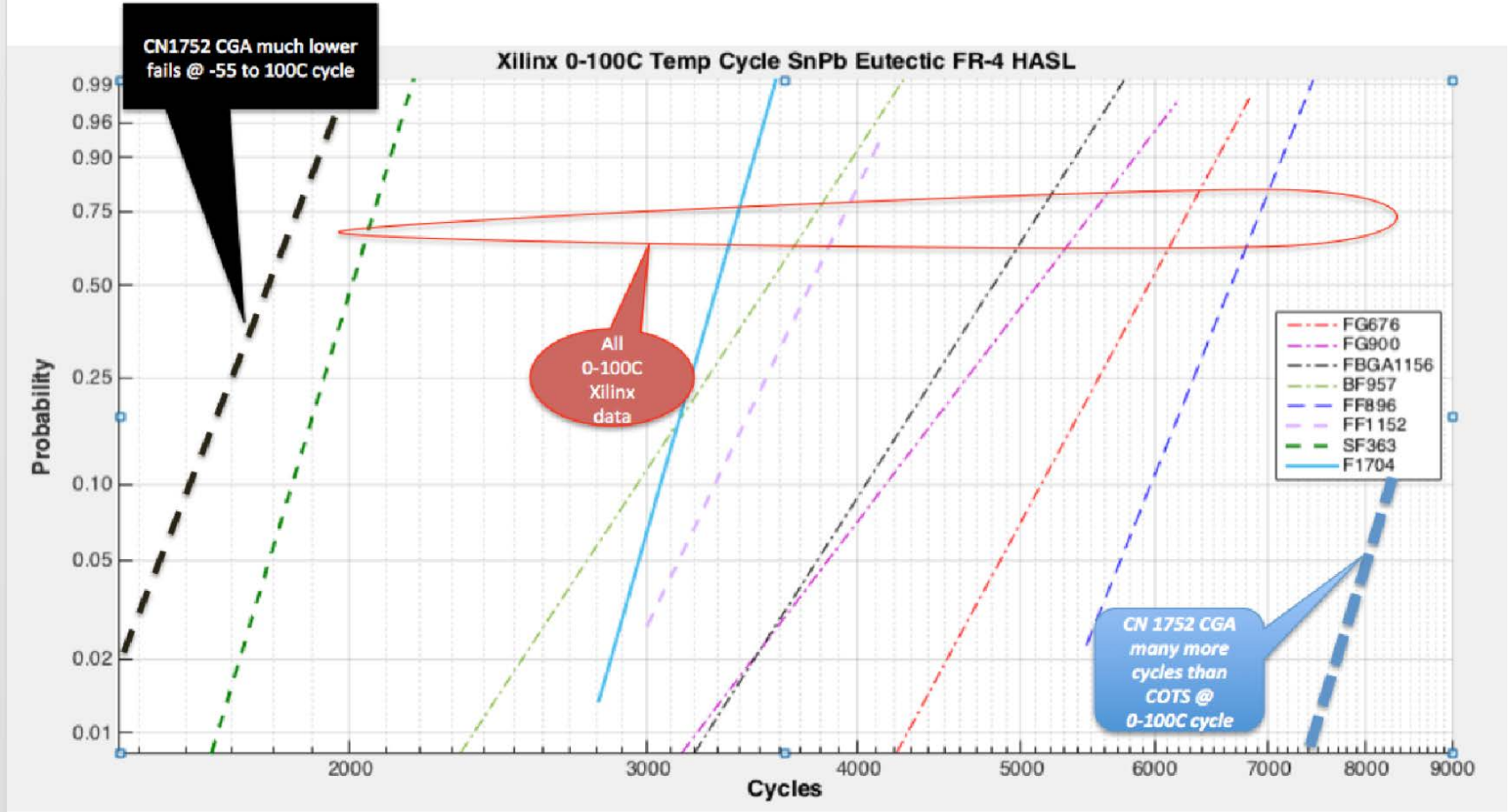




$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}}$$

- The shape parameter, β, is shown to have an inverse correlation with the number of pins.
- There also appears to be a correlation to the type of package

Physics of Failure Analysis of COTS FPGA Packages vs. Space CGA



- For the same test conditions, the CGA parts have significantly improved reliability over all the other package types.
- However, CGA reliability is a strong function of test conditions.

Physics of Failure Analysis of COTS FPGA Packages vs. Space CGA

- High pin count CGA package have significantly improved reliability over other packaging types for a given PCB material and temp cycle range.
- Temp cycle range has a significant effect on reliability of CGA packages. This indicates different physics of failure mechanisms being activated
- As a DUT, the package passes mil spec temp range (1st level)
- 2nd level (Board) testing shows passing IPC-9701 spec conditions
- Qualification process must precisely determine their temperature ranges and take care to not extrapolate to different operating regimes.
- Additional testing is planned to investigate this effect.

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