

## Commercialization of Specialized Nanotechnology Fabrication in a Certified Domestic Foundry

NASA Electronic Parts and Packaging (NEPP) Program  
2016 Electronics Technology Workshop

Wilbur Catabay

June 16, 2016

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### Outline

- TSI Semiconductors
  - Specialized Foundry Services
  - TDCS - Technology Development & Commercialization Services
- Case Studies
  - Foundry, Customer Foundry, Development
- Leveraging Automotive Certifications for Military Standards
- Summary




## TSI Semiconductors at a Glance

### Business Segments

- Automotive
- Industrial & Power Management
- Mil-Aero
- IOT

Strong customer technology collaboration with a flexible model for Foundry and Development with novel materials


### Strong Domestic Presence



Customer	Technology	Approx Revenue	Customer	Technology	Approx Revenue
A- US	Medical	\$ 50B	F- US	Consumer	Start-up
B- US	RF Antenna	\$ 25B	G- US	ATE	Start-up
C- Japan	Automotive / Diversified	\$ 9B	H- China	MEMS	Start-up
D- Japan	Automotive / Diversified	\$ 8B	I- US	Lighting	Start-up
E- US	Memory	\$ 6B	J- US	Memory	Start-up

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### US On-Shore Facilities, Roseville, Ca



- Foundry, Custom Foundry & Development
- Capacity of 10,000 wafers per month
- Capacity at 30% of clean room space

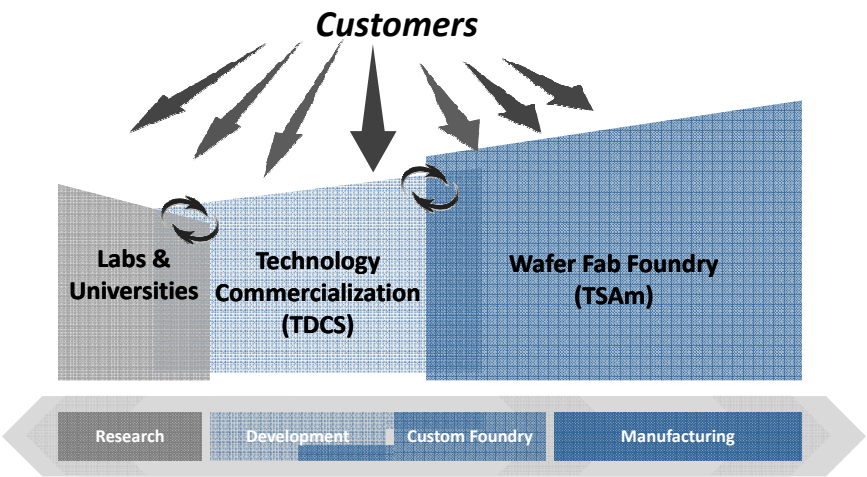
### World Class Foundry


- Over 30 years of continuous operations
- 24/7 Operations, Clean room 150,000 Sq/ft
- Logic, High Voltage, Mix Signal, Analog, RF
- Novel Materials Integration
- IP Secure Environment
- ISO & Auto Certification
- DMEA Trusted & ITAR




## Custom Foundry: Development to Manufacturing

**Customers**









## TSI Process Technology Platforms


**Low Voltage**  
1.8V, \*3.3V, 5V - 20V  
Display, Optics, Drivers, Medical,  
Automotive, Wireless Charging



**Automotive**

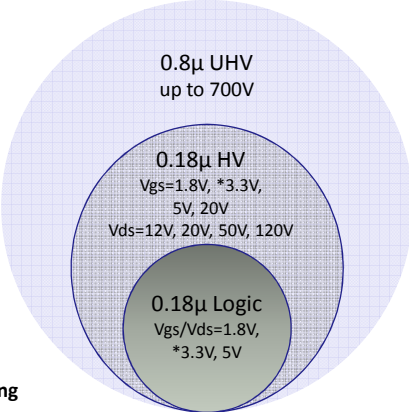


**Medical**




**Telecom /Networking**


**Medium Voltage**  
12V - 120V  
Automotive, Industrial, Medical,  
Networks, Lighting




**Ultra High Voltage**  
Up to 700V  
LED, IGBT, MOSFET



**Industrial**




**Aerospace**



**Lighting**

0.8μ UHV up to 700V  
0.18μ HV Vgs=1.8V, \*3.3V, 5V, 20V Vds=12V, 20V, 50V, 120V  
0.18μ Logic Vgs/Vds=1.8V, \*3.3V, 5V

5 \*available Q4'16




## IBM 7HV Technology Transfer

- 0.18μ technology was transferred in 8 months
- Two customers completed silicon runs during the transfer period
- Significant number of devices from Logic, HV, Analog, RF, Mix-Signal

TSI Semiconductors Process Device Menu					
Process	Logic CMOS		Analog/Mixed Signal/RF		High Voltage
VGS	1.8V & 5V	5V Only	1.8V & 5V	5V Only	1.8V, 5V & 20V
Triple Well Isolation	Yes	Yes	Yes	Yes	Yes
FETs	1.8V, 5V	5V Only	1.8V (RF only), 5V	5V Only	1.8V, 5V, 12V, 20V, 25V, 50V, 120V
	High Vt * (2ML)	High Vt * (2ML)	High Vt * (2ML)	High Vt * (2ML)	High Vt * (2ML)
	Super high Vt * (2ML)	Super high Vt * (2ML)	Super high Vt * (2ML)	Super high Vt * (2ML)	Super high Vt * (2ML)
Resistors	N+, P+ diffusion & poly	N+, P+ diffusion & poly	N+, P+ diffusion & poly	N+, P+ diffusion & poly	N+, P+ diffusion & poly
			RR poly high R - 1.6KD/sq (1ML)	RR poly high R - 1.6KD/sq (1ML)	RR poly high R - 1.6KD/sq (1ML)
			RP poly precision R - 16SD/sq (1ML)	RP poly precision R - 16SD/sq (1ML)	RP poly precision R - 16SD/sq (1ML)
			TaH BEOL (1ML)	TaH BEOL (1ML)	TaH BEOL (1ML)
Diodes	Schottky Barrier	Schottky Barrier	Schottky Barrier	Schottky Barrier	Schottky Barrier
Decoupling Caps and Variators	1.8V/5V N, P caps, vars	1.8V/5V N, P caps, vars	1.8V/5V N, P caps, vars	1.8V/5V N, P caps, vars	1.8V/5V N, P caps, vars
BEOL Caps	Vertical native (VWcap)	Vertical native (VWcap)	Vertical native (VWcap)	Vertical native (VWcap)	Vertical native (VWcap)
			Single MM - 2.1 fF/μm <sup>2</sup> (1ML)	Single MM - 2.1 fF/μm <sup>2</sup> (1ML)	Single MM - 2.1 fF/μm <sup>2</sup> (1ML)
			Dual MM - 4.1 fF/μm <sup>2</sup> (1ML)	Dual MM - 4.1 fF/μm <sup>2</sup> (1ML)	Dual MM - 4.1 fF/μm <sup>2</sup> (1ML)
BEOL Metal	6LM-M1-MT	6LM-M1-MT	7LM-M1-MT Analog Metal (AM) - 4μm	7LM-M1-MT Analog Metal (AM) - 4μm	7LM-M1-MT Analog Metal (AM) - 4μm
	IM, V3, MS, VS	IM, V3, MS, VS	IM, V3, IM, V3, MS, VS	IM, V3, IM, V3, MS, VS	IM, V3, IM, V3, MS, VS
Inductors			Analog Metal (AM) - 4μm Al	Analog Metal (AM) - 4μm Al	Analog Metal (AM) - 4μm Al
Masks (TP, 3LM)	21	16	21	16	21

\* Optional Devices/Layers

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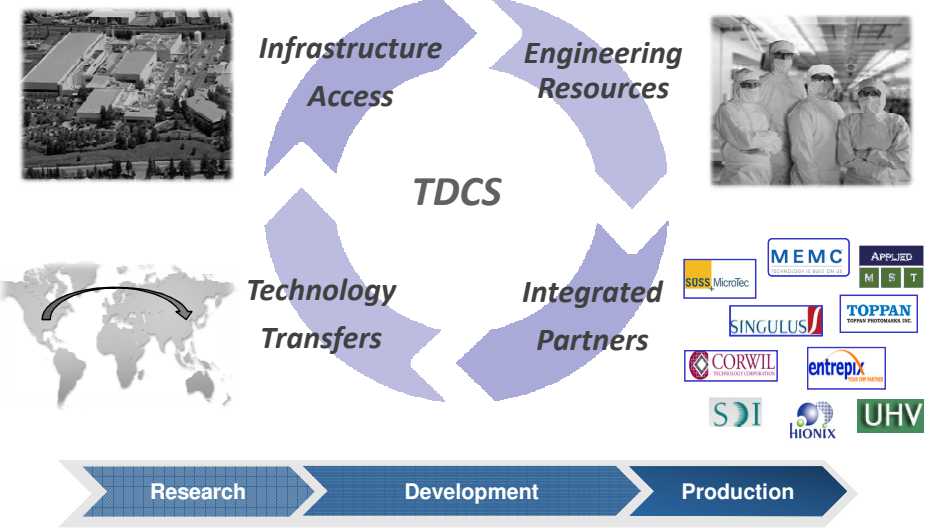
## Technology Development & Commercialization Services (TDCS)

*We create a collaborative relationship with customers to enable the fastest and most cost effective time to market for technology and product commercialization while enabling customer IP independence*


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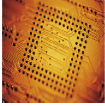
### Technology Development - Collaboration




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## Process Module Toolbox




Semiconductor




Medical




Telecom



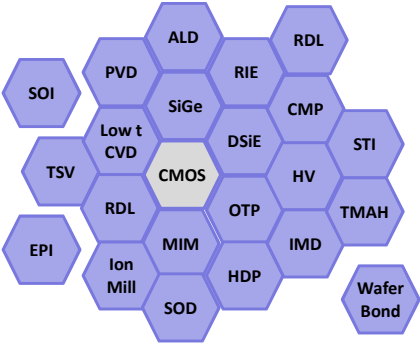
Mil Aero



Consumer Mobility




Clean Energy



We offer a toolbox of proven process modules and process techniques. These modules can be combined and integrated to deliver unique, differentiating functionality to novel technologies.

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## New Materials Flexibility – Emerging Market Focus


**TDCS Equipment Capability**

**TSI TDCS Installed Equipment**

**Traditional CMOS Elements**

H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac	Rf	Db	Sg	Bh	Hs	Mt									
		Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu		
		Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr		

**Element Review Board (ERB) enables safe & efficient introduction of new materials into facilities**

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## Non-Volatile Memory Materials Development

### Memory Materials Development

New Materials Flexibility – Emerging Market Focus

Element Review Board (ERB) enables safe & efficient introduction of new materials into facilities

Device	Materials	Process Module's
MRAM	Co, Fe, B, Ni Ta, Ti, Pt, Mn, Ru, Mg, Ir, Al, Metal Oxides	<ul style="list-style-type: none"> <li>Low temp processing (&lt;200C)</li> <li>Nobel Etch and Cleans</li> <li>AlCu Interconnect</li> <li>Interconnect with CMOS</li> <li>Materials Integration</li> <li>CMP</li> <li>Hardmask and Liner Integration</li> <li>Pattern Shrink</li> </ul>
PCRAM	Ag, GeS2, GST (Ge, Sb, Te)	
ReRAM	Zr, Pr, Ca, Y, Pd, La, Complex Metal Oxides	
FeRAM	PZT (Pb, Zr, Ti, O), SBT (Sr, Bi, Ta, O), BLT (Bi, La, Ti, O)	
NRAM	CNT, W	
SQC	Nb/AIOx/Nb, TiPt	

## How to deal with a Variety of Novel Materials

Many Variation in Materials and Thicknesses,  
not one Etch Solution that fits all applications

#### Memory Devices

Materials	Thickness (A)
Ta	100 - 500A
CoFeB	30A
MgO	15A
Ru	10A – 60A
CoFe	40A
PtMn	125A
GST	500A
Ag	--
SiO <sub>2</sub>	20 - 500A
HfO <sub>x</sub>	20 - 500A
Al <sub>2</sub> O <sub>3</sub>	20 - 500A
TiN	20 - 500A
SiGe	500 – 2kA

#### Life Sciences

Materials	Thickness (A)
Ta	50A
Ru	10A - 20A
NiFe	20A
CoFe	475A
TiN	1kA
a-Si	2kA
AlOx	50A

μWells

#### MEMS

Materials	Thickness (A)
Co	500A
CoNi	600A
Ni	1000A
NiFe	500A
Al	10kA
SiGe, Ge	2kA
Ru	500A

Magnetic Stack

#### Miscellaneous

Materials	Thickness (A)
Pt	1000A
PZT	Up to 2.2um
Nb	3kA

4k Metal Thk

## Etching of Novel Materials



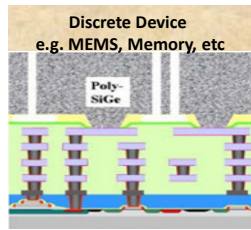
	LAM 9600	AMAT DPS2	Tegal 6540 *	Veeco Ion Mill
Gases Available	Chamber A (60C): BCl <sub>3</sub> , Cl <sub>2</sub> , Ar, N <sub>2</sub> , O <sub>2</sub> , SF <sub>6</sub> , He, O <sub>2</sub>  Chamber B (250C): DSQ O <sub>2</sub> , H <sub>2</sub> O	Chamber A (250C): BCl <sub>3</sub> , Cl <sub>2</sub> , Ar  Chamber B (65C): CF <sub>4</sub> , HeO <sub>2</sub> , HBr, Cl <sub>2</sub>	HRe 2.1 (30-80C): BCl <sub>3</sub> , Cl <sub>2</sub> , CHF <sub>3</sub> , CF <sub>4</sub> , Ar, O <sub>2</sub>  HRe 4.0 (170-350C): CO, Cl <sub>2</sub> , NH <sub>3</sub> , CF <sub>4</sub> , Ar, O <sub>2</sub>	Single Chamber: Ar
Materials Etched (Examples)	Al, TiN/Al/Ti, TiW/TiAl, GST, Ru, Nb, Al <sub>2</sub> O <sub>3</sub>	Chamber A: High-k, Al <sub>2</sub> O <sub>3</sub> , TiN, TaN, Ru, Zr,  Chamber B: Metal Gate Stacks - Poly & metal alloys	HRe 2.1: Oxide, Ti, TiN, W, Ta, GST  HRe 4.0: Ti, TiN, Nb, Pt, AlO <sub>x</sub> , Ta, PtMn, CoFe, MgO, Ru, Ag	Oxide, Ti, TiN, W, Ag, CoFe, Ni, Mg

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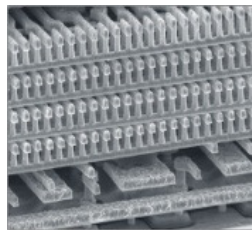
\* In storage



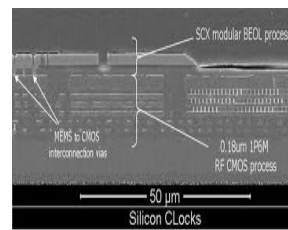
## Novel Device Integration on CMOS Substrates



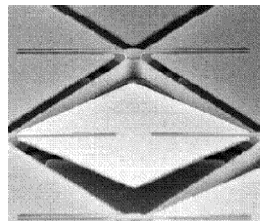
*Monolithic integration of Discrete Devices and CMOS*



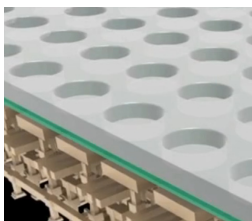
*3-D Memory: Courtesy Sandisk*



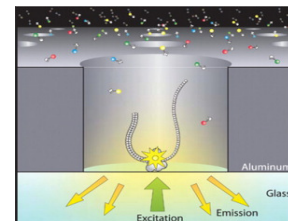
*MEMS Resonator courtesy of Silicon Clocks*



*Micro-Mirrors over CMOS courtesy of Spatial Photonics*



*Lab-on-a-chip integrates microfluidic sensors courtesy of Ion Torrent*



*Lab-on-a-chip integrates microfluidic sensors courtesy of Pacific Biosciences*

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## Integration of Novel Devices from 3<sup>rd</sup> party Foundry's

**Build Devices on CMOS**

*W Plug Interconnect to Cu*

Customer	Foundry	Technology
A	TSMC, SMIC	Memory
B	Novati	Memory
C	TSMC	Life Sciences
D	Tower Jazz	RF MEMS
E	Cypress	Life Sciences
F	Vendor C	Memory

*Enabling interconnect to CMOS Foundry wafers to integrate novel devices; enables secure split processing i.e.. Novati and Cypress Trusted Fabs*

## Alignment to 3<sup>rd</sup> party Foundry Wafers

- Foundry wafers arriving at TSI have a wide range of variations
  - Nikon Litho → ASML, Canon, model types, lens NA, substrate, etc.
  - Challenge is to integrate the differences incoming TSI lithography equipment

**Scanner Manufacturer**

**FIA Field Image Alignment**

**Placement rule for LSA and FIA**

- for Y alignment block rotate 90degree
- ▭ for X alignment

Put on edge of the shot near center

**Wafer Rotational Adjustments**

**3<sup>rd</sup> Party Alignment Marks**

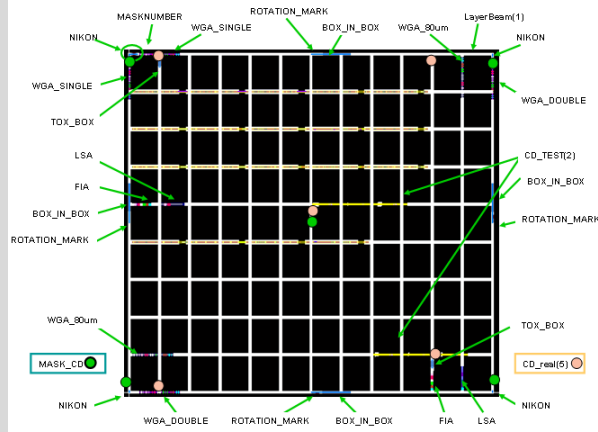
**Box in Box Alignments**



## Methodology to Support 3<sup>rd</sup> party Foundry Wafers

### Checklists & Recommendations:

- ✓ WGA triple (internal)
- ✓ WGA double and single (external)
- ✓ FIA
- ✓ LSA
- ✓ Box in Box
- ✓ Rotation Mark (Optional)
- ✓ CD bars scribe
- ✓ TOX/MRH (Optional)
- ✓ Corner marks and Nikon crosses (Optional)
- ✓ Mask number (Optional)
- ✓ MASK\_CD
- ✓ PCMs (Optional)
- ✓ Scribe Fill (Optional)
- ✓ Layer Beam (Optional)



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## Case Studies on Foundry Development Collaborations

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## UC Berkeley and Stanford Web-site/Press Release

you are here: → home → news center → press releases → berkeley and stanford launch nanofabrication partnership with tsi semiconductors

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**Berkeley and Stanford launch nanofabrication partnership with TSI Semiconductors**

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### Berkeley and Stanford launch nanofabrication partnership with TSI Semiconductors


College of Engineering | August 15, 2013

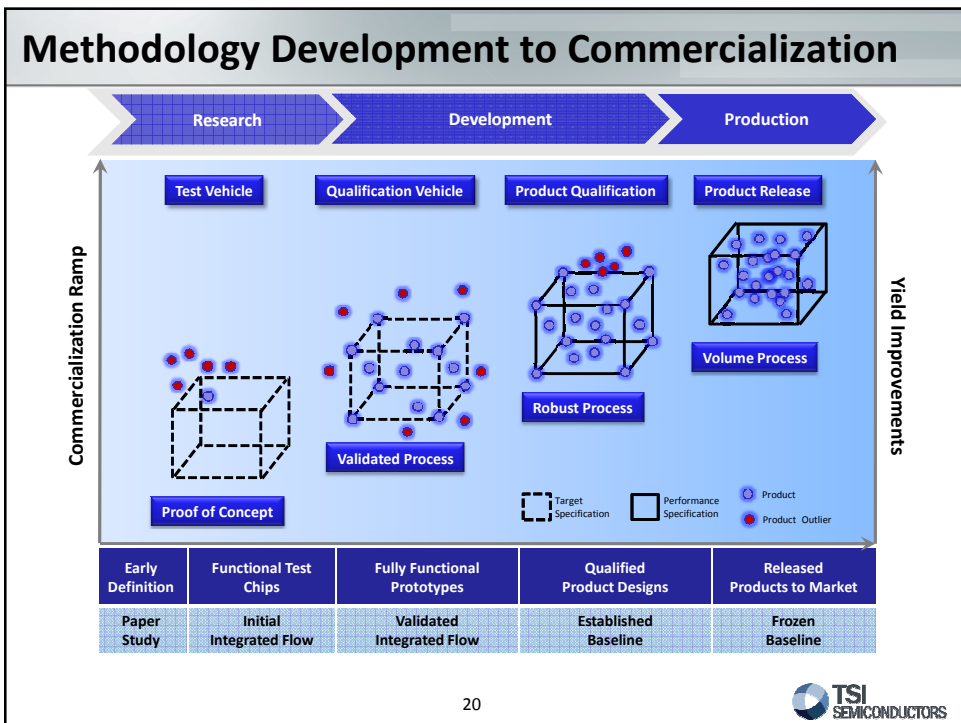
**BERKELEY** – The College of Engineering at the University of California, Berkeley today announced that its Marvell Nanofabrication Laboratory, along with Stanford University's Nanofabrication Facility, has initiated a virtual technology transfer exercise with TSI Semiconductors, LLC, a specialty foundry offering flexible technology development and advanced manufacturing solutions for projects ranging from the smallest to very large lot sizes.

The technology transfer exercise will be conducted with TSI's research and development organization, Technology Development & Commercialization Services (TDCS), at the firm's corporate headquarters in Roseville, CA. TDCS provides dedicated fabrication equipment to enable clients to manage their own development activities.

The Berkeley and Stanford laboratories and TDCS are mapping a large range of fabrication requirements to process technologies available at their facilities so that start-up companies can efficiently translate their proof-of-concept prototypes into production-approved process flows.

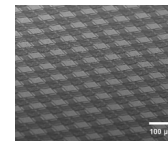
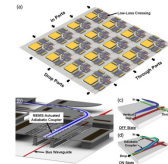






# Photonics Waveguide Technology

- **Business Model**
  - Jointly Develop leading edge Photonic MEMS Switch
  - Requires need for process innovation, commercialization in a Foundry Facility
- **POC - University California Berkeley**
  - Integrate multi-state Photonics project with TSI
  - Small scale lab on 6 inch wafer pieces
- **Commercialization - TDCS**
  - Development and Fabrication to integrate into CMOS into 200mm Processes
  - Develop process library for commercialization
- **Production – Still in Development**
  - Completed stage 1 passive components
  - Working on development & integration for stage 2 active components

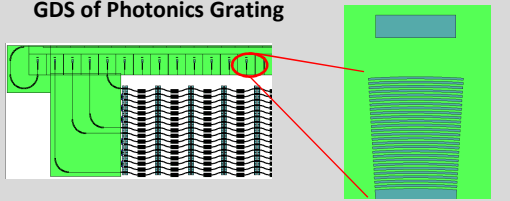


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# UCB Photonics Project – Stage 1

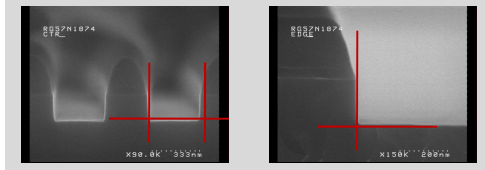
GDS of Photonics Grating



Poor Profile



Improved Profile



Process Improvements

- ✓ Lithography Exposure
- ✓ Etch Characterization
- ✓ Line Edge Roughness Improvements

Parameters	UCB	Foundry A	Foundry B	Foundry C	TSI
Lithography	248DUV	193nm	193nm	248DUV	248 DUV
Wafer Size (mm)	150	300	300	200	200
Wave Guide Loss	5db/cm	0.5dm/cm	0.1db/cm	1db/cm	<1.0db/cm





**TS16949:2009**



**ISO9001:2008**

## Leveraging Certifications



**Trusted**




**ITAR**

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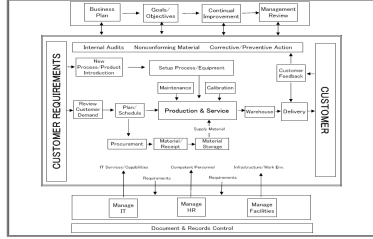
## Certification and Compliance

- TS16949:2009 – certification applies for the design & development, production, installation and servicing of automotive related products
  - This was prepared by the International Automotive Task Force (IATF) and ISO technical committee
  - Attributes for AEC-Q100 (Automotive Electronics Council)
- ISO9000 – Quality Management Systems
- ISO14001 – Environmental Management Systems
- DMEA Accreditation of Trusted Facility
- ITAR Certified in Electronics category

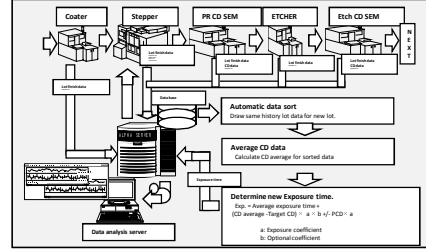


# Quality Business Process Management Systems

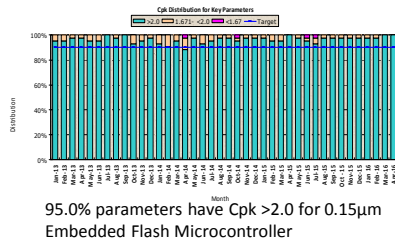
## QMS Process – TS16949:2009



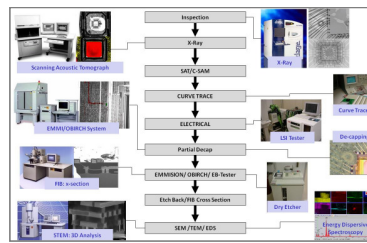
## Advanced Process Control (APC)



## Cpk Trend - Critical Nodes & Process



## On-Site Failure Analysis Protocols



# TSI Stress Test Qual for IC's – Partial Lists

Test Conditions	Type	TSI16949/AEC-Q100	Mil Guidelines
Reliability & Quality Tests (partial list)	TDDDB	✓	✓
	Hot Carrier Injection	✓	✓
	Negative Bias Temp Instability	✓	✓
	Electromigration	✓	✓
	Stress Migration	✓	✓
	ESD	✓	✓
	Latch-Up	✓	✓
	Electrothermally Induced Gate Leakage	Customer Request	✓
	Soft Error rate	✓ Sort	✓
	Process Avg Tests	✓ Sort/FT	✓
	Stat Bin/Yield Analysis	✓ Sort/FT	✓
	*Radiation Hardness	Customer request	✓

\* In progress by Design with Customer



## Summary

- TSI is positioned as a US-based specialty foundry with a technology platform supporting industrial, automotive, Mil-Aero and medical markets
- We are also positioned to provide a development service (TDCS) for innovative and disruptive materials development not found in typical Production Foundry Fabrications
- Customer IP is safe and secure – Trusted, ITAR Certified
- We are based in Northern CA location, close to tech eco-system
- Our services business model and collaboration enables faster and cost effective time to market for these technologies

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## Thank You

**Wilbur Catabay**  
SVP TDCS & Corporate Strategy  
TSI Semiconductors Corporation

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