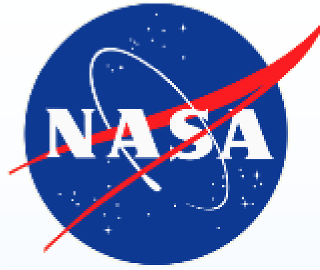

DDR Memories

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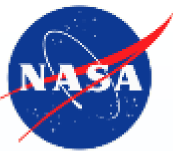
Double Data Rate (DDR)

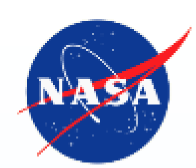


Acronyms

Acronym	Definition
1MB	1 Megabit
3D	Three Dimensional
3DIC	Three Dimensional Integrated Circuits
AC	Alternating Current
AEC	Automotive Electronics Council
AES	Advanced Encryption Standard
AF	Air Force
AFRL	Air Force Research Laboratory
AFSMC	Air Force Space and Missile Systems Center
AMS	Agile Mixed Signal
ARM	ARM Holdings Public Limited Company
BGA	Ball Grid Array
BOK	Body of Knowledge
CAN	Controller Area Network
CBRAM	Conductive Bridging Random Access Memory
CCI	Correct Coding Initiative
CGA	Column Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CN	Xilinx ceramic flip-chip (CF and CN) packages are ceramic column grid array (CCGA) packages
COTS	Commercial Off The Shelf
CRC	Cyclic Redundancy Check
CRÈME	Cosmic Ray Effects on Micro Electronics
CRÈME MC	Cosmic Ray Effects on Micro Electronics Monte Carlo
CSE	Crypto Security Engine
CU	Control Unit
DC	Direct Current
D-Cache	defered cache
DCU	Distributed Control Unit
DDR	Double Data Rate (DDR3 = Generation 3; DDR4 = Generation 4)
DIMM	Dual Inline Memory Module
DLA	Defense Logistics Agency
DMA	Direct Memory Access
DMEA	Defense MicroElectronics Activity
DoD	Department of Defense
DOE	Department of Energy
DSP	Digital Signal Processing
dSPI	Dynamic Signal Processing Instrument
Dual Ch.	Dual Channel
DUT	Device Under Test
ECC	Error-Correcting Code
EEE	Electrical, Electronic, and Electromechanical
EMAC	Equipment Monitor And Control
EMIB	Multi-die Interconnect Bridge
ESA	European Space Agency
eTimers	Event Timers
ETW	Electronics Technology Workshop
FCCU	Fluidized Catalytic Cracking Unit
FeRAM	Ferroelectric Random Access Memory
FinFET	Fin Field Effect Transistor (the conducting channel is wrapped by a thin silicon "fin")
FPGA	Field Programmable Gate Array
FPU	Floating Point Unit
FY	Fiscal Year
Gb	Gigabyte
GCR	Galactic Cosmic Ray
GIC	Global Industry Classification

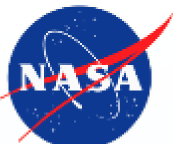
Acronym	Definition
GHz	Gigahertz
Gov't	Government
GPU	Graphics Processing Unit
GRC	NASA Glenn Research Center
GSFC	Goddard Space Flight Center
GSN	Goal Structured Notation
GTH/GTY	Transceiver Type
HALT	Highly Accelerated Life Test
HAST	Highly Accelerated Stress Test
HBM	High Bandwidth Memory
HDIO	High Density Digital Input/Output
HDR	High-Dynamic-Range
HiREV	High Reliability Virtual Electronics Center
HMC	Hybrid Memory Cube
HP Labs	Hewlett-Packard Laboratories
HPIO	High Performance Input/Output
HPS	High Pressure Sodium
HUPTI	Hampton University Proton Therapy Institute
I/F	interface
I/O	input/output
I2C	Inter-Integrated Circuit
i2MOS	Microsemi second generation of Rad-Hard MOSFET
IC	Integrated Circuit
JFAC	Joint Federated Assurance Center
JPL	Jet Propulsion Lab
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (FPGAs use JTAG to provide access to their programming debug/emulation functions)
KB	Kilobyte
L2 Cache	independent caches organized as a hierarchy (L1, L2, etc.)
L-mem	Long-Memory
LP	Low Power
LPDDR	Low Power Double Data Rate (Memory)
MBMA	Model-Based Missions Assurance
MGH	Massachusetts General Hospital
Mil/Aero	Military/Aerospace
MIPI	Mobile Industry Processor Interface
MMC	MultiMediaCard
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MP	Microprocessor
MP	Multiport
MPFE	Multiport Front-End
MPU	Microprocessor Unit
Msg	message
MT/s	Million Transfers per second
NAND	Negated AND or NOT AND
NASA	National Aeronautics and Space Administration
NASA GSFC	NASA Goddard Space Flight Center
NASA STMD	NASA's Space Technology Mission Directorate
Navy Crane	Naval Surface Warfare Center, Crane, Indiana
NEPP	NASA Electronic Parts and Packaging
NGSP	Next Generation Space Processor
NOR	Not OR logic gate

Acronym	Definition
NRL	Naval Research Laboratory
NRO	United States Navy National Reconnaissance Office
NSWC Crane	Naval Surface Warfare Center, Crane Division
NVM (NVMe)	Non Volatile Memory (Non Volatile Memory Express)
OCM	On-chip RAM
PBGA	Plastic Ball Grid Array
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCIe Gen2	Peripheral Component Interconnect Express Generation 2
PLL	Phase Locked Loop
POL	point of load
PoP	Package on Package
PPAP	Production Part Approval Process
Proc.	Processing
QDR	quad data rate
QFN	Quad Flat Pack No Lead
QSPI	Serial Quad Input/Output
R&D	Research and Development
R&M	Reliability and Maintainability
RAM	Random Access Memory
ReRAM	Resistive Random Access Memory
RGB	Red, Green, and Blue
RH	Radiation Hardened
ROM	Read Only Memory
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SD/eMMC	Secure Digital embedded MultiMediaCard
SD-HC	Secure Digital High Capacity
SDM	Spatial-Division-Multiplexing
SDRAM	Synchronous Dynamic Random Access Memory
SEE	Single Event Effect
SESI	secondary electrospray ionization
Si	Silicon
SiC	Silicon Carbide
SK Hynix	SK Hynix Semiconductor Company
SLU	Saint Louis University
SMDs	Selected Item Descriptions
SMMU	System Memory Management Unit
SNL	Sandia National Laboratories
SOA	Safe Operating Area
SOC	Systems on a Chip
SPI	Serial Peripheral Interface
STT	Spin Transfer Torque
TBD	To Be Determined
Temp	Temperature
THD+N	Total Harmonic Distortion Plus Noise
TID	Total Ionizing Dose
TRIUMF	Tri-University Meson Facility
T-Sensor	Temperature-Sensor
TSMC	Taiwan Semiconductor Manufacturing Company
U MD	University of Maryland
UART	Universal Asynchronous Receiver/Transmitter
UFHPTI	University of Florida Proton Health Therapy Institute
UltraRAM	Ultra Random Access Memory
USB	Universal Serial Bus
VNAND	Vertical NAND
WDT	Watchdog Timer



Outline

- What the technology is (and isn't)
- Our tasks and their purpose
- Collaborations
  - Roadmap
  - Partners
  - Results to date
  - Plans
- Comments



Technology

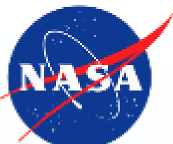
- **Double Data Rate (DDR) Memories**
  - **Memory transfer upon rising and falling edges of the clock signal - permits double the transfer rate without increasing the frequency of the clock signal**
  - **DDR Memories permit VERY large capacities and advanced error correction features**
  - **Flight computers boot from ROM, but tend to run from RAM**

Type	Acronym	Data rate	Prefetch buffer size
Synchronous Dynamic Random Access Memory	SDRAM	66-133 MT/s	1 bit
Double Data Rate SDRAM	DDR	266-400 MT/s	2 bits
Double Data Rate Two SDRAM	DDR2	533-800 MT/s	4 bits
Double Data Rate Three SDRAM	DDR3	800-1600 MT/s	8 bits
Double Data Rate Fourth SDRAM	DDR4	2133-3200 MT/s	8 bits

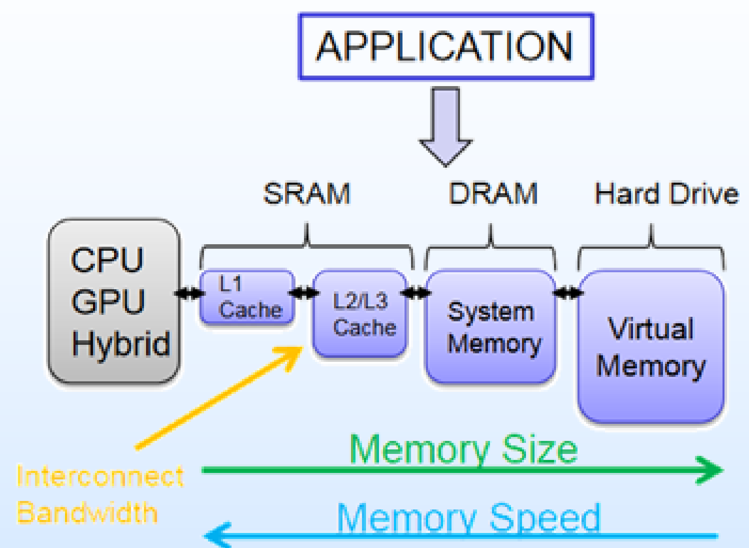
< 0.2 GHz

> 2.0 GHz

MT/S: million transfers per second



Purpose

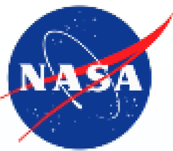


Mode	LPDDR1	LPDDR2	LPDDR3	LPDDR4
Data Rate	400Mbps	800Mbps	1600Mbps	**3200Mbps**
tCK	2.5ns	1.25ns	0.625ns	**0.3125ns**
Data eye area (Normalized)	14	1	0.5	0.09

Semicon West 2013: Minho Kim, SK Hynix, "High Performance & Low Power Memory Trends"

http://met-ri.lolipop.jp/SW2013_pdf_link/SW2013_TechXPOTs/08_GenerationMobile_ICPackaging/08_ICPackaging_presentation/SW2013_Minho%20Kim_SK%20Hynix.pdf

- **DDR DRAM devices are relatively low power compared to faster Static Random Access Memory (SRAM) while still being fast enough to provide high speed main memory or data buffering services**
- **Processor performance requirements are highly dependent on the application of the flight project, BUT is strongly dependent on the rate at which data can be accessed from memory**
- **Faster memories may lack the reliability required in flight projects**



DDR Roadmap

- collaborative with JPL, others

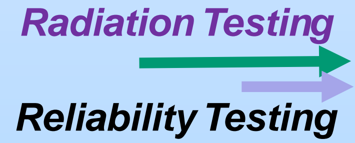
DDR2
- ISSI
- Hynix
- Samsung
- Micron

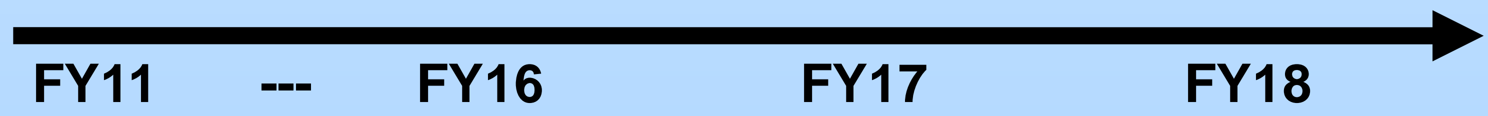
DDR3
- Intelligent Memories
- Hynix
- Samsung
- Micron 16nm

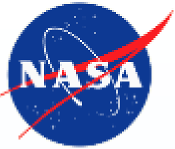
DDR4
- Samsung
- Micron

3D Memories
- DiRAM (Tezzaron)
- Optane (Intel)

(is also NVM)

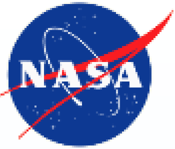






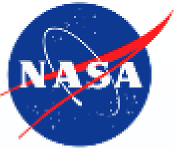
Partners

- JPL, Navy Crane and NASA GSFC have performed testing on DDR memories since FY11
- NASA GSFC has been working with Kozio, SimmTester and NXP to develop test capabilities
  - DC leakage current (idle, standby, read, write)
  - AC operations (bad blocks, pattern writing, erase)



Qualification Guidance

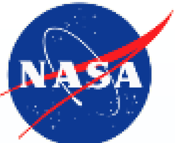
- Evaluate radiation tolerance and/or reliability of:
  - Highly scaled (i.e., large number of bits) memories, and,
  - New technology device technologies such as 3D memory, resistive, emerging magnetic, or carbon/graphene-based devices
    - As a minimum, samples must be on path to commercialization
    - We often work with manufacturers and other agencies when possible



Qualification Guidance (Cont'd)

- **Public documents**
  - Radiation effects presentations on DDR, DDR2 and DDR3 memories can be found radhome.gsfc.nasa.gov
  - NEPP DDR Device Reliability Reports (FY11 – 13) can be found on NASA Technical Reports Server (www.sti.nasa.gov)

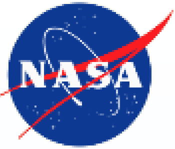
- **Future guidelines will be developed for this technology to include qualification, usage and test methods**



Results to Date

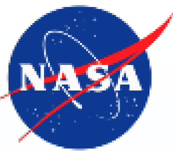
- **NEPP has conducted reliability, SEE and TID tests on DDR devices down to 16nm**

Manufacturer	SDRAM	DDR	DDR2	DDR3
ISSI	X	X	X	X
Micron		X	X	X
Samsung		X	X	X
Hynix		X	X	X
Intelligent Memory				X



Plans (w Schedule)

- A DDR4 tester is being planned as plug-n-play and is ready to proceed when funding is available
  - DDR4 DUTs are already commercially available
- Testing will traverse the same test vectors as previous DDR2 and DDR3 testing
  - Results will be appended to DDR work to date



FY17-18: DDR Testing

Description:

- This is a task over all device topologies and process.
- The intent is to determine inherent radiation tolerance and sensitivities,
- Identify challenges for future radiation hardening efforts,
- Investigate new failure modes and effects
- Testing includes total dose, single event (proton) and reliability. Test vehicles will include a variety of volatile memory devices as available

FY17-18 Plans:

- Prove out DDR4 test capability
- Probable test structures for TID and SEE:
  - Micron
  - Samsung
  - Hynix
- Tests:
  - characterization pre and post-rad

Schedule:

Microelectronics T&E	FY17				FY18							
	M	J	J	A	S	O	N	D	J	F	M	A
On-going discussions for test samples	■	■	■	■	■	■	■	■	■	■	■	■
DDR4 Tester Development	■	◇	■	■								
TID Testing					◇	■	■	◇	■	■	■	
SEE Testing					■	■	■	■	■	■	■	
Analysis and Comparison						■	■	■	■	■	■	◇

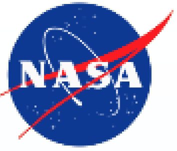
PIs: GSFC/Lentech/Wyrwas

Deliverables:

- Test reports and quarterly reports
- Expected submissions for publications

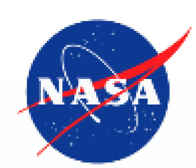
NASA and Non-NASA Organizations/Procurements:

- Source procurements: TID (GSFC), Proton



Comments

- DIMM testing is the most cost effective way to procure 100s of DUTs
- A build out of new equipment is necessary to carry out assessments on DDR4
- Ready-to-go as soon as DUTs are procured (and facility availability)
  - Decapsulation for SEE test preparation (2-week turn)
  - As-received DUTs can be TID tested



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