PBGA & QFN
FCBGA/3D Stack TC/TSC Evaluation

by

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http://nepp.nasa.gov
PBGA & QFN

- PBGA TC Evaluation
  - Numerous BGA packages
  - WLP assembly challenge
  - Standard 3D stack
  - High I/O flip chip BGA, 2.5D (passive interposer)
  - Accelerated testing/failure mechanisms
  - PCB finish effect

- QFN evaluation
  - Various QFN package sizes
  - Effect of conformal coating
  - Accelerated TSC/TC testing

- TMV/2.5D/TSV
  - TMV test vehicle and build
  - Interposer 2.5D test vehicle build
  - TSV daisy-chain test approach
Best Practices and Guidelines
• Test, usage, screening, qualification
• Radiation facility studies

Guideline with Test Results NEPP Website

NEPP – Product Delivery

NASA EEE Parts Policy and Standards
Government and Industry Standards
Representation
• SAE G11/G17
• JEDC/JPC
• Aerospace TORs

Assurance

NEPP Standard Products
• Test, summary, and audit reports
• Conference and workshop presentations
• Alerts

Related task areas:
Technology/parts evaluations lead to new best practices, etc...

NEPP – Memories

New materials/architectures
• Resistive
• High/low density
• Spin torques transfer magnetoresistive
• Antiferromagnets and spin
• Intel Ceramic
• Enabling ”universal” memories

ORAMs
• Displays/technology (in progress)
• Components ECM (future)
• Processors/CAM (future)

Related task areas:
Deprocessing for single event testing (also w/processors, FPGAs, ...)

NEPP – Processors, Systems on a Chip (SOC), and Field Programmable Gate Arrays (FPGAs)

State of the Art COTS Processes
• TSMC CMOS 90, 45, 32, 22
• IBM, Inari, AMD

“Space” FPGAs
• Microsemi/MIO
• VME/MIO
• ALI/Brea/Alti
• Taiwan/FPGAs

COTS FPGAs
• V蒂亞納
• Megatech
• TSC Microelectronics

Potential future task areas:
adversarial intelligence (AI) hardware, Intel Stratix 10

Best Practices and Guidelines

• Test, usage, screening, qualification
• Radiation facility studies

Realizing Sleep in a Nanoscale World: A Review

Reza Ghaffarian/JPL/Caltech
Best Practices and Guidelines
- Test, usage, screening, qualification
- Radiation facility studies

BOK
- Technology and product status and gap analysis

NEPP TC Reliability

NEPP ETW-2017
Guideline Test Results
NEW NEPP TASK
Outline

• Reliability
  • FCBGA/PBGA/WLP
  • 3D stack

• PCB Finish
  • HASL for SnPb
  • ENEPIG for WLP and FPGA

• Reliability Results
  • 200 Thermal cycles
  • 200 Thermal shock cycles
  • X-ray, optical & X-section/SEM images

• Summary
- Designed test matrix
- Select high I/O PBGA/FCBGAs and FPGA & 3D stack daisy-chain package for solder joint reliability and monitoring
- Selected two PCB finish (HASL/ENEPIC) with traces either on top or one layer under with microvia interconnections
- Successfully assembled TVs both single- and double-sided
- Performed QA evaluation followed by reliability testing
- Performed 200 TC (-55°C/100°C) or 200TSC (-65°C/150°C)
- PBGA pitch from 0.4 mm to 1.27 mm
- 3D stack, 1mm pitch
- WLP, 1600 balls, 0.3 mm pitch
SnPb or SAC on ENEPIG

A PCB with “corrosion spikes” on Ni layer. The IMC layer spalled off.
Tegehall-ESA

ENEPIG/SnPb is NOT recommended for high T use.
Milad-Uyemura

Growth Rate of IMCs
Sn-37Pb > Sn-3.0Ag-0.5Cu
3D Stack
Single-sided
3D Stack
Double-sided
X-ray FCBGA 1924 I/O
3D Stack
200TC (-55°C/100°C)
FCBGA 1924
200 TSC(-65°C/150°C)

SN11 ENEPIG
SN11 Back

SN12 HASL
SN12 Back

NEPP ETW- 2017
X-ray
FCBGA
1924

SN11
ENEPIG

SN12
HASL
FCBGA 1924 on ENEPIG 200 TS (-65/150°C)
FCBGA 1924 on HASL
200 TSC (-65°C/150°C)

No defective solder connections were found.
SEM/EDS
FCBGA
1924
ENEPIG
HASL

NEPP ETW- 2017
Summary

- Released NEPP report
  - [https://nepp.nasa.gov/](https://nepp.nasa.gov/)
  - Evaluated FCBGA, FPBGA, 3D Stack, and more
  - PCB finish
    - HASL/ENEPIG

- 3D Stack/FPBGA1924
  - 200 TC (-55°C/125°C) on ENEPIG
    - No failures of 3D stack/FCBGA
  - 200 TSC (-65°C/150°C)
    - No failure of FCBGA 1924
    - Failure of FPBGA from package sites

- Evaluate further when funded
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http://nepp.nasa.gov

Thank You!