Advanced Packaging Technologies

Under Various Thermal Cycles

by

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Jet Propulsion Laboratory
National Aeronautics & Space Administration
California Institute of Technology

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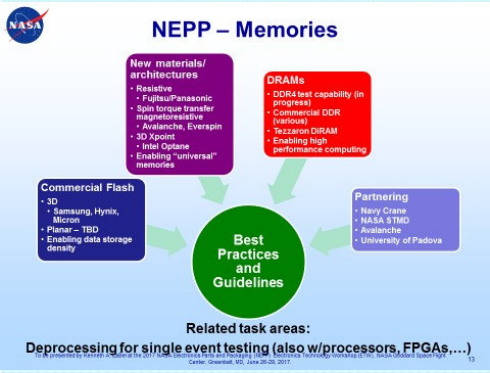
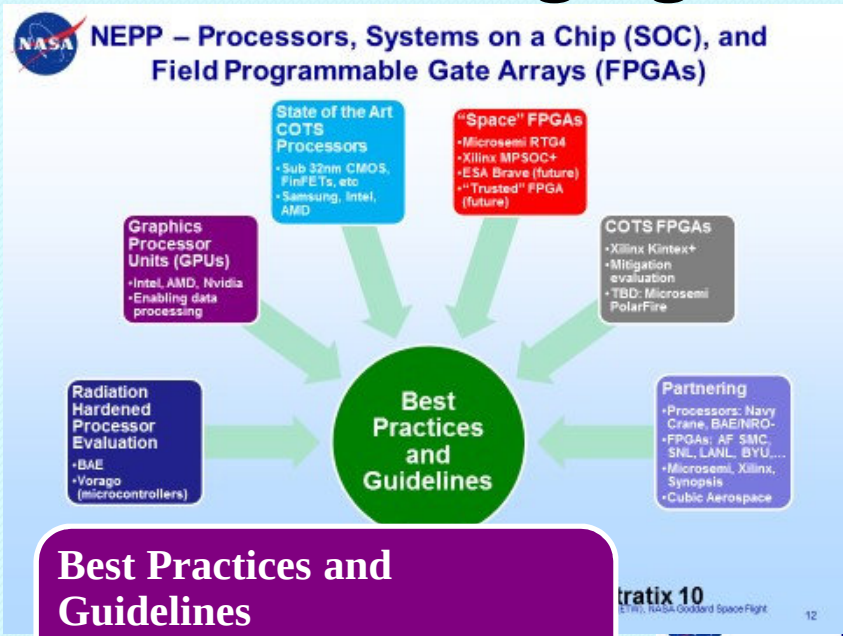
http://nepp.nasa.gov

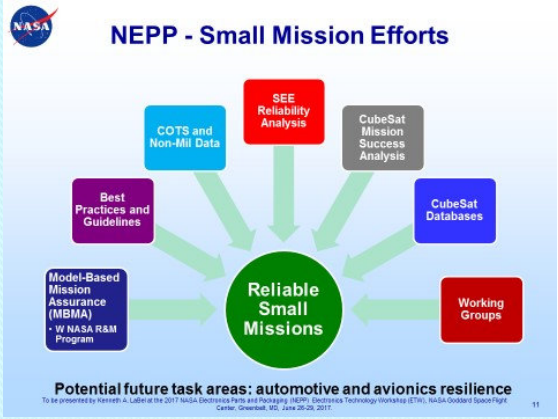
Outline

- Advanced Packaging Technologies
  - NEPP Tasks: FCBGA/TMV/WLP/TSV
  - Standard &WLP to Fan-out WLP (FO-WLP)
- Reliability under thermal stress
  - Creep/fatigue thermal stresses and combined stresses
- TC Reliability for Advanced Single Package
  - Test vehicle and advanced array packages
  - FCBGA1924 behavior under TC
  - FPBGA evaluation after TC
- TMV/2.5D (SiP)/3D/WLP TSV Evaluation
  - 3D memory TC evaluation
  - TMV test vehicle build and TC evaluation
  - System in package (SiP) and TC evaluation
  - WLP test vehicle design (FOWLP and 3D TSV)
- Summary

FCBGA/TMV/TSV Packaging Technologies







Best Practices and Guidelines

- Test, usage, screening, qualification
- Radiation facility studies

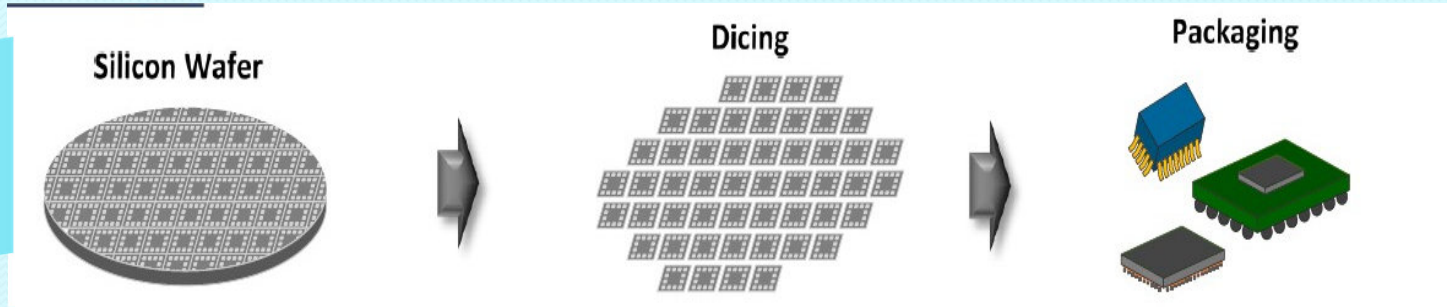
BOK

- Technology and product status and gap analysis

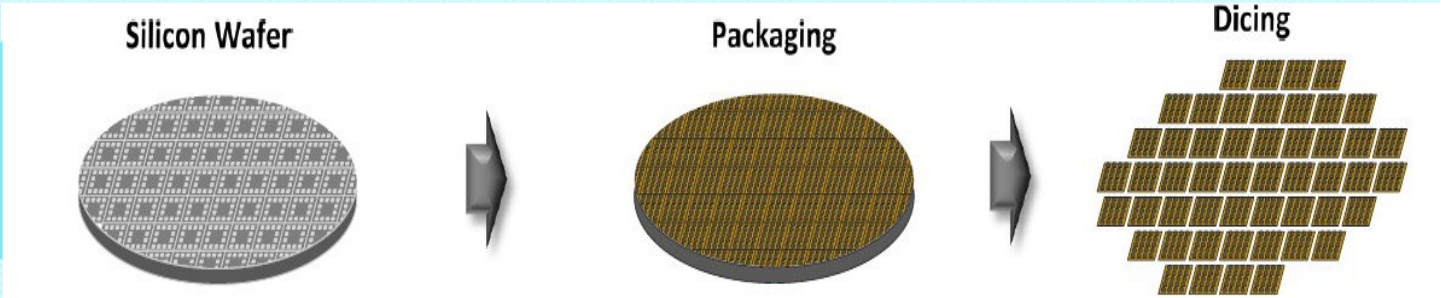
Test Results & BOK Guidelines NEPP Website

Standard to FO-WLP Packaging Technologies

Standard Packaging



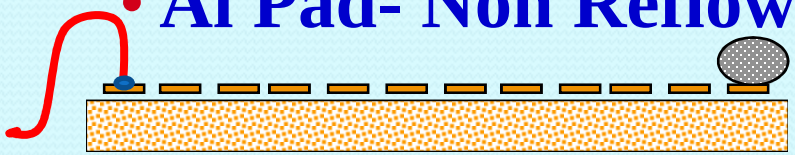
WLP Packaging



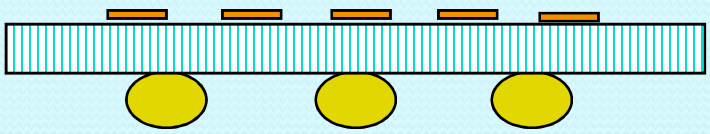
Fan-Out WLP

Packaging Concept

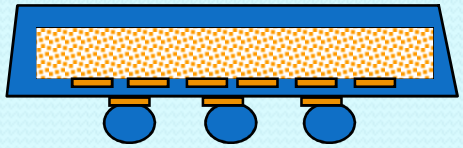
- Chip node ~ 14 nm
- Die pitch ~ 150 µm
- Al Pad- Non Reflow



- Interposer
  - Polymer, Ceramic, Flex
  - Cu:Ni:Au Pad

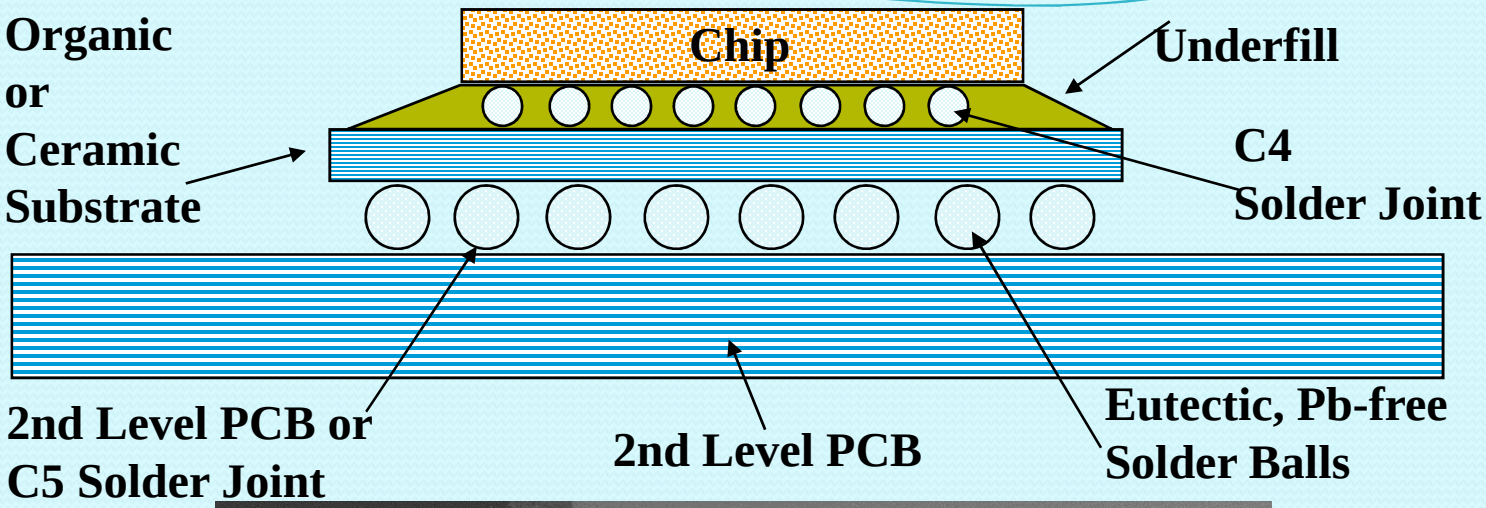


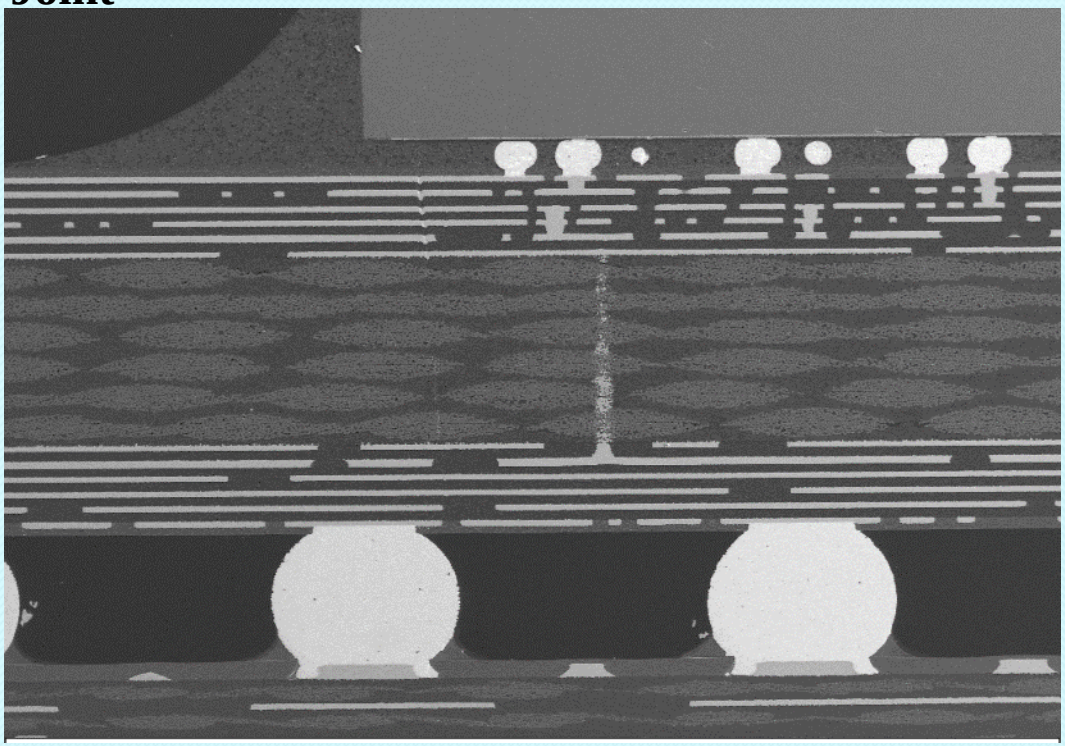
- Wafer
  - Pitch limitation
  - Mold & Fan-out



- Norm pitch for PCB (> 0.3 mm)

Flip Chip BGA (FCBGA)





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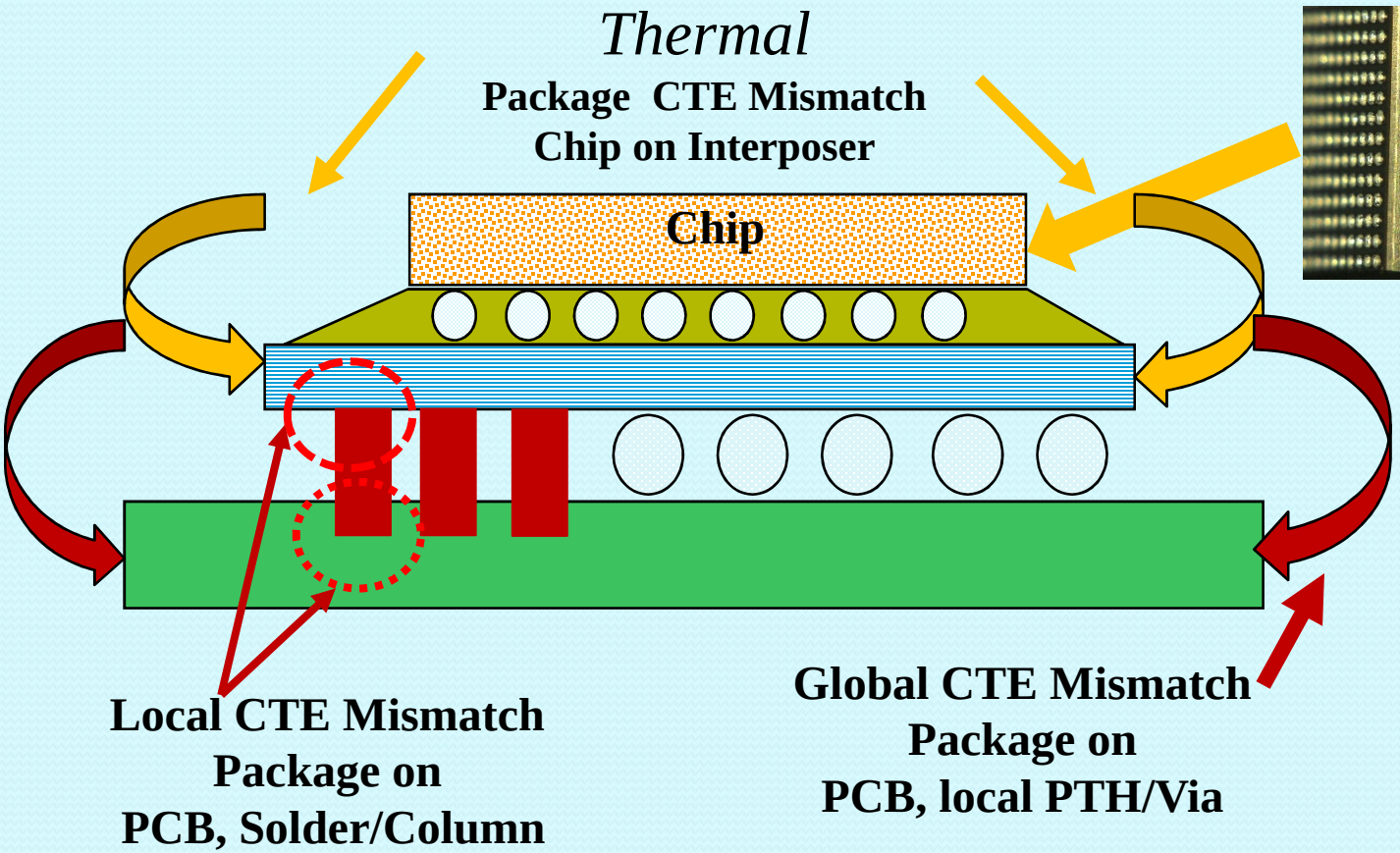
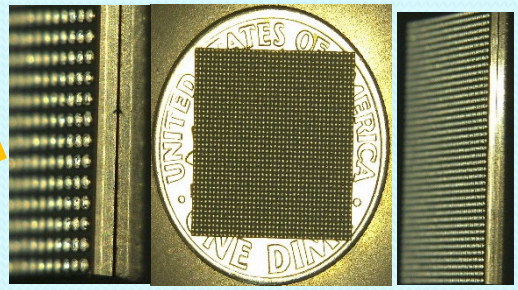
Packaging Reliability Under Thermal Stress





WLP
Fan Out WLP

$$\Delta D = (\alpha_c - \alpha_s)(T_c - T_0)\, L_D/H$$

Fatigue Models Under TC

$$N_f(50\%) = \frac{1}{2}\left[\frac{2\varepsilon'_f}{\Delta D}\right]^m$$

$$\Delta D = (\alpha_c - \alpha_s)(T_c - T_0)\, L_D/H$$

Appears to be simple!

W/O

Physics of Failure (PoF)

Model: Semi-analytical, Semi-empirical

New Approach $\mathbf{N_f \sim W^c}$

Engelmaier-Wild Model

Accel TC for Solder

$$\Delta D = \Delta\alpha \quad \Delta T \quad LD/H$$

$\Delta T =$ 0℃ to 100℃	***Creep (time dependent)***
$\Delta T =$ -55℃ to 100℃	Creep + Fatigue
$\Delta T =$ -55℃ to 125℃	Excess creep + Fatigue
$\Delta T =$ -65℃ to 150℃	Excess creep + Fatigue
$\Delta T =$ -120℃ to 85℃	Mild creep + Excess Fatigue
$\Delta T =$ -196℃ to 25℃	***Low creep + Excess Fatigue***

Note: New failure mechanisms when extreme hot/cold

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Synergism TC+ Mech

ΔT + Vib + ΔT	for CBGA/CGA/PBGA
ΔT + Drop + ΔT	for CGA/FCBGA
Vibration at cold/hot	for FPBGA/FCBGA/QFN
Vibration at hot	for FPBGA/FCBGA
Vibration with ΔT	for FPBGA/FCBGA

T-V Sequence

$$CDI = \left(\frac{n_T}{N_T}\right)^{0.47} + \left(\frac{n_V}{N_V}\right)^{0.70}$$

V-T Sequence

$$CDI = \left(\frac{n_T}{N_T}\right)^{0.91} + \left(\frac{n_V}{N_V}\right)^{0.93}$$

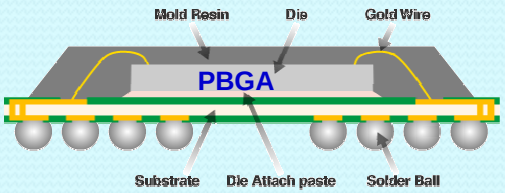
A. Perkins: Solder Joint Reliability Prediction for Multiple Environments

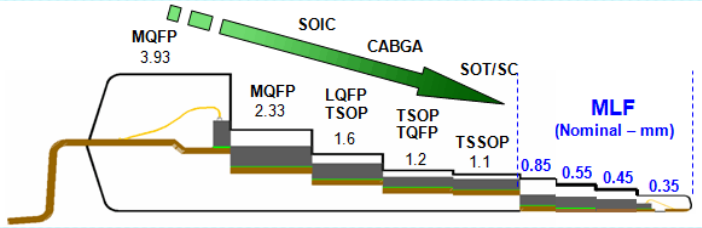
Standard Single Chip Packaging

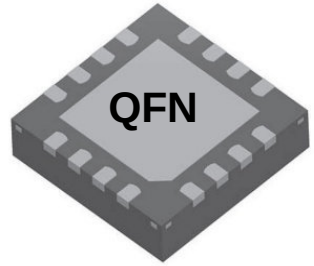
PBGA/SOC
QFN/MLF

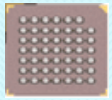
Wire bond to Flip Chip
CBGA to CCGA

CSP / WLP
a/M/W-
QFN/LGA



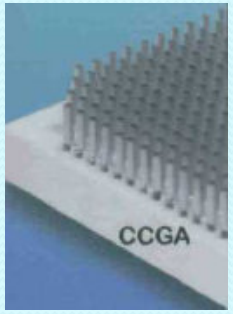


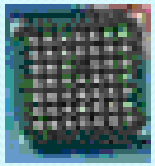




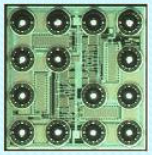
CBGA

2116 FCBGA
ASIC

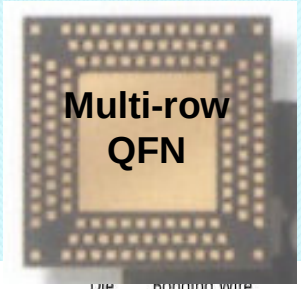


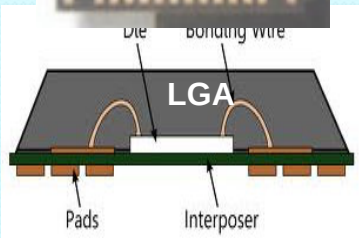


Chip Scale
Packaging
(CSP)



Wafer
Level
Packaging





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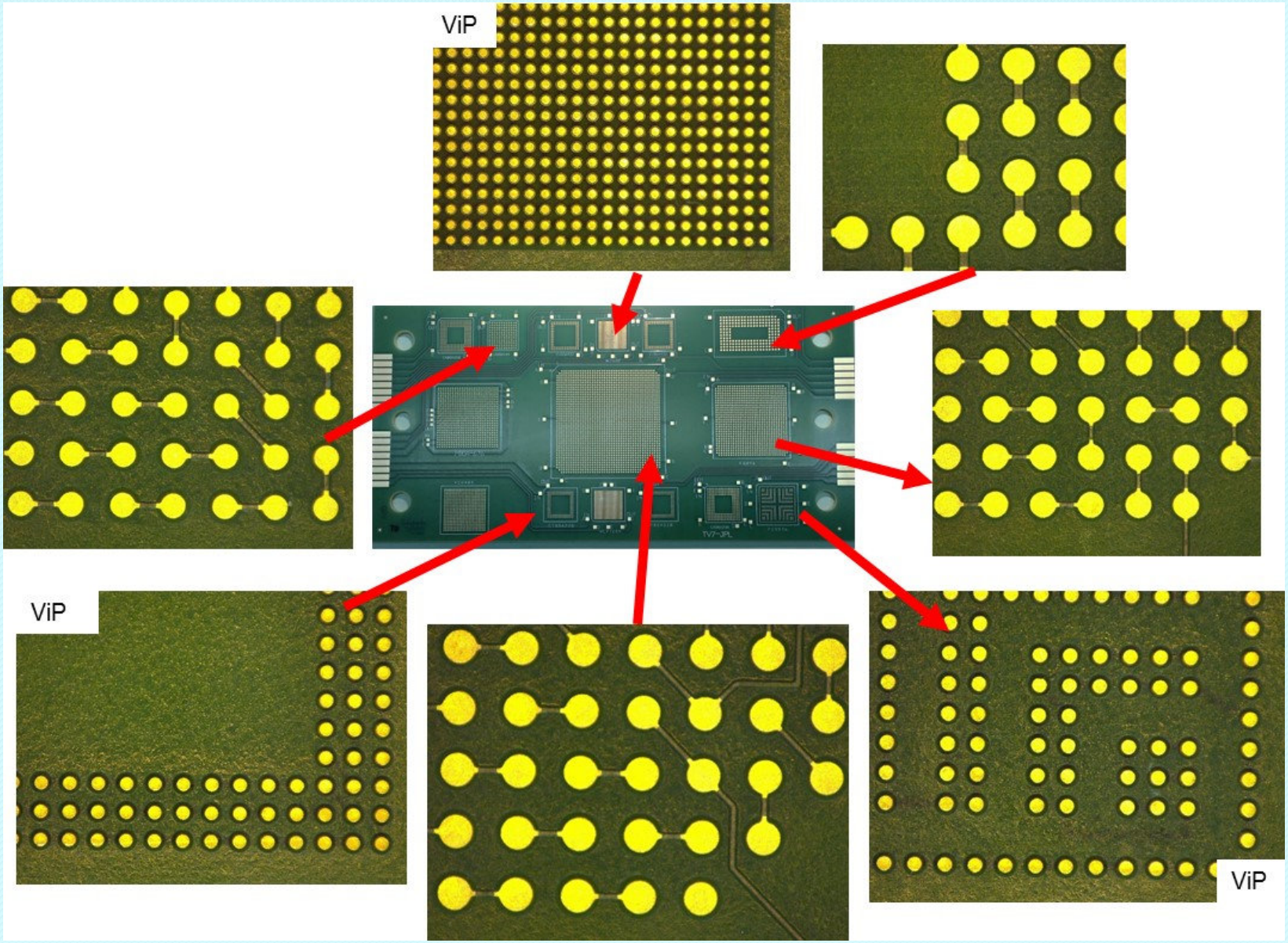
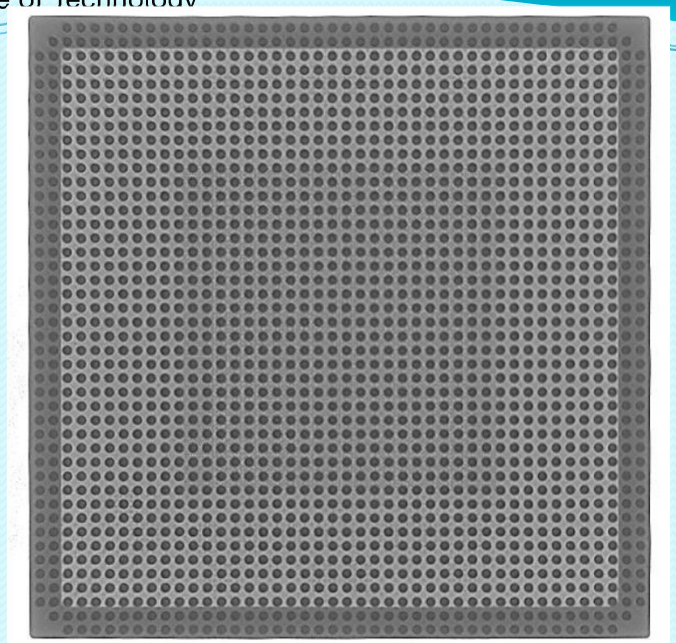
TC of Standard Packages

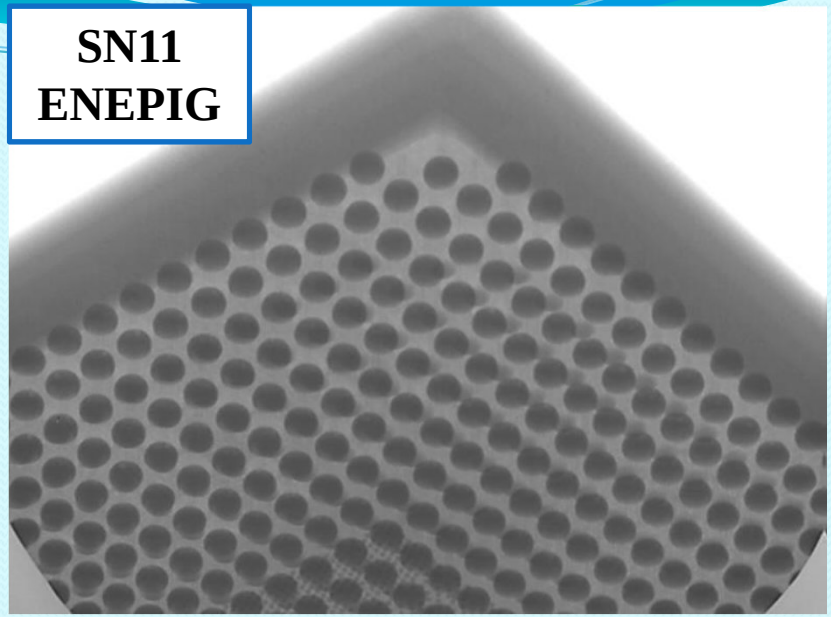


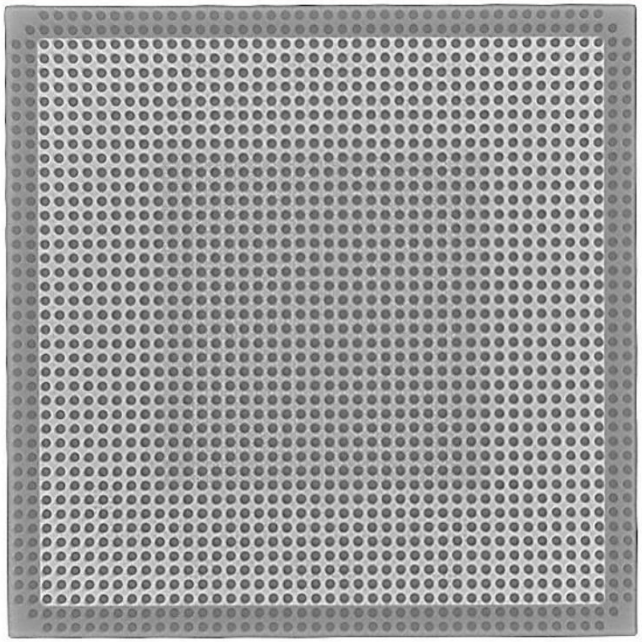
FCBGA/PBGA & more

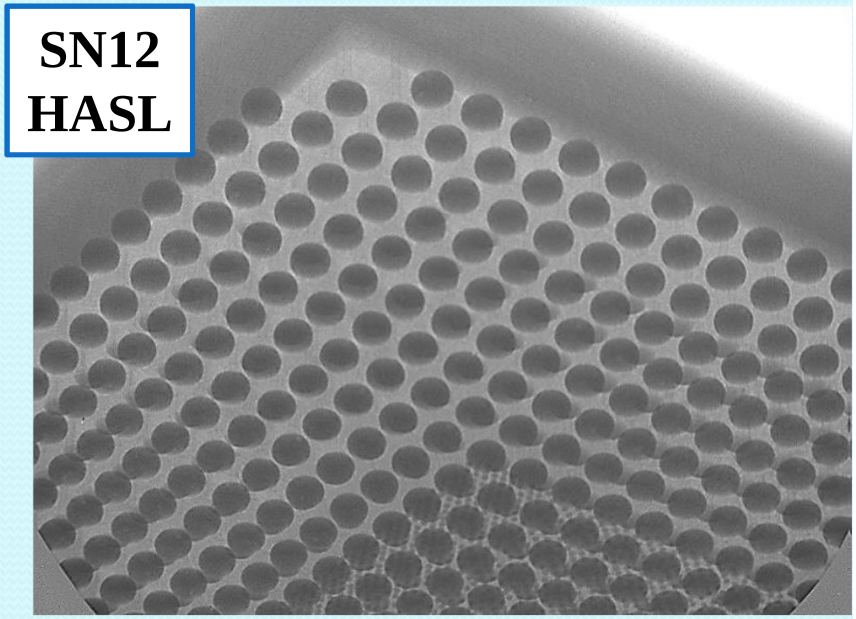
- Test matrix covered numerous standard packaging technologies
- FCBGA, FPBGAs, PBGAs daisy-chain package for TC reliability
- Two PCB finish (HASL/ENEPIG) W/WO Microvia
- Most single-side, one double-side mirror image
- TC= (-55°C/100°C), TC = (-55°C/125°C)
- TSC (-65°C/150°C)

X-ray FCBGA 1924









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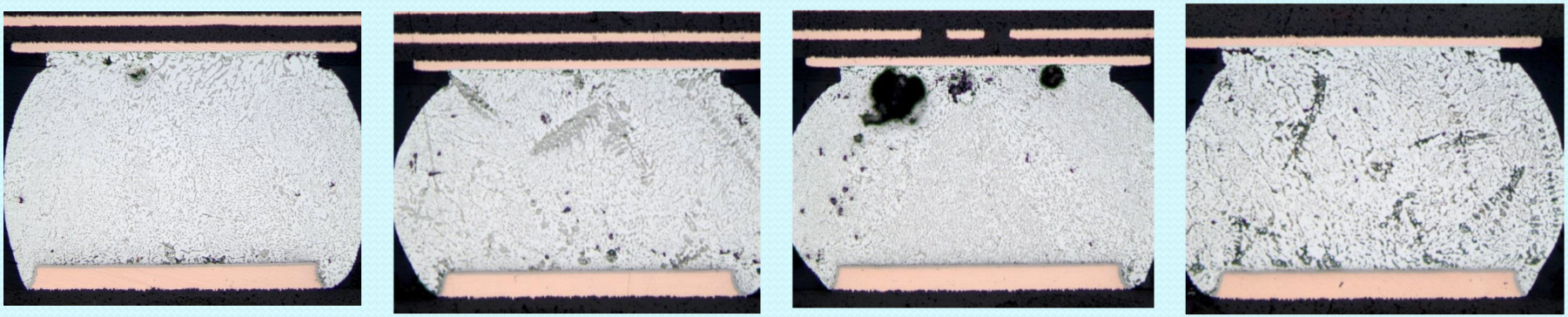
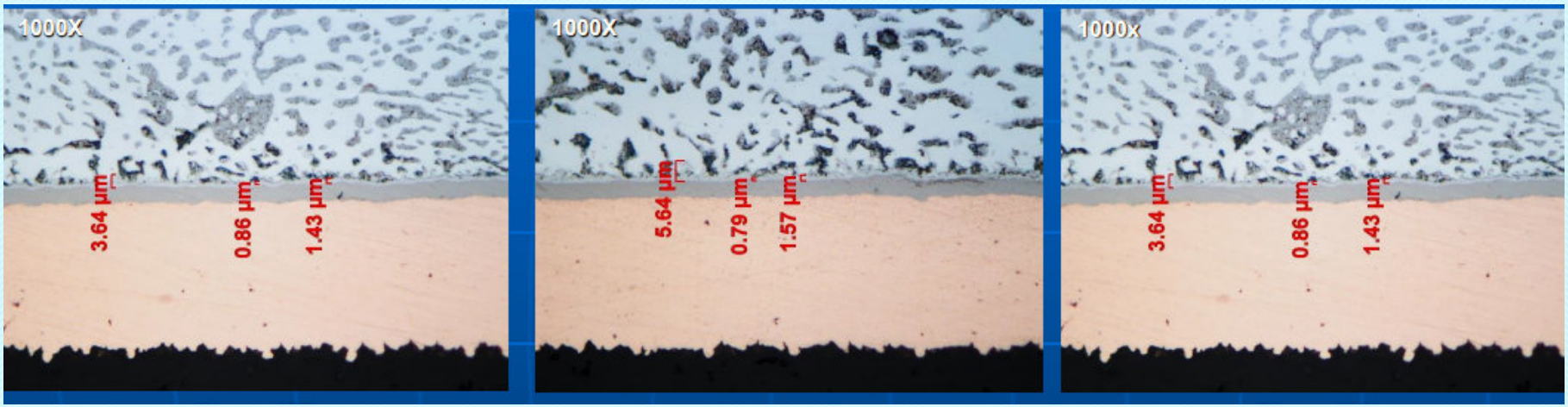
FCBGA 1924 on ENEPIG
200 TSC (-65°C/150°C)





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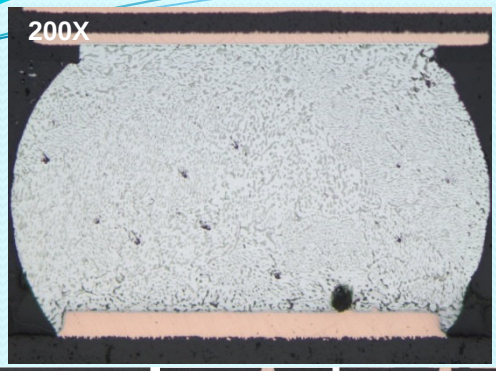
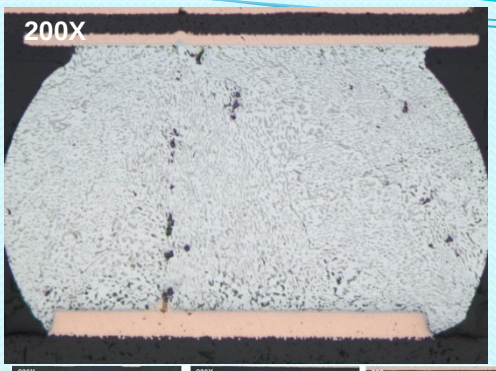
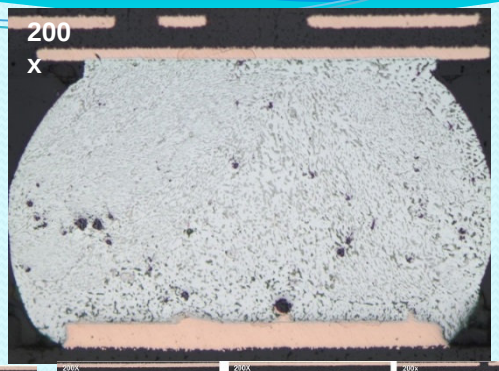
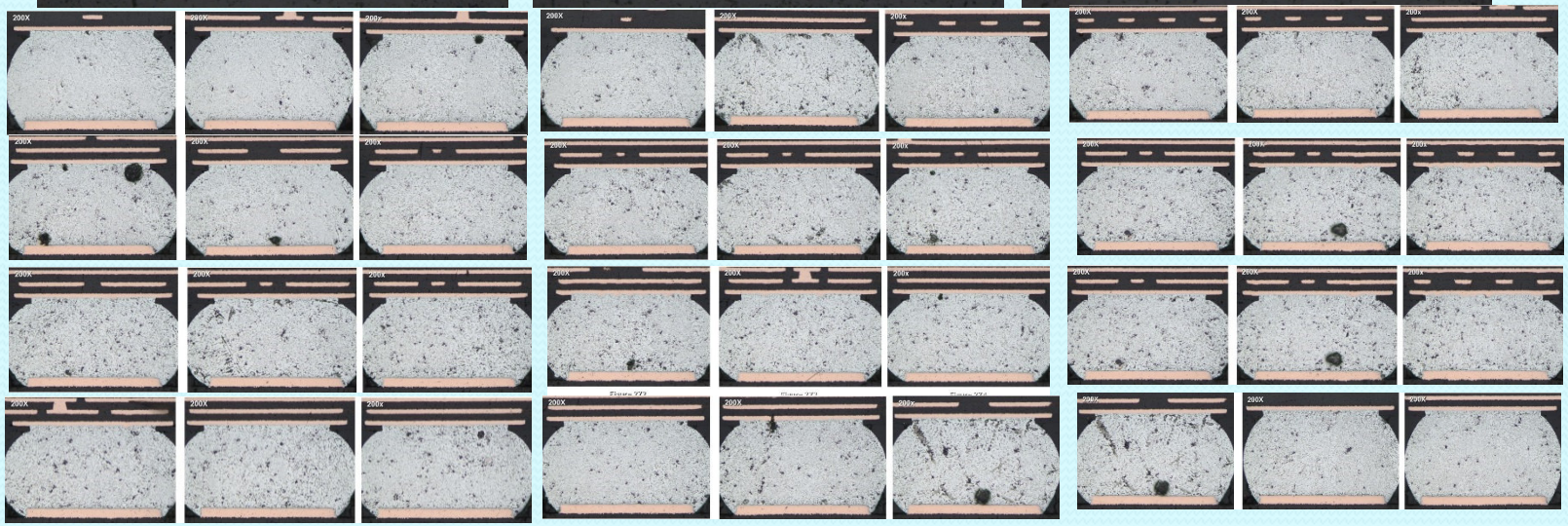
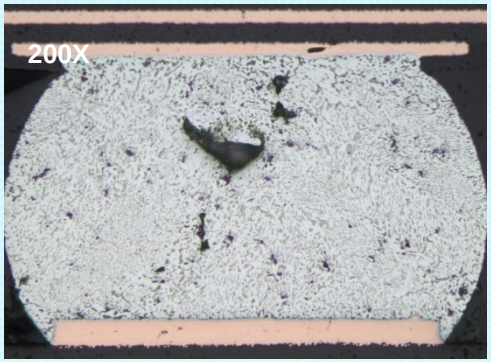
FCBGA 1924 on HASL

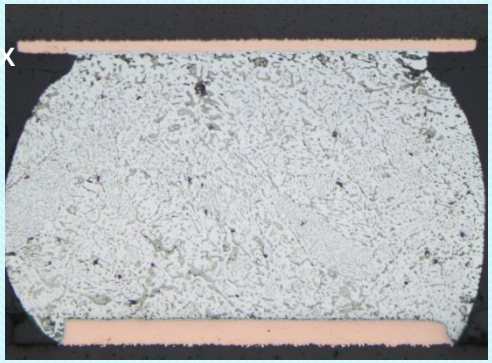












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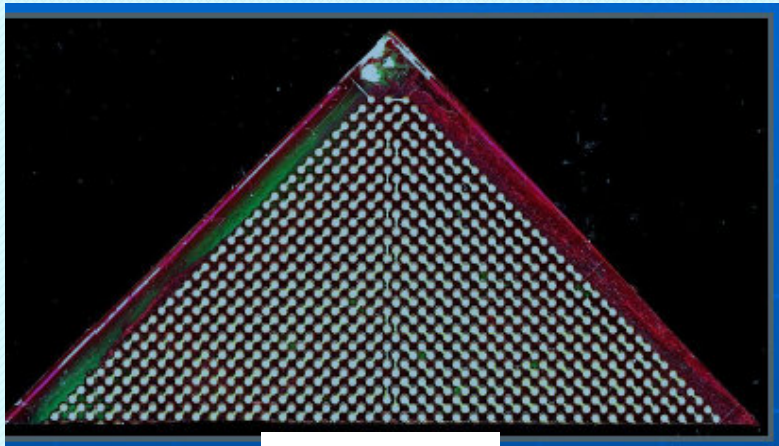
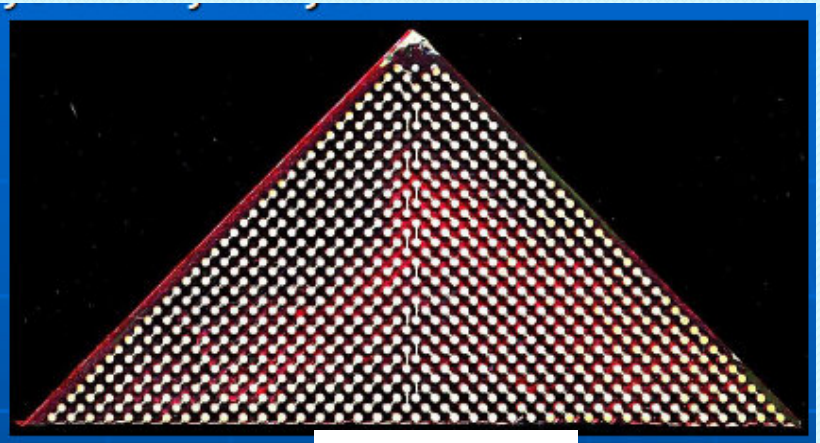
FCBGA 1924 on HASL

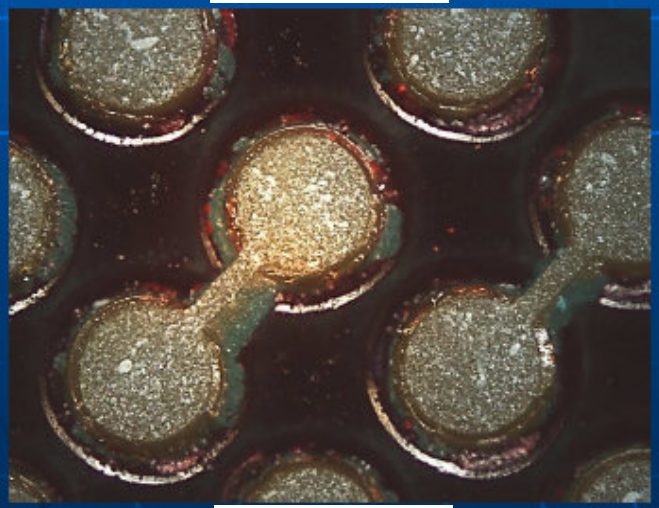
200 TSC (-65°C/150°C)



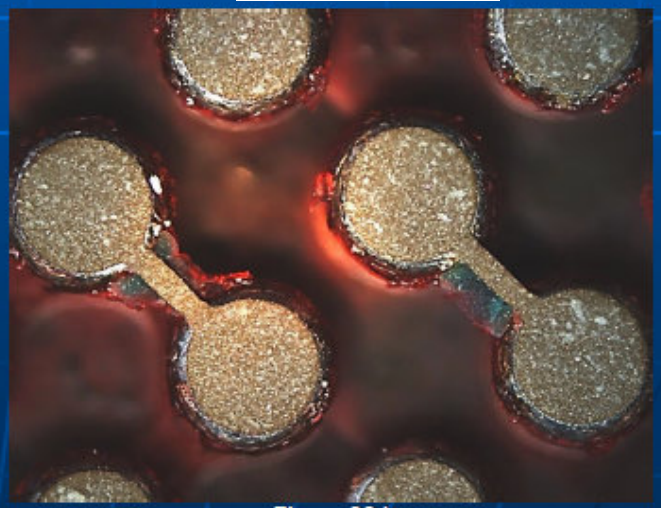
PCB Pads



BGA Pads



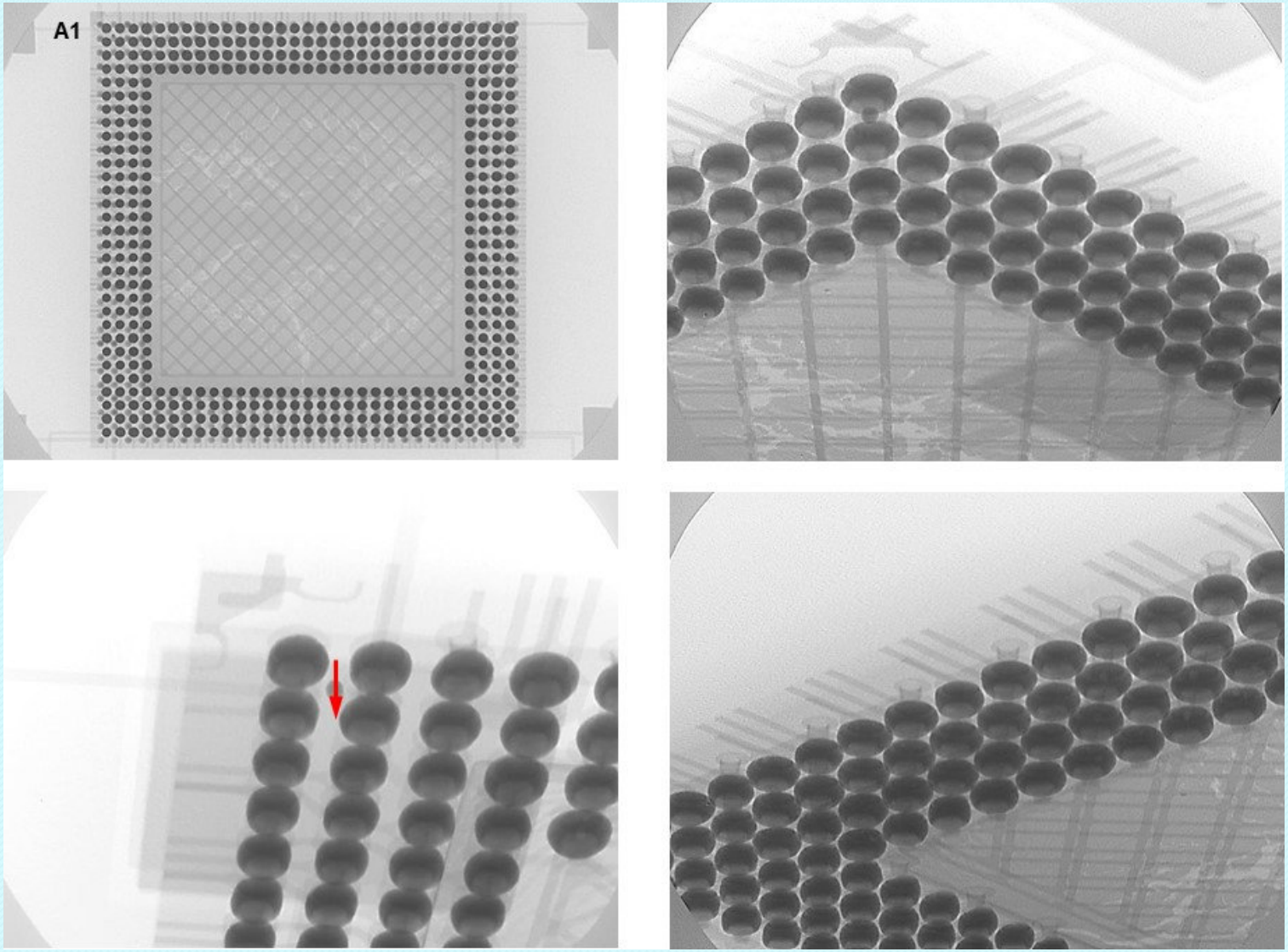
PCB Pads



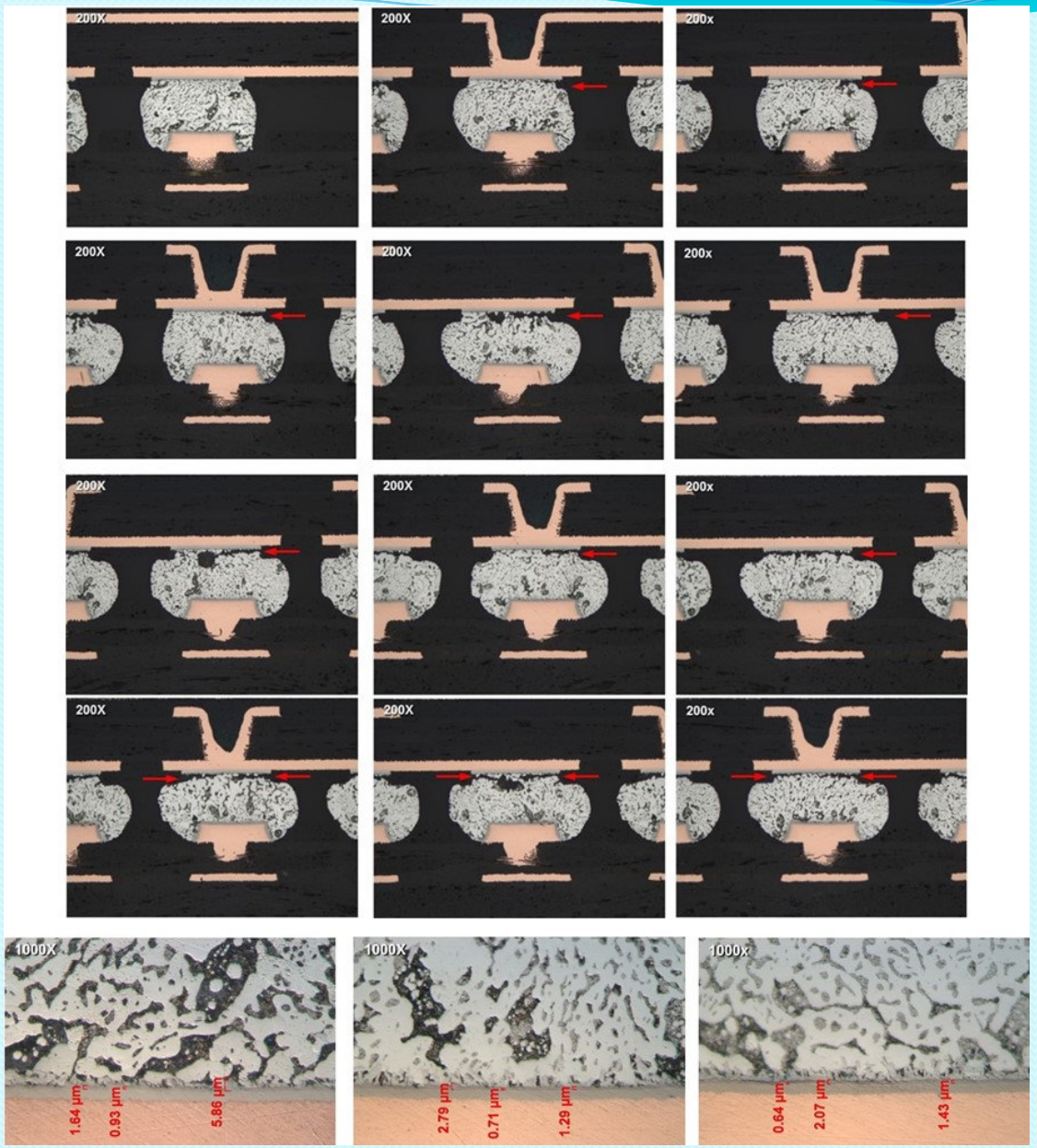
BGA Pads

No defective solder connections were found.

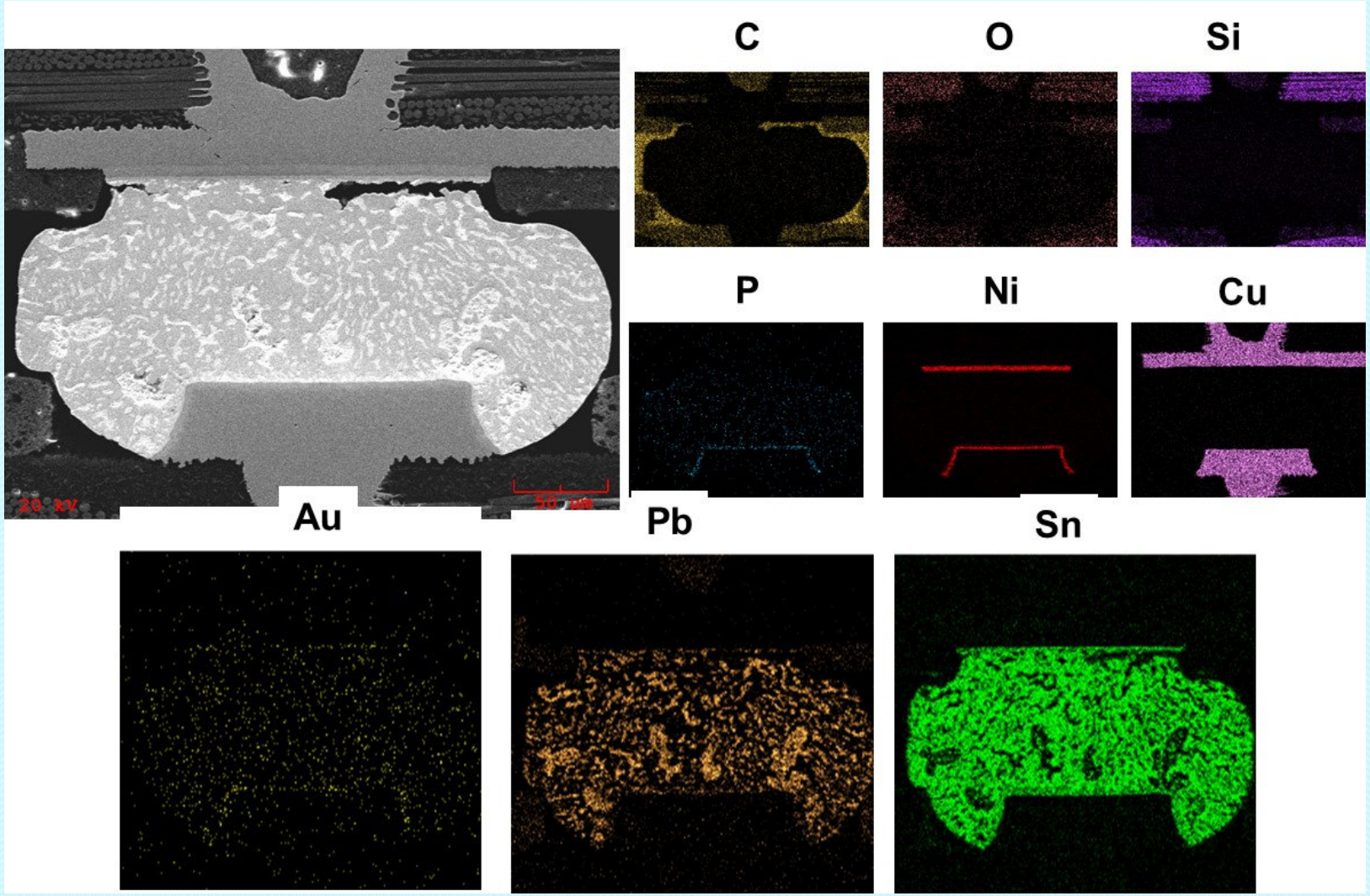
X-ray FPBGA432/ENEPIG



FPBGA432 on ENEPIG



SEM/EDS of FPBGA432 on ENEPIG PbSn Balls



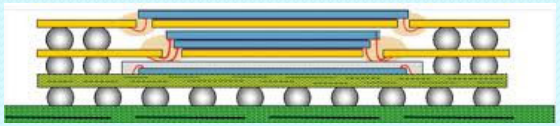
2.5D/3D
Packaging Technologies

Stack Die
PoP

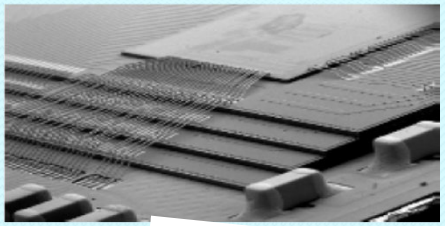
*2D to 2.5 D**
Single Chip to Multi-chip
TSV for Interposer

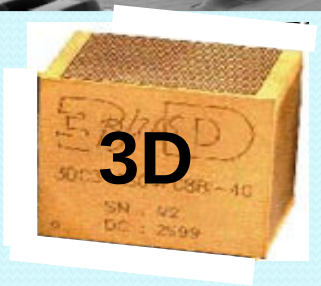
2.5D to 3DTSV
3D SIP

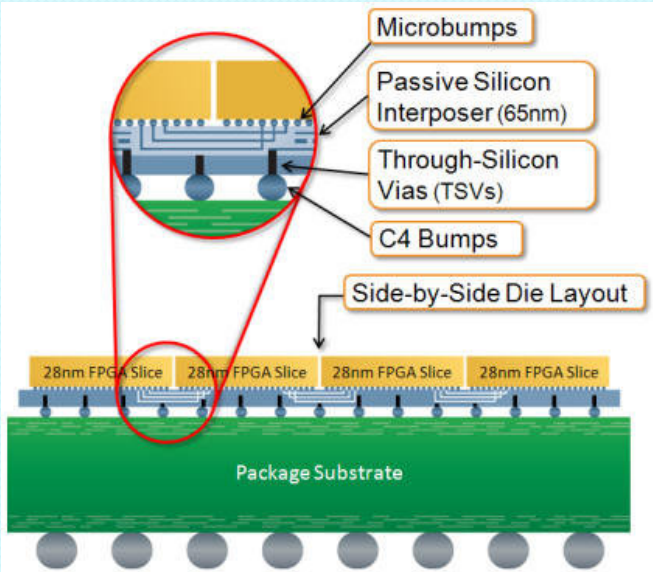
Package on Package (PoP)

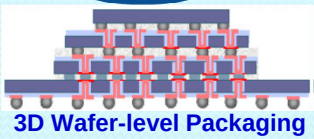


3D Wire Bond

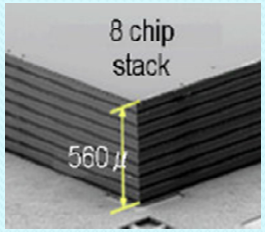






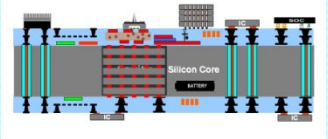


3D Wafer-level Packaging



Through-silicon Via

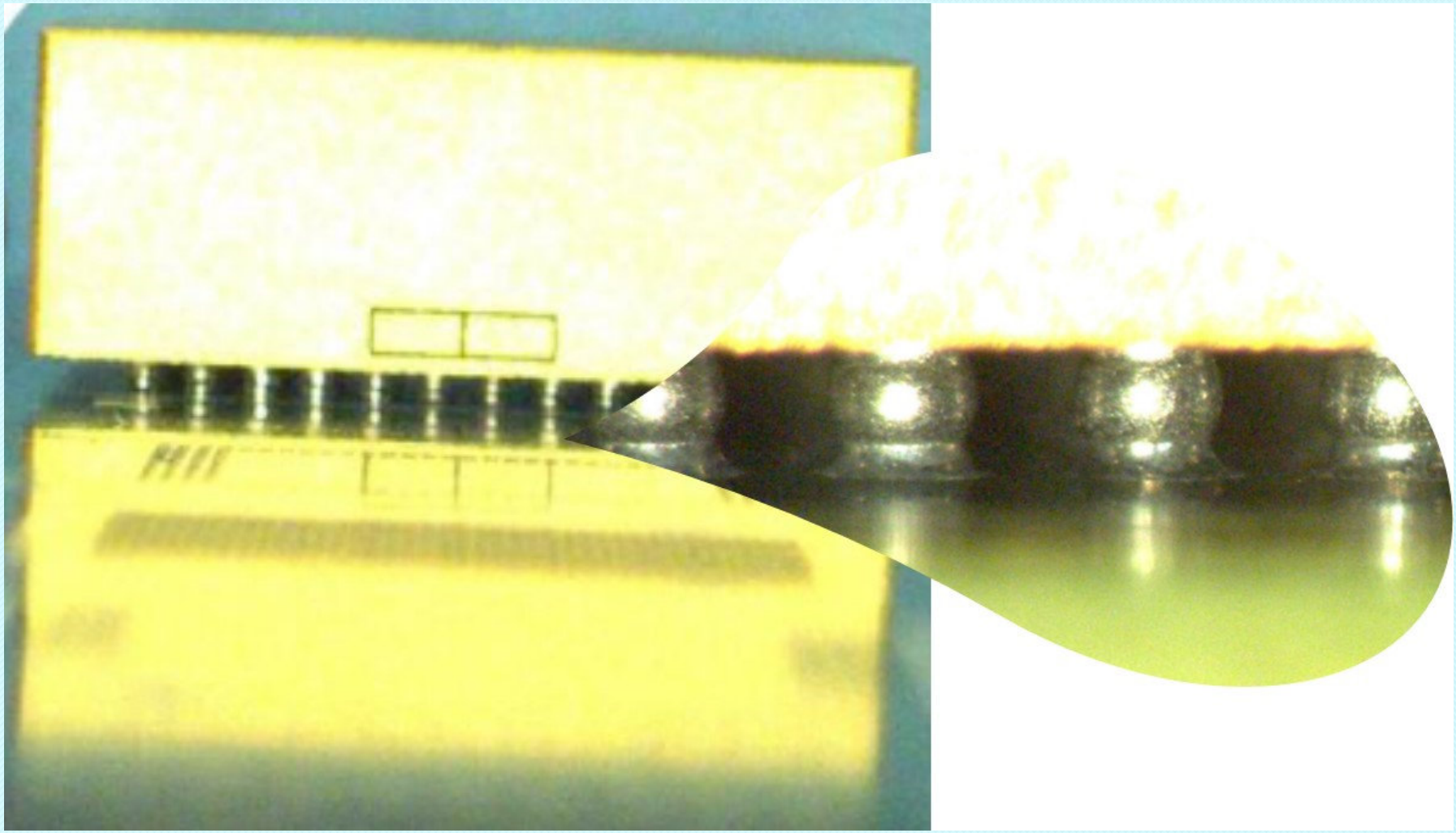
3D SiP



*** 2.5D now 2DS (on silicon substrates) and 2DO (on organic substrates)**

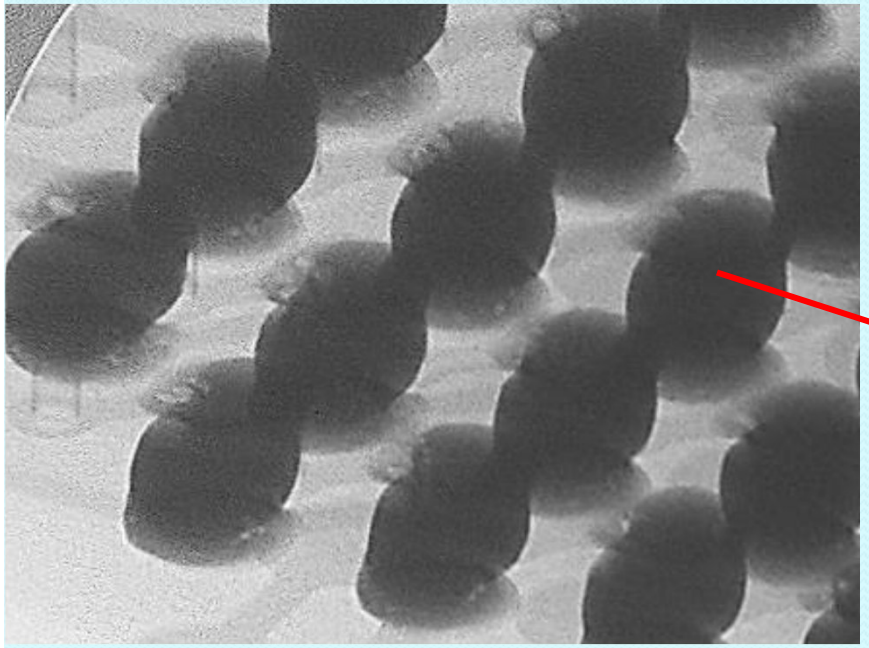
3D Stack

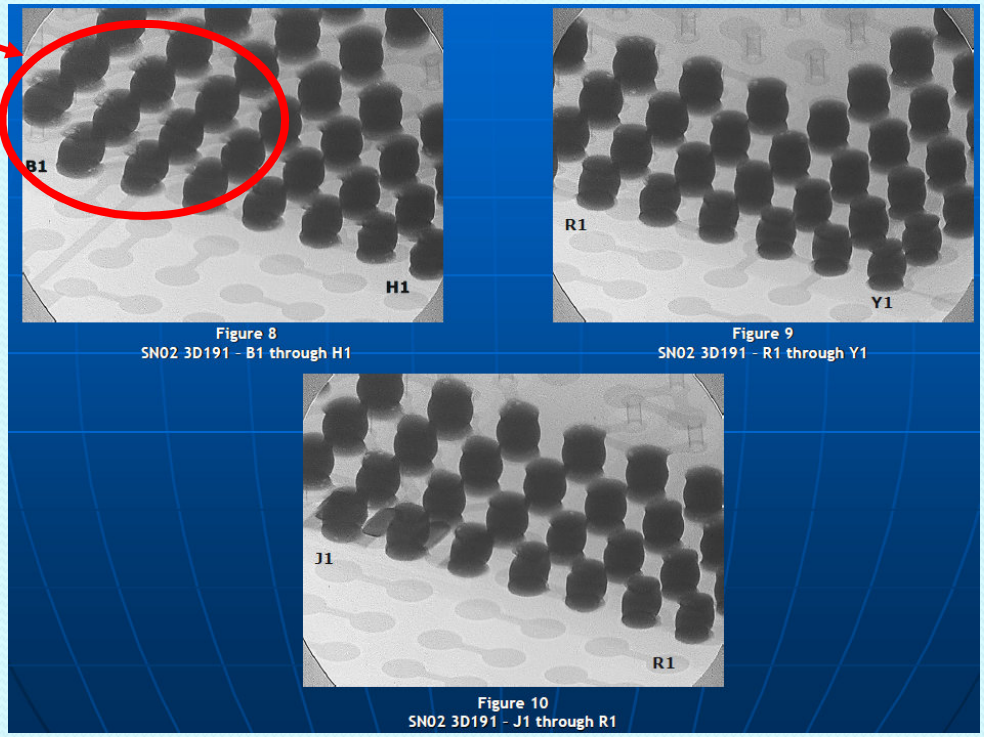
Single-sided



3D Stack

X-ray after TC





3D Stack

X-section after TC

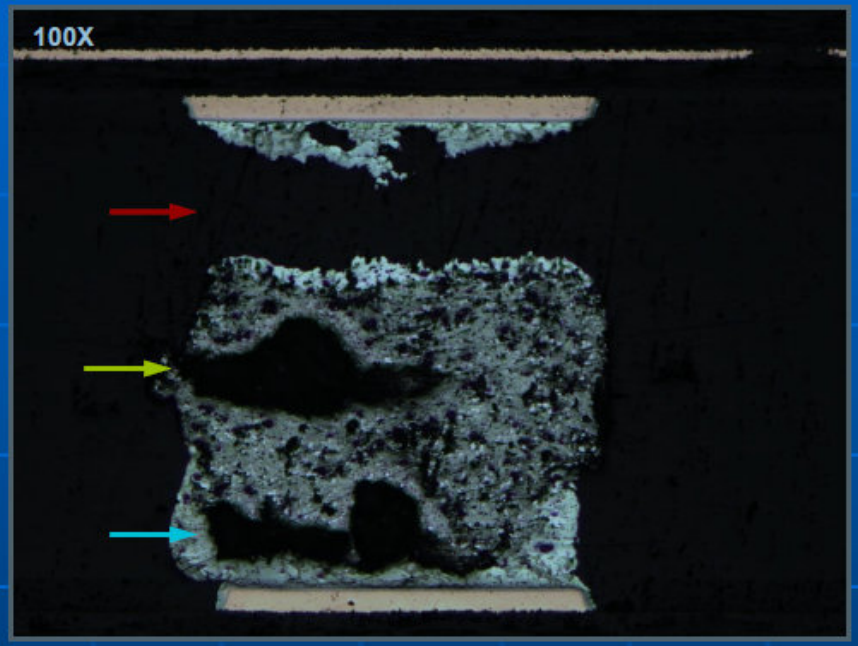


Figure 120
SN02 3D191 B1 - Bright Field Light

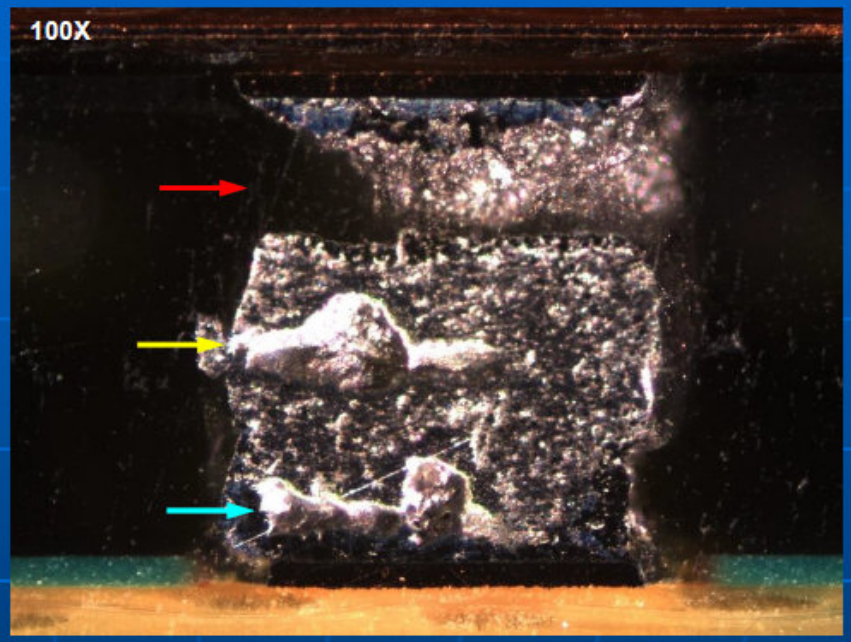
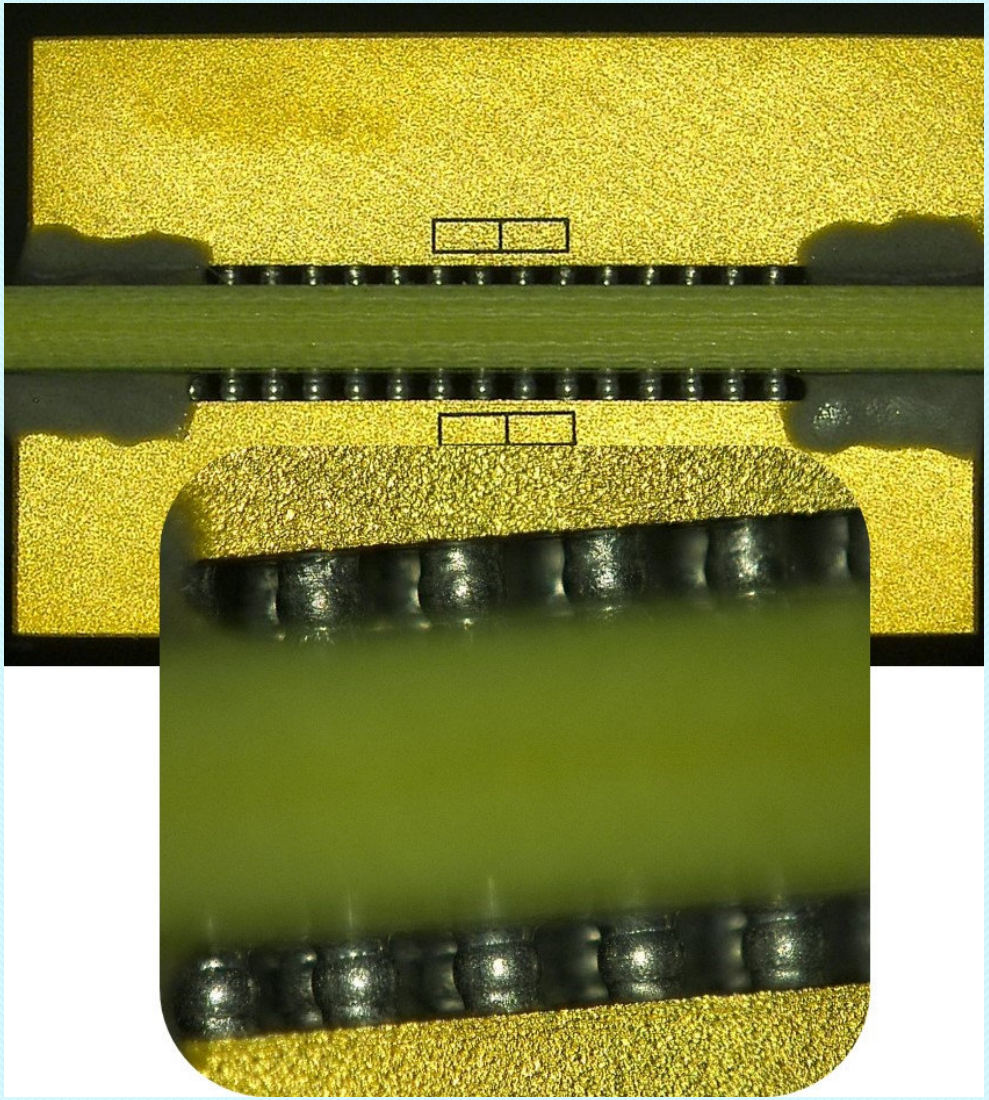


Figure 121
SN02 3D191 B1 - Dark Field Light

3D Stack

Double-sided



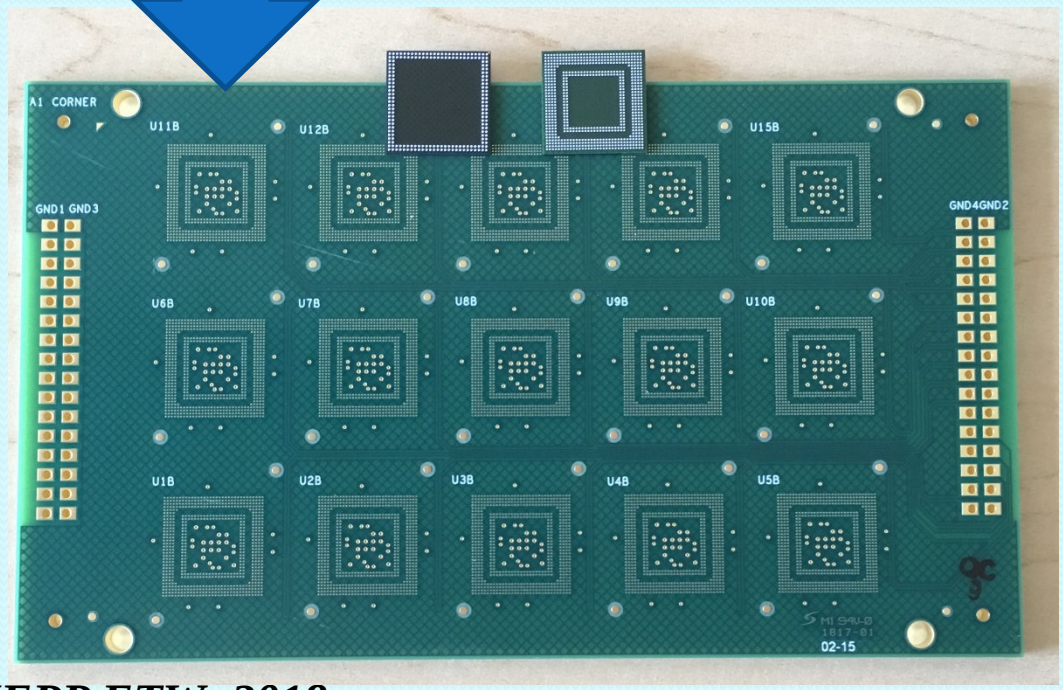
TMV/TSV Packaging Status

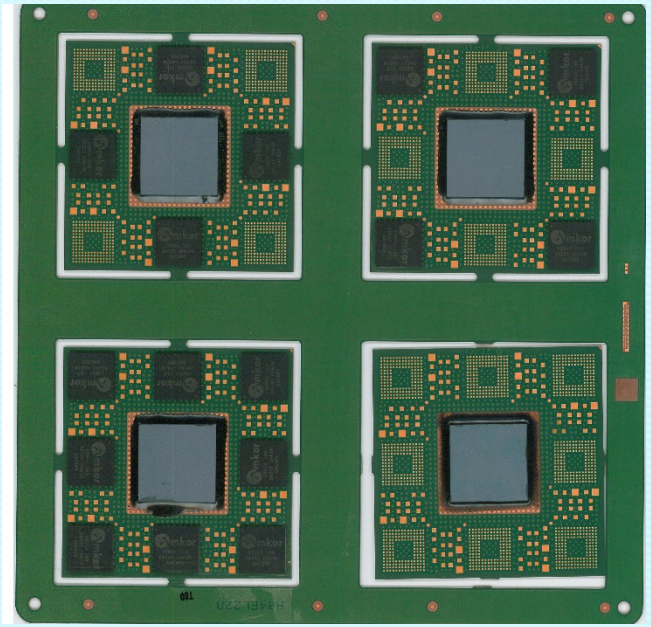
TMV

Through Mold Via (TMV)

2.5 D SIP

3D TSV





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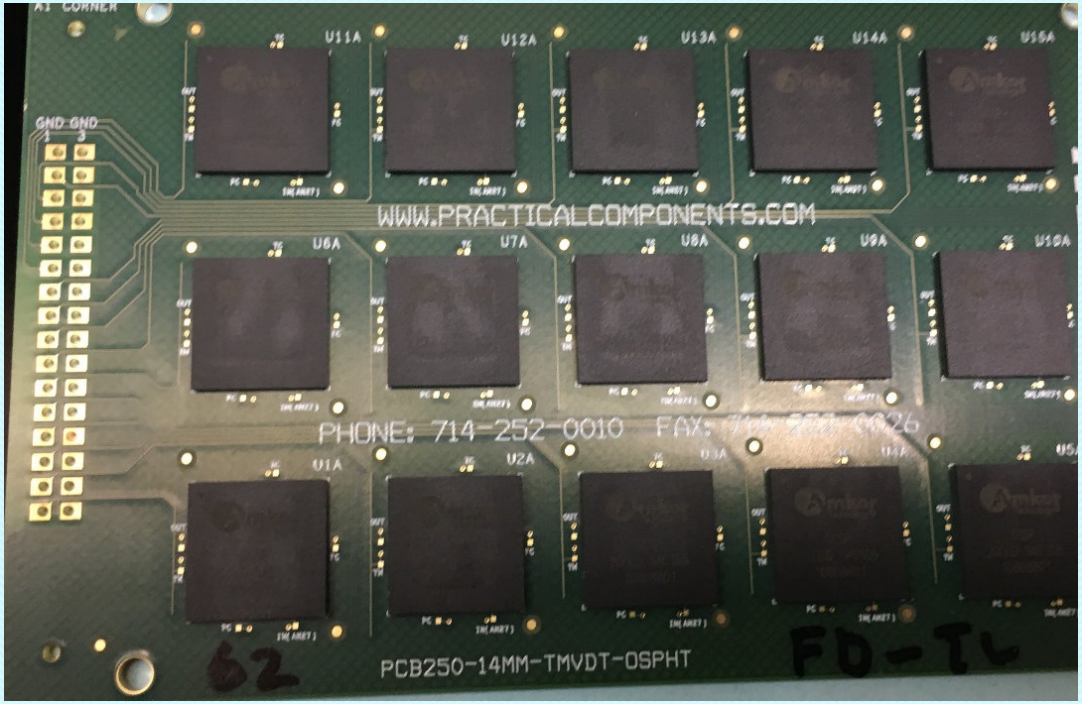
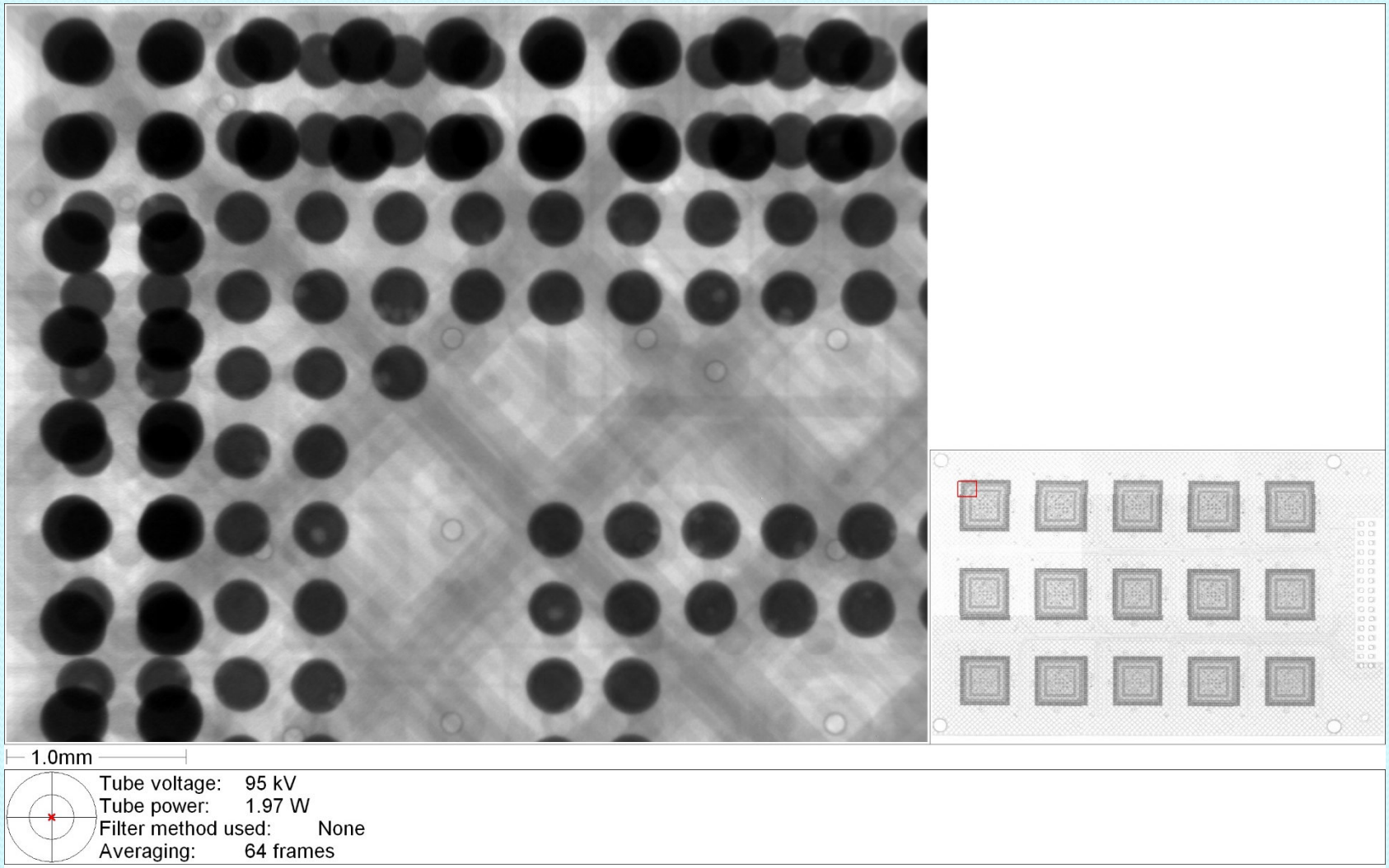
3D TMV

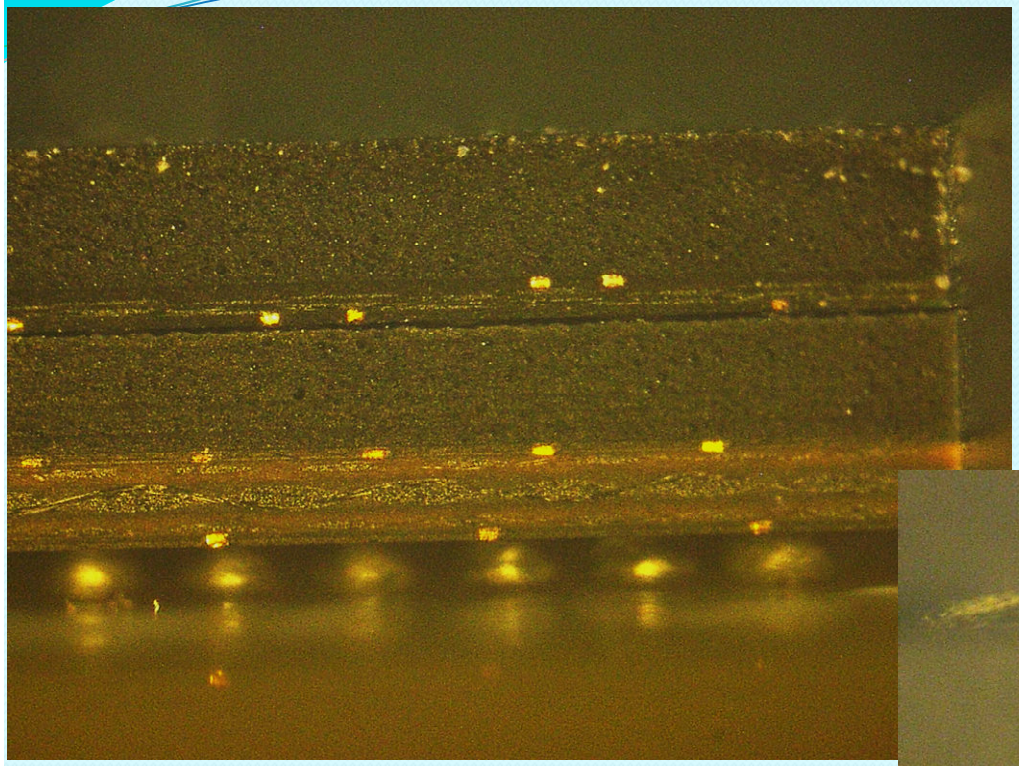
- Assembled ten (10) 3DTMV, 9-15 bottom/top parts
- Three assembly styles: Pre-stack, use solder paste for both bottom/top, use solder paste for bottom, flux for top
- No failures to 200 thermal cycles (-55/125C)
- NASA NEPP Report submitted



3D TMV

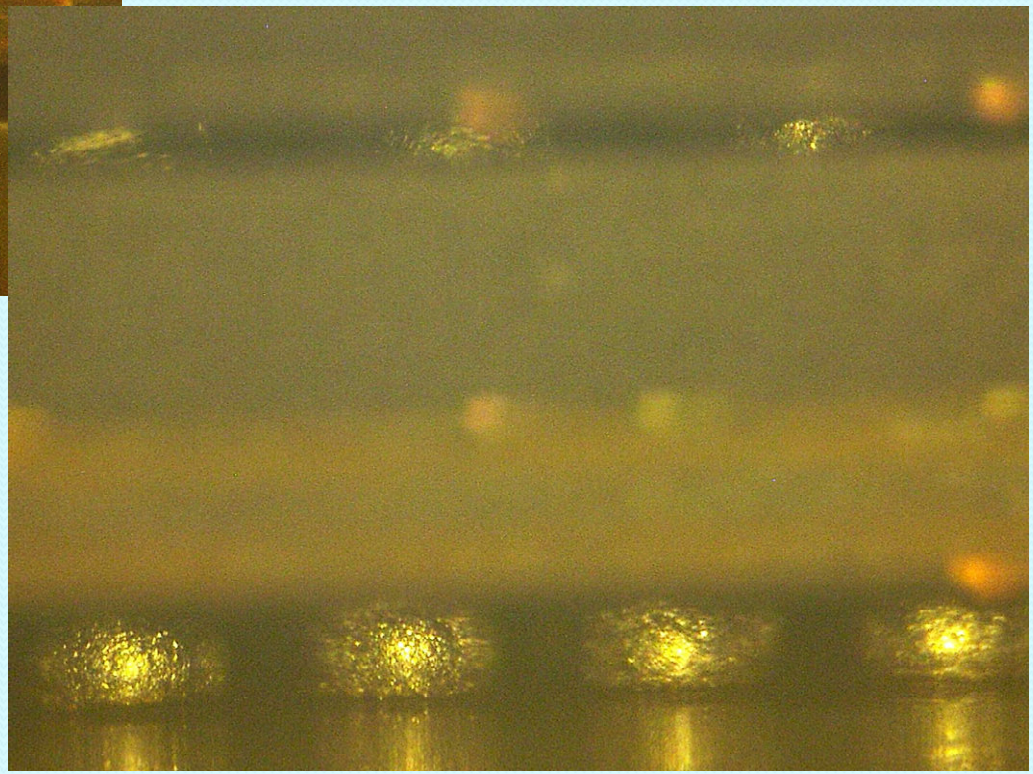

1.0mm
Tube voltage: 95 kV
Tube power: 1.97 W
Filter method used: None
Averaging: 64 frames

3D TMV after TC



Bottom: Solder Paste
Top: Solder Paste

Bottom: Solder Paste
Top: Flux Only



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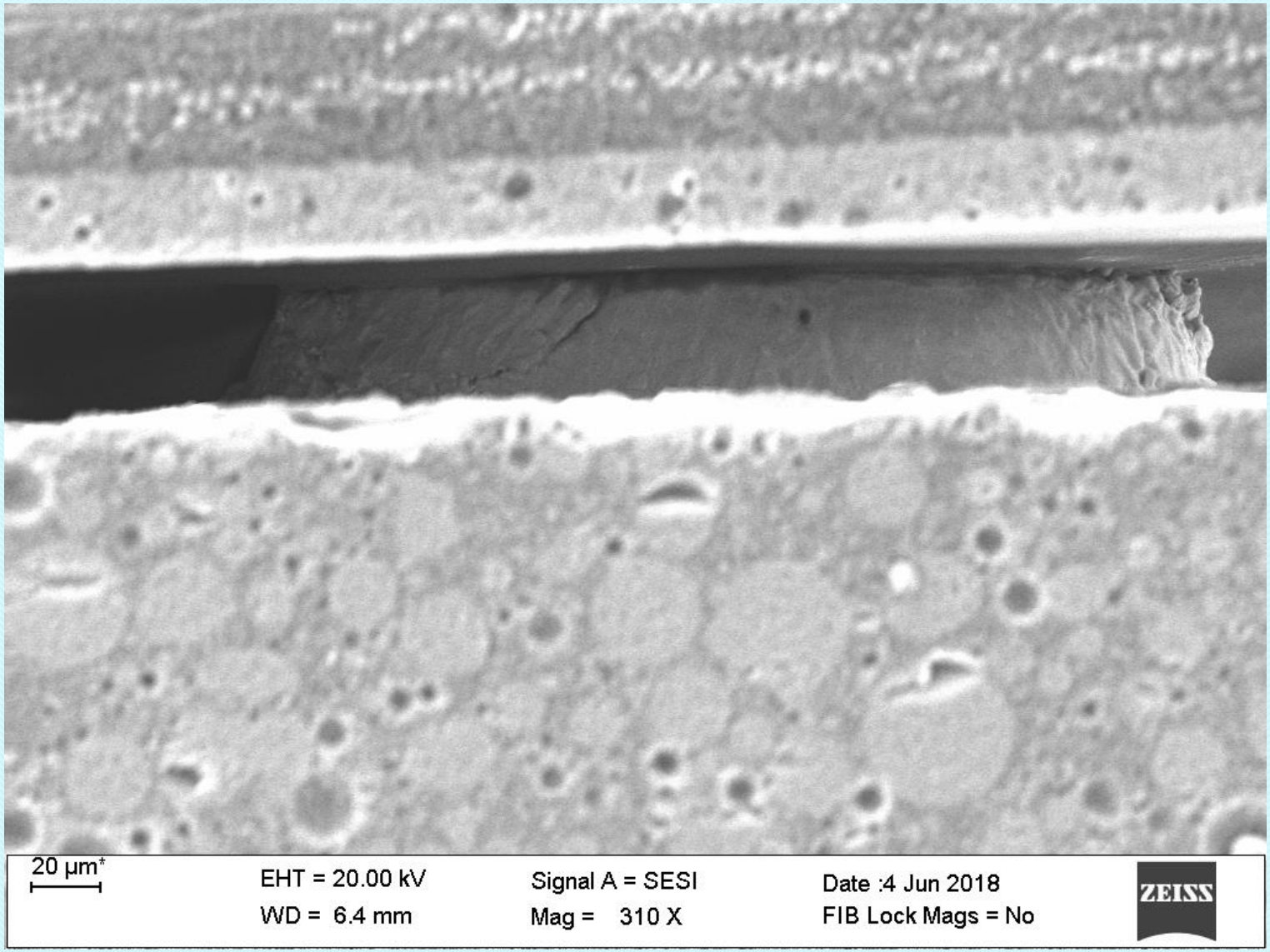
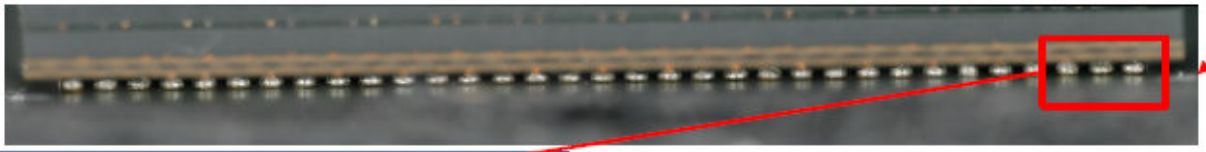
3D TMV
SEM after TC/Cut



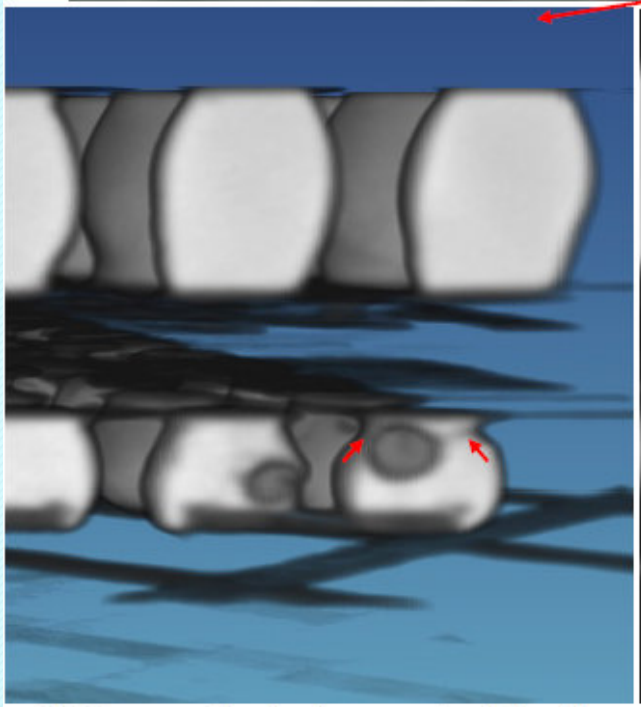
3D TMV

3D CT Scan after TC/Cut

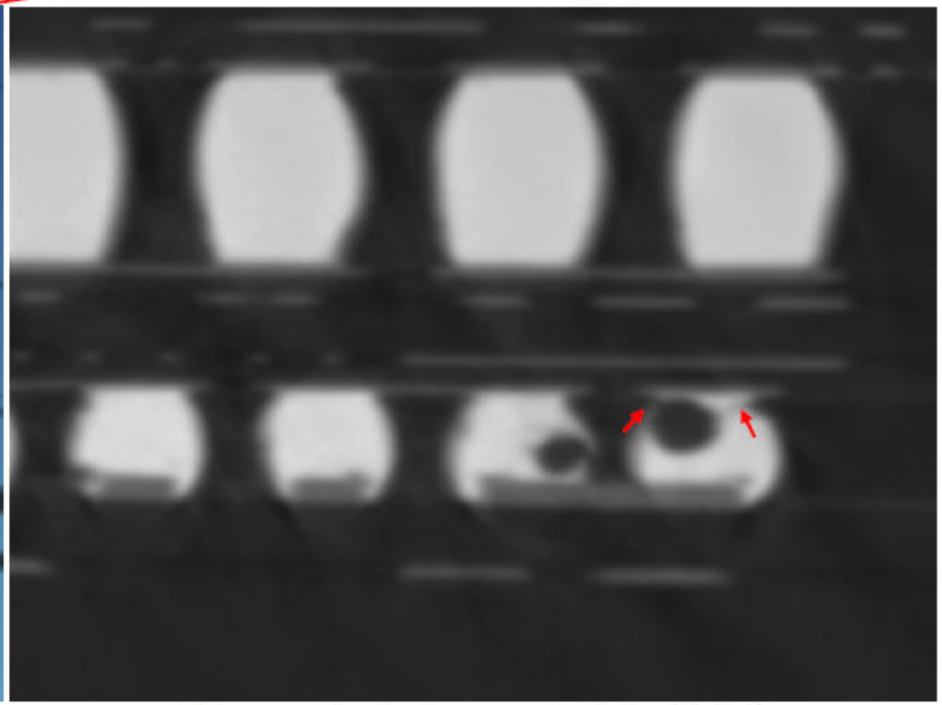
Optical Photos Board SN50



Overall photo

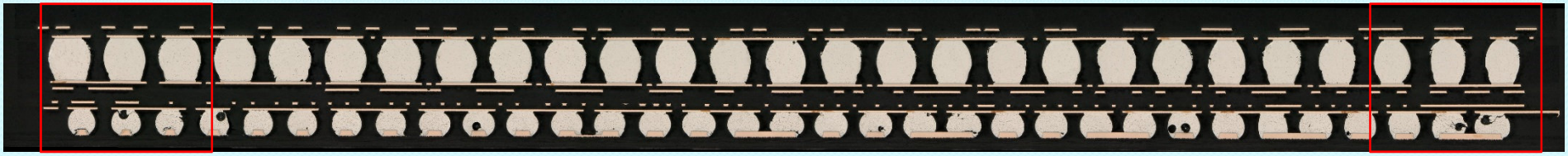


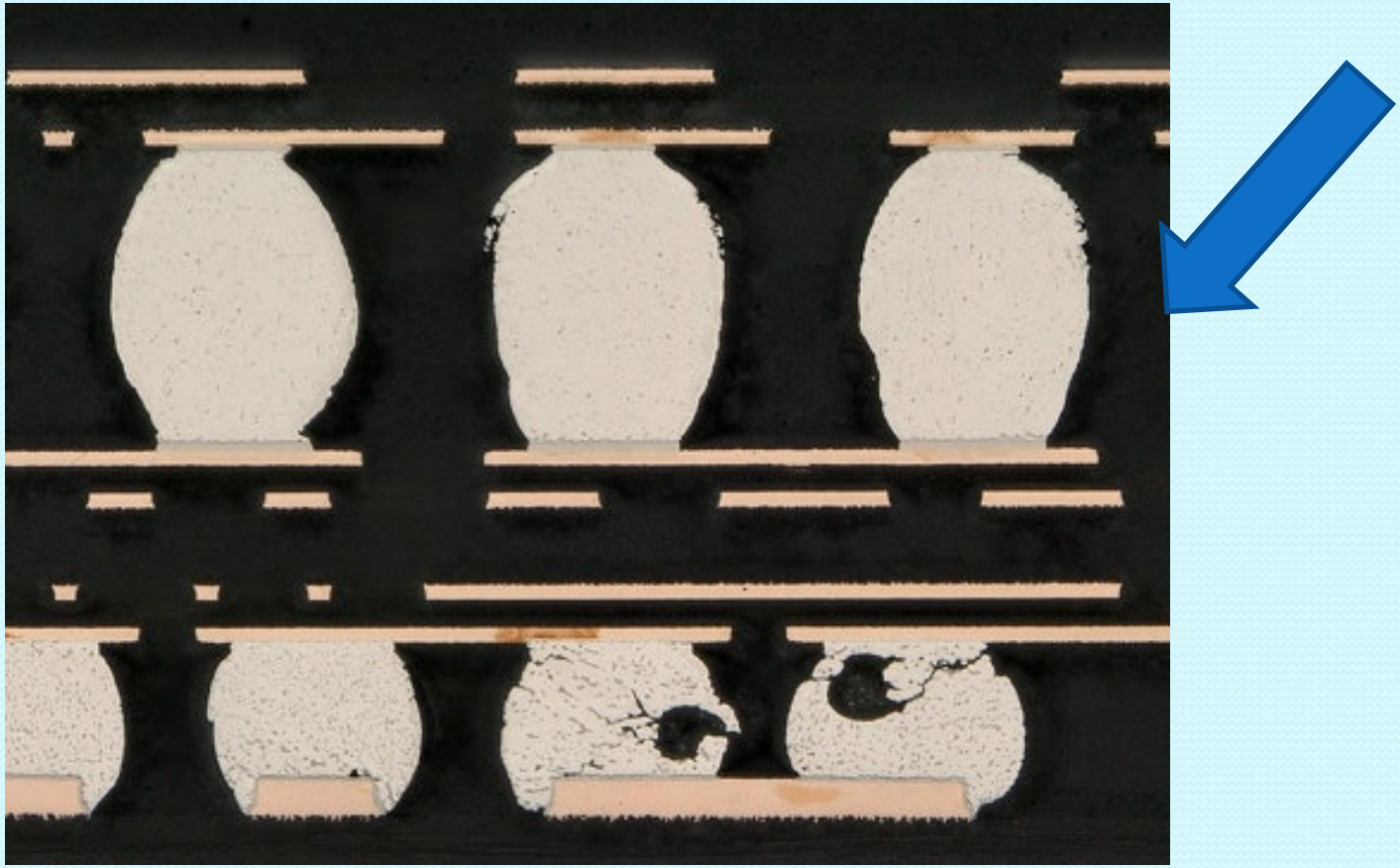
CT 3D cross section showing suspect crack in solder ball.



CT cross section showing suspect crack in solder ball.

3D TMV
X-section at 3D Scan





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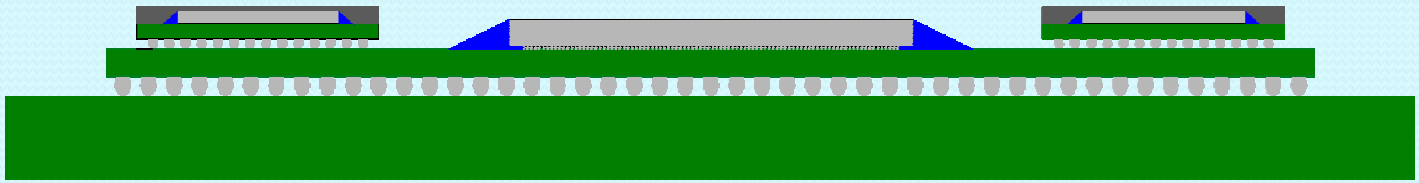
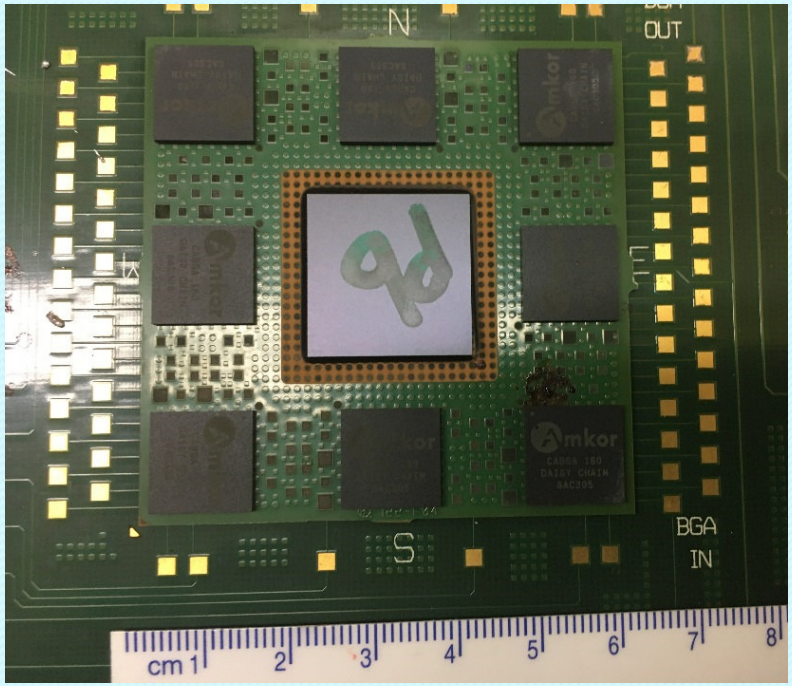
SiP TC Evaluation*

- Assembled 12 SIP includes CSP/FC
- Tin-lead and lead-free balls
- No failures to 200 thermal cycles (-40°C/125°C)



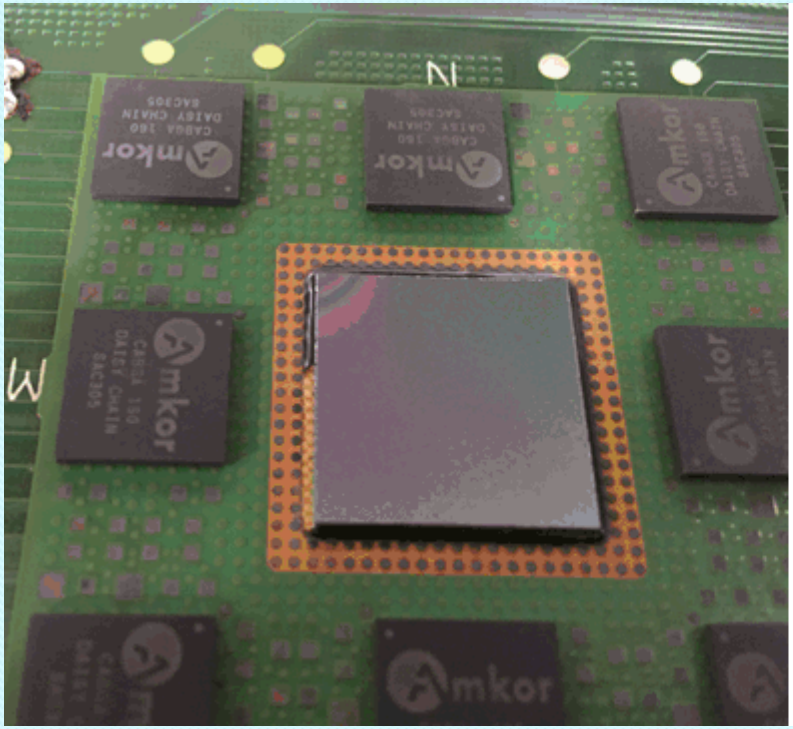


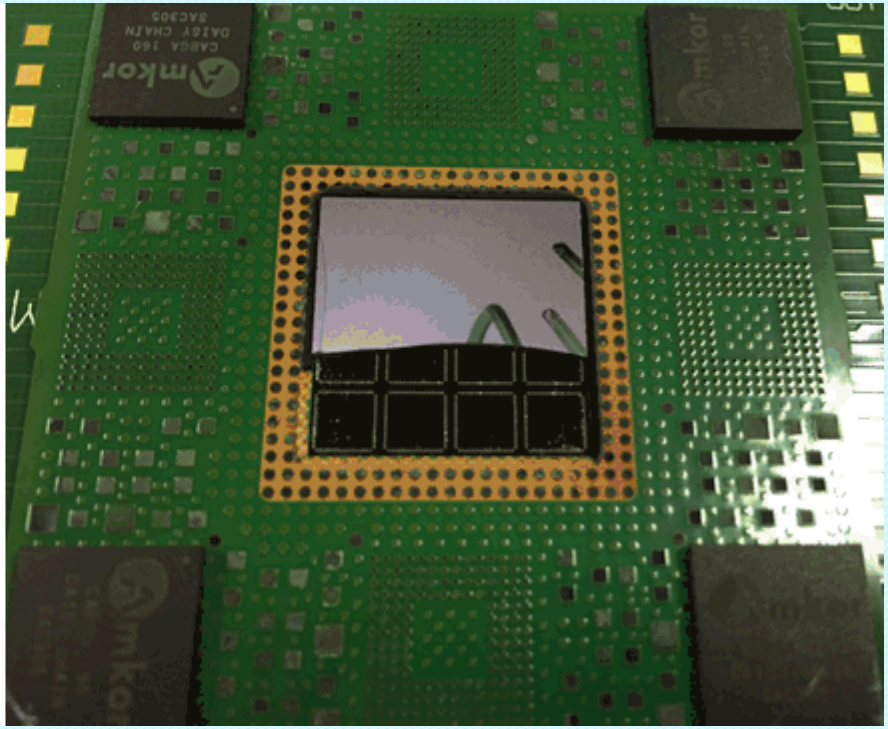
* Collaboration with AREA Consortium

Reza Ghaffarian/JPL/Caltech

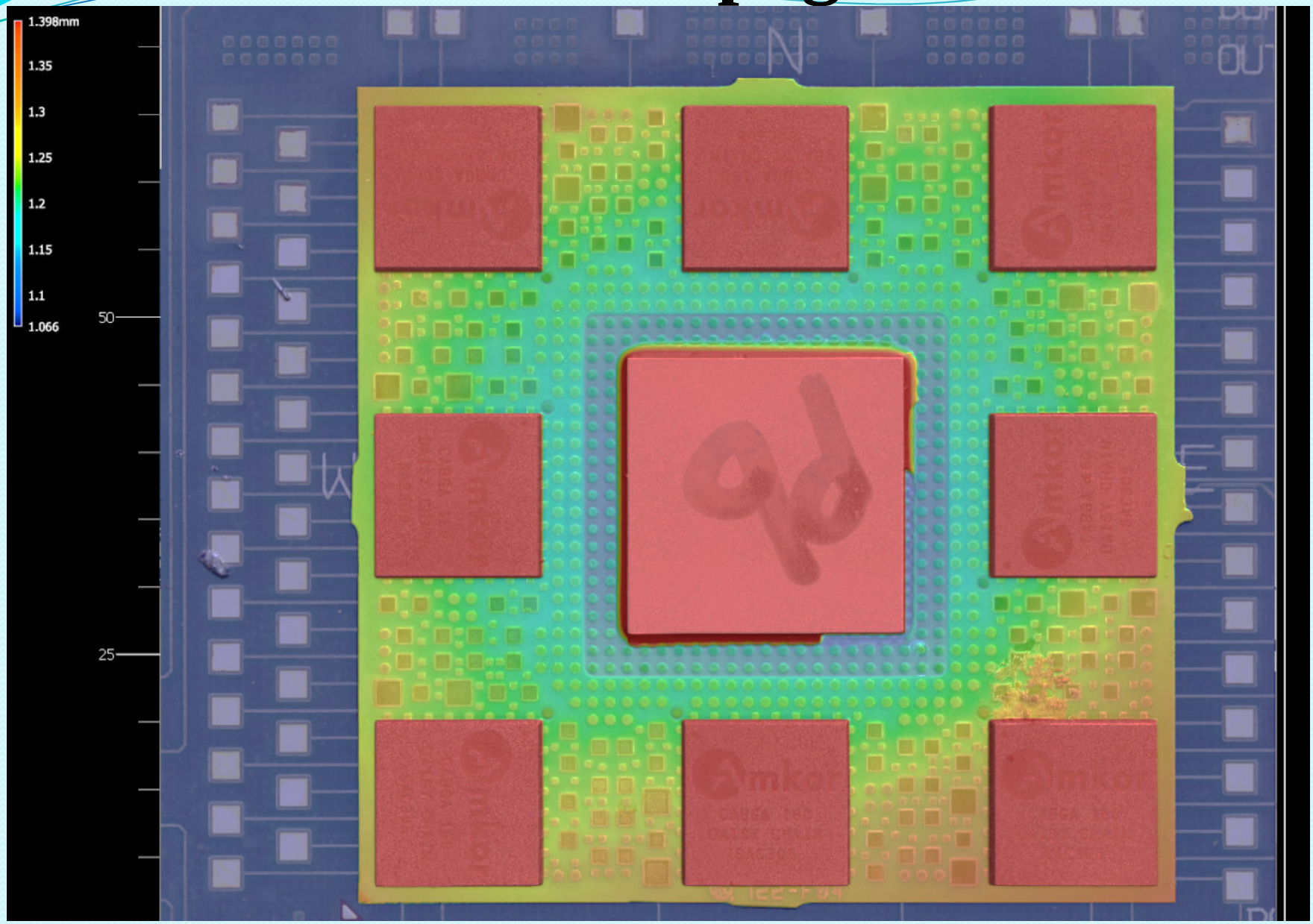
SiP TC Evaluation

- Failures at higher cycles
- Early failures and standard failures for CSPs
- Failure due to warpage for FC

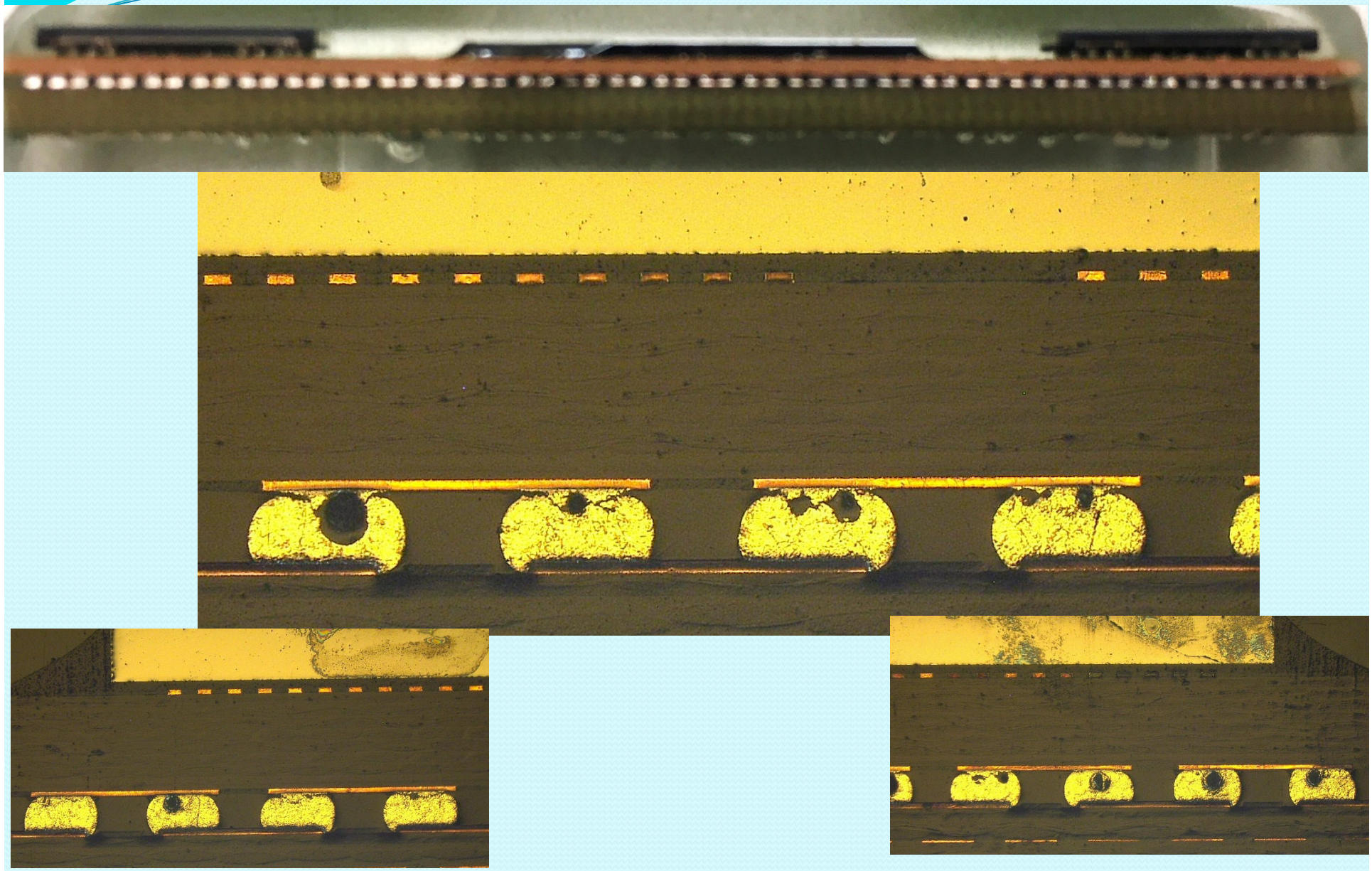




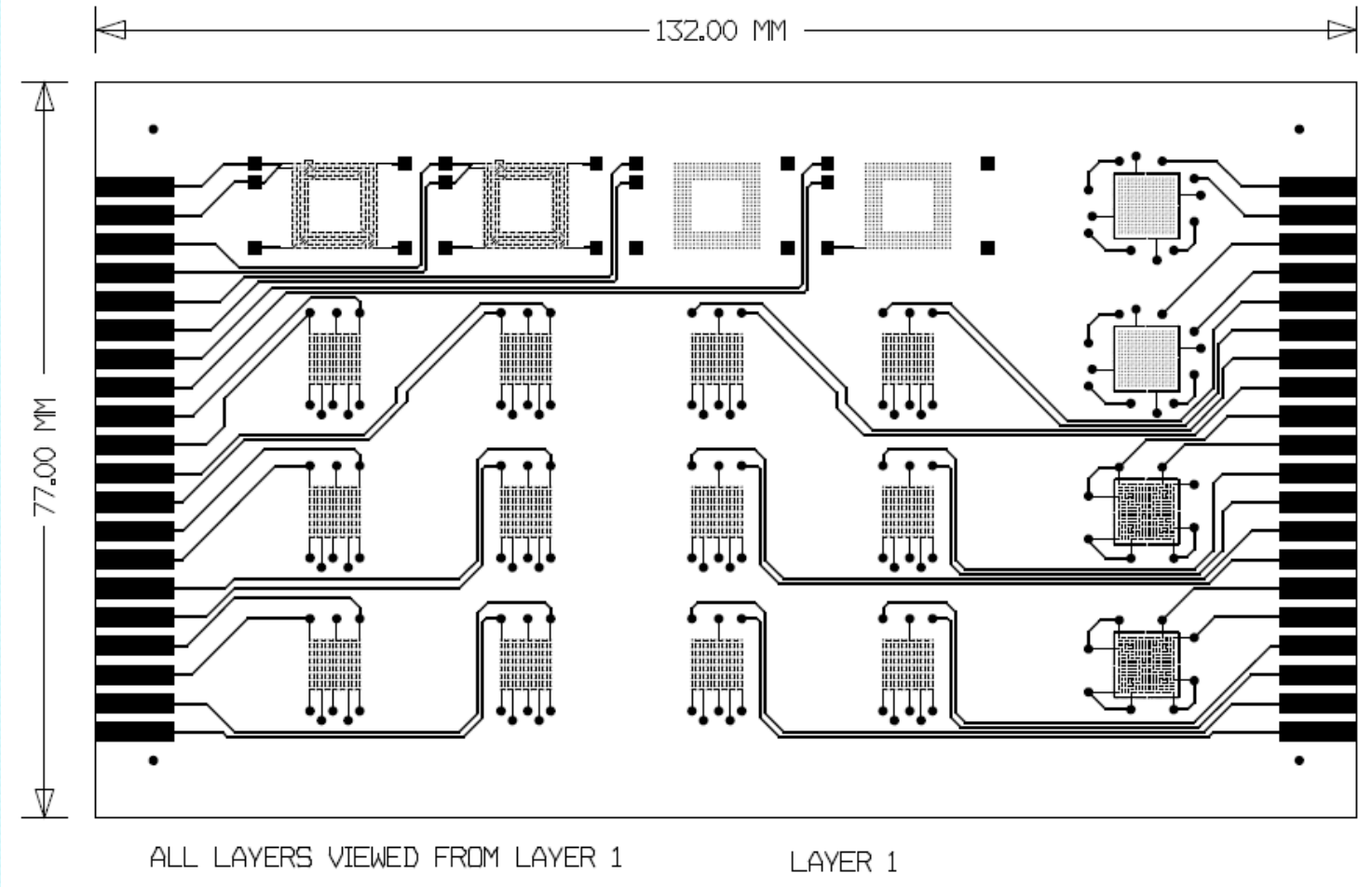
Warpage for SiP



BGA Failure in SiP



WLP & 3D TSV TC Evaluation



Option 1: Modified WLP TSV to enable PCB manufacturing

Option 2: Use interposer for TC

Summary

- Packaging technologies
  - Standard to WLP and 3DTSV
- NEPP evaluated reliability of numerous packages
  - FCBGA. FPBGA, 3D stack, WLP, SiP, and 3D TSV
  - Presented results of numerous TC evaluation
- No failure to 200 TC cycles (–55°/100°C)
  - FCBGA1924, PBGA896, FPGA, 3D stack
  - No failure condition verified by daisy-chain or X-section
- Failure to 200 TSC cycles (–65°/150°C)
  - FPBGA 432 I/O, 0.4 mm pitch failed near 100 cycles
- No failure of TMV assemblies (–55°/125°C)
  - All paste at board, but solder paste or flux on the top
  - Pre-stack with paste and then solder onto board
- No failure of SiPs (–40°/125°C)
  - Effect of top stack on lower failure initiation observed at higher cycle
  - Various failures including flip-chip at higher cycles
- Design/Assembly of WLP/FOWLP on standard PCB is challenging. Interposer needed
- NEPP Test Report on FCBGA/3D stack is on NEPP Website
- NEPP Report for TMV/SiP is being released

Jet Propulsion Laboratory
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http://nepp.nasa.gov

Thank You!