NEPP Processor Efforts 2018

Steven M. Guertin

steven.m.guertin@jpl.nasa.gov

818-321-5337

Jet Propulsion Laboratory / California Institute of Technology

Acknowledgment:

This work was sponsored by:

The NASA Electronic Parts and Packaging Program (NEPP)

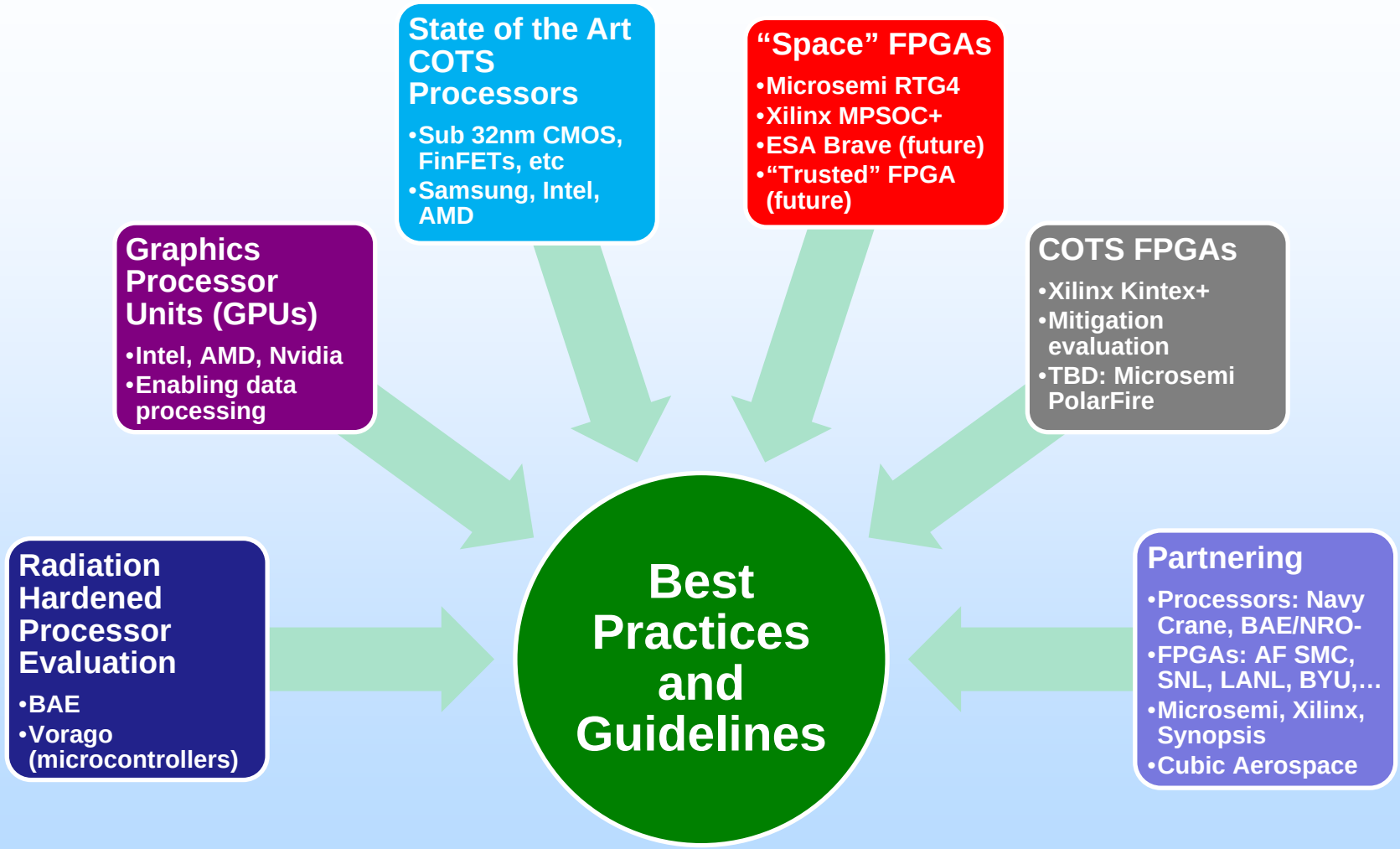
Acronyms

AFRL	Air Force Research Laboratory
AMD	Advanced Micro Devices
ASU	Arizona State University
CMOS	Complimentary Metal Oxide Semiconductor
CPU	Central Processing Unit
DDR	Dual Data Rate
DIP	Dual Inline Package
DUT	Device Under Test
FET	Field Effect Transistor
FPGA	Field Programmable Gate Array
HPSC	High Performance Space Computer
GPU	Graphics Processing Unit
GSFC	Goddard Space Flight Center
ILP	Instruction-Level Parallelism
JPL	Jet Propulsion Laboratory
LANL	Los Alamos National Laboratory
LPP	Low Power Plus
MPSOC	Multiprocessor System on Chip
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts and Packaging Program
NSWC	Naval Surface Warfare Center
OS	Operating System
POP	Package on Package
SBU	Single Bit Upset
SEE	Single Event Effects
SEL	Single Event Latchup
SOC	System on a Chip
SW	Software
TBD	To Be Determined
TID	Total Ionizing Dose

Outline

- Intro/Processor Overview
- Processor & Microcontroller Tasks Review
- Partnering & Opportunities
- Trends and Test Methods
- Test Efforts – Snapdragon
- RHBD Processors
- Test Efforts – RAD5545
- Future Directions…

NEPP – Processors, Systems on a Chip (SOC), and Field Programmable Gate Arrays (FPGAs)



Potential future task areas:

artificial intelligence (AI) hardware, Intel Stratix 10

Task Partnering

- **Engaging in collaborative efforts:**
  - **Adam Duncan & NSWC Crane folks**
  - **Carl Szabo, Ed Wyrwas, Ted Wilcox, and Ken LaBel, GSFC**
  - **Jeff George, Aerospace Corporation**
  - **Larry Clark, ASU**
  - **Heather Quinn, LANL, and other members of the Microprocessor and FPGA Mitigation Working Group**
  - **Sergeh Vartanian, Andrew Daniel, and Greg Allen, JPL**
  - **Vorago Technologies – collaborating on hardware/plans**
  - **Paolo Rech – GPU/Applications, UFRGS**
  - **Intel – informally**
  - **BAE Systems – team forming**
  - **Qualcomm Cybersecurity Solutions – team forming**

- **Looking for additional collaborators**
  - **Tester side – are you testing processors?**
  - **Manufacturer side – knowledge or hardware support**
  - **Application side – specific applications…**

What are we trying to do?

- **Primary Purpose**
  - **Utilize processors as “bleeding edge” CMOS evaluations with goals of determining failure sensitivities and modes as well as to provide guidance for future flight project testing**
  - **Evaluate emerging architectures for radiation tolerance such as multi-core, etc…**
  - **Partner with NASA/Mil-Aero developments of processors to enhance qualification processes and provide independent assessments**
  - **Provide selective radiation evaluation of small mission (aka CubeSat) electronics**

What are we trying to do?

- **Secondary Purposes**
  - **Cross section vs. linear energy transfer (LET) information on device structures & Architectures**
    - **Test and qualification methods for processors**
    - **Build knowledge base of processor architectures**
  - **Provide total ionizing dose (TID) test data and parts program information**
  - **Gather information on various fabrication facilities**
    - **CMOS Nodes**
    - **On-shore vs. off-shore fabrication**
  - **Resilience of commercial processors**
    - **Keep abreast of developing technology trends and how to perform appropriate radiation testing**
  - **Device structure sensitivity to global device sensitivity**

Focus Categories

- **Architecture** – to support evaluation and use of processor architectures throughout NASA, including processor types and FPGA/Soft processors
- Implementations – to support evaluation and use of primary form-factors
- **Fabrication Facilities/Technology** – to obtain information on fabrication facilities and related technology (e.g. Samsung 7nm, 3D, etc.)
- Application/Use Case – to support ways of using devices for different NASA needs
- Develop data on specific devices/Methods for evaluation – support actual flight use, and understand that in many cases the project will have to evaluate their own part (but we can provide guidance)
- **Manufacturers** – to have an up-to-date tool set for understanding devices from each manufacturer.
- **Collaborations** – to engage manufacturers when they are available or can work with us, we want to harness this
- **Test Method Development**
- **Guidelines and BOKs**
- **Recent work**

Advanced Processors - Commercial

- collaborative with NSWC Crane, others

14nm CMOS Processors (w/Navy Crane)

- Intel 14nm FinFET commercial
  - 5th and 6th generation
- Samsung 14nm LPP Snapdragon 820

Closing Out on processor side – see GPUs below.

- AMD Ryzen 14nm Global Foundries

Radiation Testing

10nm CMOS Processors

- Samsung 10nm Snapdragon 835

Radiation Testing

- Intel 10nm

Radiation Testing

7nm CMOS Processes

- Samsung 7nm (Qualcomm)

Radiation Testing

GPUs

- nVidia 1050 (14 nm)

Radiation Testing

- Tegra TX1/TX2 (14 nm)
- Snapdragon 820 (14 nm)

Radiation Testing

FY17 FY18 FY19 FY20

Advanced Processors – Flight/RHBD

- collaborative with BAE Systems, HSPC, others

High Performance Space Processor (HPSC)

- Joint NASA-AFRL Program for RH multi-core processor

TBD – (track status)

RH Processor

- BAE Systems RAD5510/5545
  - Leverages P5040 architecture

Radiation Testing (Collaborative with BAE Systems)

General *NASA-Specific*

Radiation Testing

Radiation Testing

Freescale Processors

- P2020 Communication Processor (w/Air Force)
- P5040 Network Processor

Closeout

FY17 **FY18** **FY19** **FY20**

Microcontrollers & Soft Processors

- collaborative with Vorago, others

CubeSat/SmallSat Microcontrollers

- No current plans

Automotive-Grade Microcontrollers

- No current plans

Radiation-Hardened Microcontrollers

- Vorago VA10820 ARM Cortex-M0 MCU
- Vorago M4

Test Review/Collaboration

- Cobham UT32M0R500

Establishing Approach

Hard vs. Soft Core Processors

- Soft/Hard ARM in Xilinx FPGA

Establishing Approach & Collaboration

FY17 **FY18** **FY19** **FY20**

Target Devices

- GPUs – nVidia 1050
  - 12 nm TSMC, stacked die, 3D
  - “Standard test for proton facilities”
- Cell-phone/mobile SOCs
  - Qualcomm Snapdragon 835 10 nm Samsung
  - nVidia Tegra X1/X2 16 nm TSMC
- High Performance Processors – Intel & AMD Ryzen 7
  - Intel 14 nm, AMD Global Foundaries 14 nm
  - Future: Intel 10 nm late in 2018
  - “Standard test for proton facilities”
- Microcontrollers – Cobham UT32M0R500, Vorago VA10820, M4
  - ARM, current-generation devices
- RHBD Devices
  - RAD5545 - ~10 GOPs, PowerPC – participating in testing
  - HPSC - ~100 GOPs, significant power scaling, ARM – monitoring development

Developed Test Architectures

- For potential users – we have developed and are supporting knowledge base on the following devices and architectures
  - PIC family (simple Harvard architecture)
  - MSP family (Custom von-Neumann)
  - Atmel AT91 family (ARM)
  - PowerPC e500, e5500, etc. (P2020, MPC56xx, P5020)
  - Sparc (Cobham UT699)
  - Intel x64/x86 (tests of various devices AMD and Intel similar)
  - Maestro (RAW architecture, no active efforts)
- Potential future architectures
  - MIPS
  - RISC-V
  - FPGA Soft/Hard Core Evaluations Approaches

Deliverables

- **SOC Test Guideline – fully released 3/2018**
- **Radiation test data/reports on:**
  - **P2020 – SEE (single event effects) – Heavy Ion & Proton**
  - **Intel 14nm – including power device SEE failure related to firmware**
  - **AMD Ryzen 16nm – test reports**
  - **Samsung 14nm LPP/Snapdragon 820 SEE – Heavy Ion & Proton – test reports**
  - **RAD55xx radiation data (testing soon…)**
  - **Samsung 10nm/Snapdragon 835 SEE (details TBD)**
  - **Vorago VA10820/M4 (morphing to review effort)**
  - **GPU reports (see Ed Wyrwas' materials)**

Snapdragon 835

- **Samsung 10 nm**
  - **8 Kyro 280 CPUs**
  - **Adreno 540 GPU**
  - **Hexago DSP**

- **Using Intrinsyc's 835 Mobile Hardware Development Kit – Android only, which is not desired…**
- **This board uses package-on-package (they essentially all do)**
- **No avenue to put Linux on the board.**

Test Approach - Snapdragon 835

- Run codes under available operating systems
- Utilize debugging utilities (in this case the Android Debug Bridge)
- Run a suite of programs under the beam
  - Try to avoid when multiple programs are giving essentially the same data
- Compare the nominal debug utility output vs. that under the beam
  - If any deviation is observed in systems that are able to return data before a crash

- Note that the test efforts on the 820 showed that it is extremely difficult to expose to any number of heavy ions before a crash occurs.

The Snapdragon Profiler

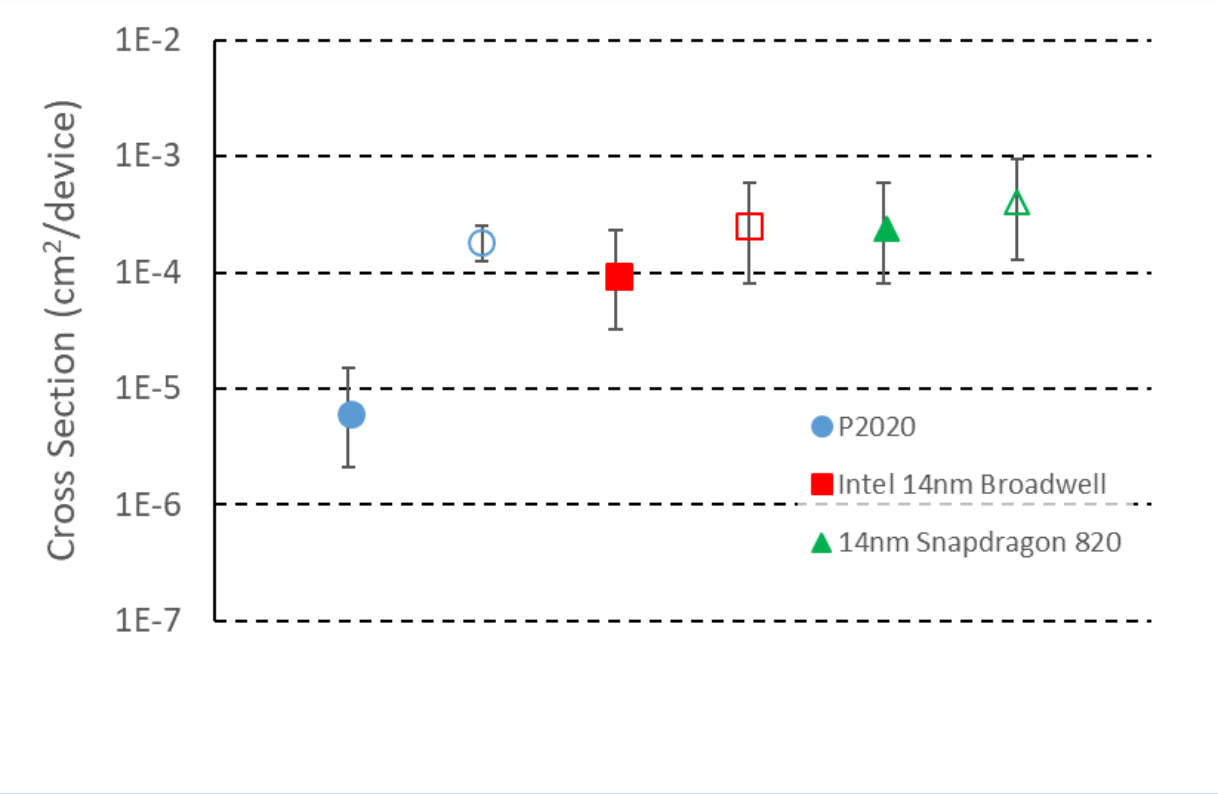
- **CPU Performance:**
  - Branch Misses
  - Cache Misses
  - Cache Miss Ratio
  - Cache Reference
  - Clock
  - Context Switches
  - Core Frequency
  - Core Load
  - Core Utilization
  - Cycles
  - Cycles/Instruction
  - Instructions
  - Page Faults
  - Task Clock
- **Memory Performance**
  - DDR Frequency
  - Utilization (bytes)
- **GPU Performance:**
  - Clocks/Second: Number of GPU clocks per seconds
  - % CP Overhead
  - % Bus Busy
  - Frequency
  - Temperature
  - % Utilization
  - Avg Bytes/Fragment
  - Avg Bytes/Vertex
  - Avg Memory Latency Cycles
  - CP Data Read (Bytes/sec)
  - Read Total (Bytes/sec)
  - SP Memory Read(Bytes/Second)
  - Texture Memory Read
  - Vertex Memory Read
  - VisStream Writes (Bytes/Sec)
  - Write Total

Snapdragon Applications

- All running under Android (looking for Linux alternatives… might change if another board can be found)
- Memory test (more effective than registers when running in OS)
- Matrix operations (transpose/multiplication)
- Image rotation application

- Evaluating some other applications, like Camera and Sensor, but lower priority
- Also partners with GPU-side

Open vs. Closed Info



- **Cross section for crashes while running “other” tests.**
- **Closed symbols are “low utilization”, while open symbols are “high utilization”.**
- **The P2020, although an SOC is easily configured to run in a very minimal mode. The Intel and Snapdragon devices are more realistic for new and future devices with minimal documentation.**

RHBD Processors

- RAD750 is old, but solid… but it's ~400 Dhyrstone 2.1 MIPS
- Modern processors are 20,000+ Dhrystone 2.1 MIPS

- But eventually we want to move to newer devices
  - Higher performance – orders of magnitude
  - Advanced architectures & features

- Devices/Architectures supported by NEPP
  - PowerPC → RAD5545 (NEPP supporting rad testing)
  - ARM → HPSC (informing NEPP efforts)
- We are working to:
  - Evaluate equivalent functional units
  - Establish viable ways to test these SOCs
  - Explore different operating configurations to compare high performance, and compare to high reliability operations

RAD5545 Efforts

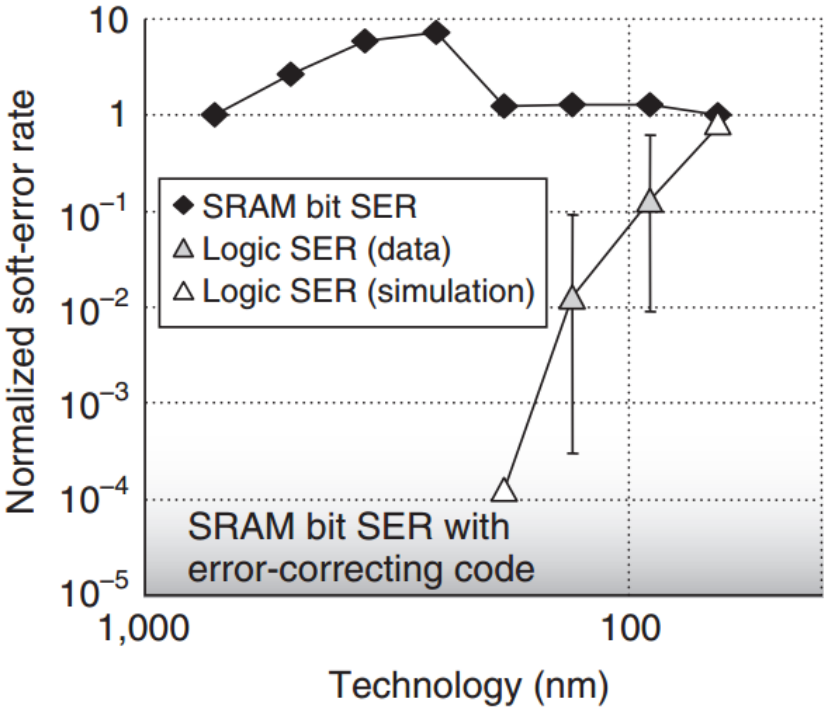
- Migrating existing P5020 and P2020 codes to be ready to explore RAD5545 capability
- Planning collaborative testing with BAE
- Focused on previous test methods

- But also augmenting with system-level performance testing…

- However, this is pushing the development of system-level performance evaluation.
  - We are looking into how to specify radiation performance in high performance systems with built-in fault tolerance.

RHBD Difficulties

- Bits have not been getting harder for SEE, in fact at the bit level SEE is much worse
- But bit SEEs are not the whole story
- This is making the old "< 1e-10 errors/bit-day" out of date – currently developing method of specifying here
  - By far all new RHBD devices easily beat this



Baumann, Texas Instruments
(*IEEE Design and Test of Computers,* May/Jun 2005)

- Need method to identify how to evaluate
  - Radiation performance per functional unit
  - Radiation tolerance vs. device configuration vs. performance per power
  - Under development for RAD5545, HPSC, and comparison to RAD750 and consumer devices

Future Directions

- **Continue working on 7 nm Samsung and 10 nm Intel devices as they become available.**
- **Continue efforts on GPUs, including embedded GPUs (such as in phones) and related machine learning algorithms and AI (See Ed Wyrwas' talk)**
- **Continue collaboration and evaluation of RHBD and COTS microcontrollers for things like CubeSats**
- **Establish a way to functionally compare the RAD5545, RAD750, HPSC, and other flight processors to enable something like an apples-to-apples comparison of radiation performance against system processing capability.**
  - **Also applies to when it might be good to move to something like a GPU as a coprocessor. "We lose a factor of availability for orders of magnitude more processing." – Ed Wyrwas**
- **Compare the performance of soft-core and hard-core processors performing the same workloads.**