Radiation Testing of Advanced Non-Volatile Memories

Edward Wilcox

ted.wilcox@nasa.gov

NASA / Goddard Space Flight Center

To be presented by Edward Wilcox at the 2018 NEPP Electronics Technology Workshop (ETW), NASA GSFC, Greenbelt, MD, June 18-21, 1, 2018.

Acronyms

- CMOS: Complementary Metal-Oxide Semiconductor
- COTS: Commercial Off The Shelf
- DRAM: Dynamic Random Access Memory
- ECC: Error-Correcting Code
- EDAC: Error Detection and Correction
- EEPROM: Electrically-Erasable Programmable Read-Only Memory
- FRAM: Ferroelectric RAM
- GEO: Geostationary Earth Orbit
- LET: Linear Energy Transfer
- MBU: Multiple Bit Upset
- MCU: Multiple Cell Upset
- MLC: Multi-level Cell
- MRAM: Magnetoresistive RAM
- NAND: Not AND (Flash Technology)
- NEPP: NASA Electronics and Packaging Program
- NVM: Non-Volatile Memory
- nvSRAM: Non-volatile SRAM
- QLC: Quad-level Cell
- RBER: Raw Bit Error Rate
- SBU: Single Bit Upset
- SEE: Single Event Effects
- SEFI: Single Event Functional Interruption
- SEU: Single Event Upset
- SLC: Single-level Cell
- SRAM: Static Random Access Memory
- SSD: Solid State Drive
- SSR: Solid State Recorded
- STT-MRAM: Spin-torque Transfer MRAM
- TID: Total Ionizing Dose
- TLC: Triple-level Cell
- UBER: Uncorrected Bit Error Rate

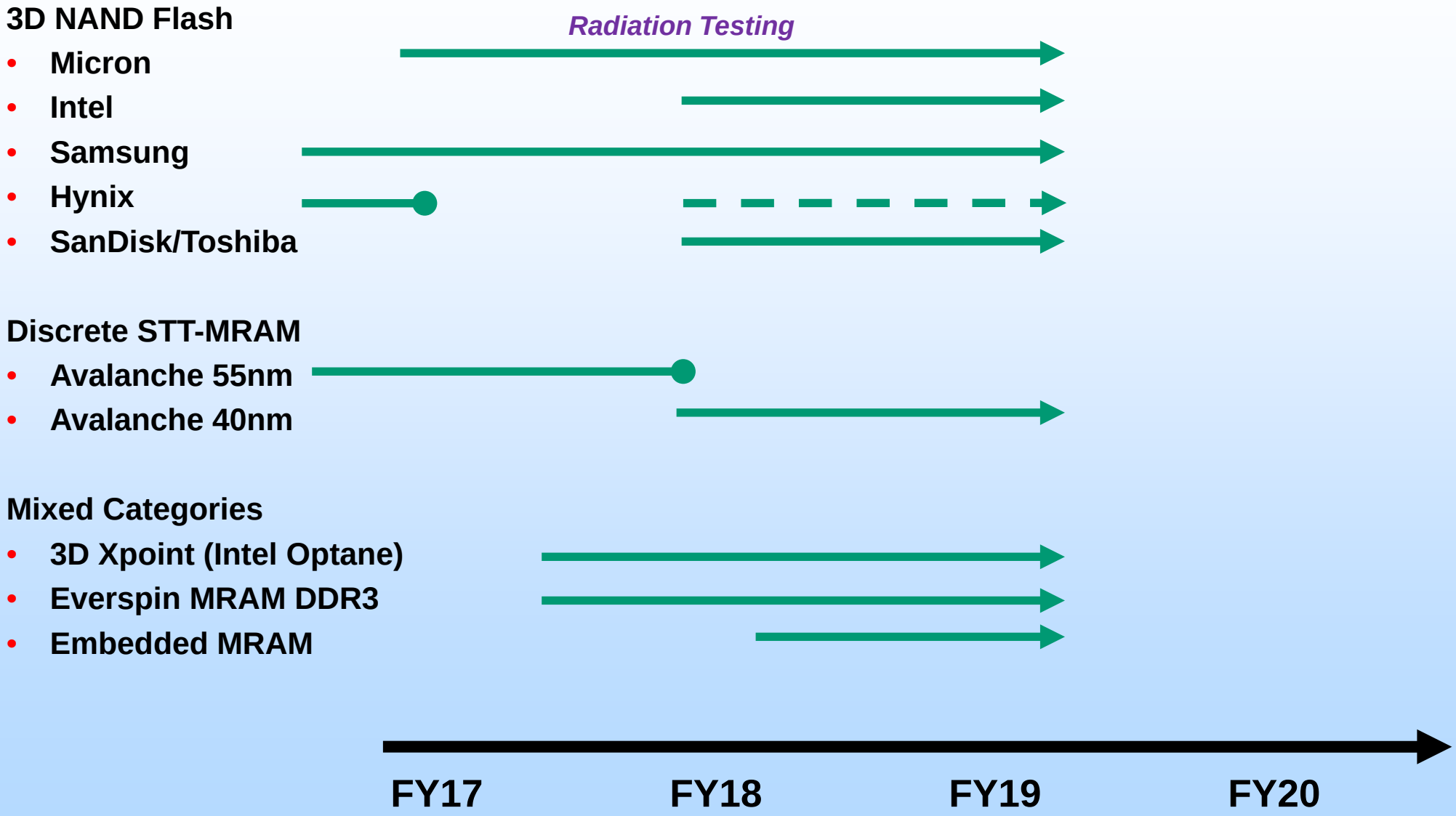
Outline

- Non-Volatile Memory Technologies
- Roadmap of Existing Efforts
- Recent Memory Testing Results
- Ongoing Testing
- Plans

NVM Technology

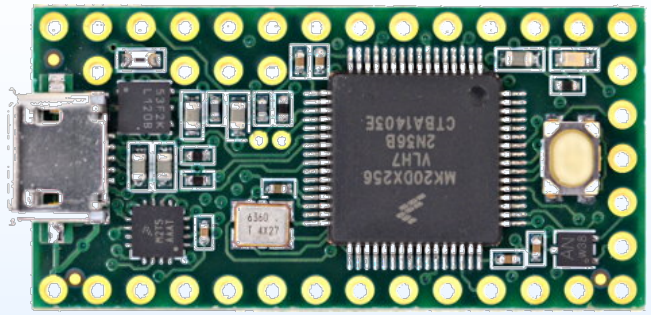
- **Advanced Non-Volatile Memories**
  - **Includes memory technologies or products used for long- and intermediate-term storage of data in a non-volatile storage cell**
  - **It IS: NAND/NOR flash, MRAM, ReRAM, FRAM, PCM, etc used in**
    - **EEPROMs**
    - **nvSRAMs**
    - **Solid-State Recorders**
    - **Boot PROMs**
    - **Etc**
  - **Embedded NVM or DRAM-like NVM technologies are a collaborative effort with other NEPP tasks (scaled CMOS process evaluation, DDR memories)**
    - **Obvious Example: Intel *512GB* Optane DIMM… pin-compatible with DDR4, but NVM**

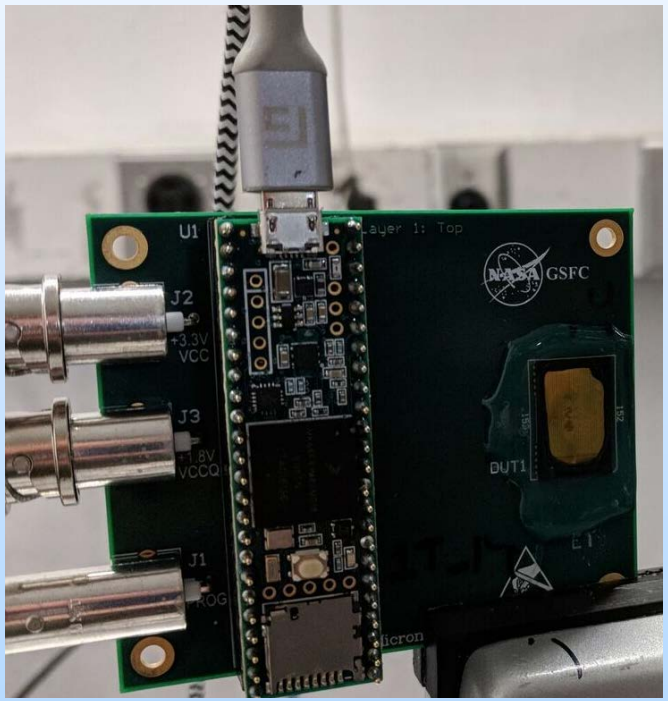
NVM Radiation Testing Roadmap

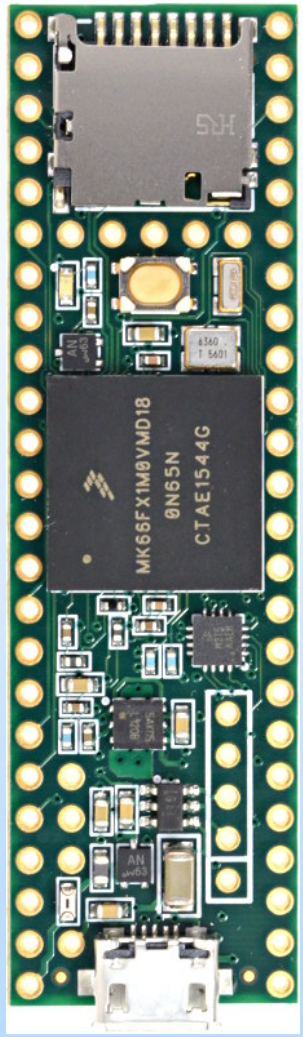


Our Memory Testing Approach

- Teensy 3.2 and 3.6 Arduino-compatible Microcontroller Boards
- < $30
- Easy toolset & programming, yet low-level quasi-real-time access
- Up to 240 MHz CPU core with 120 MHz data bus
- 10Mbps USB link to PC
- Not appropriate for DRAM, high-bandwidth, or timing-sensitive devices

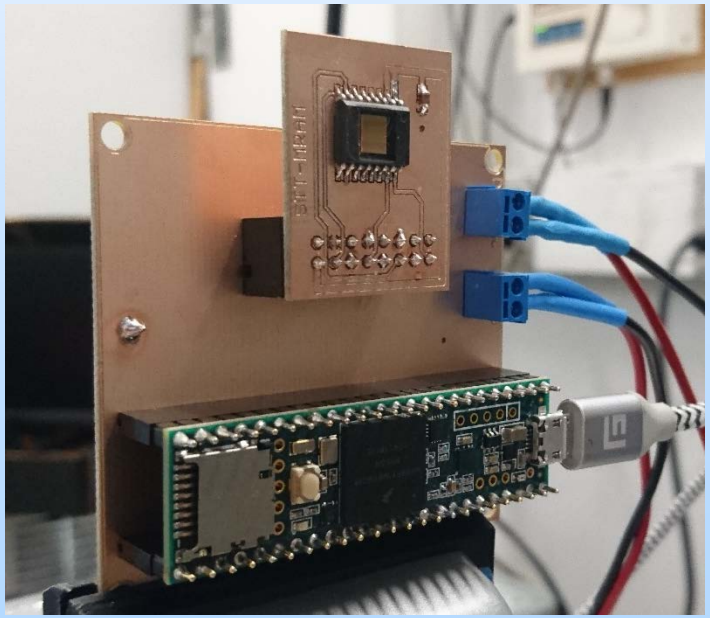






Recent Results – Avalanche STTMRAM

- pMTJ STT-MRAM
- 55nm CMOS
- 4Mb-8Mb serial nvSRAM functionality

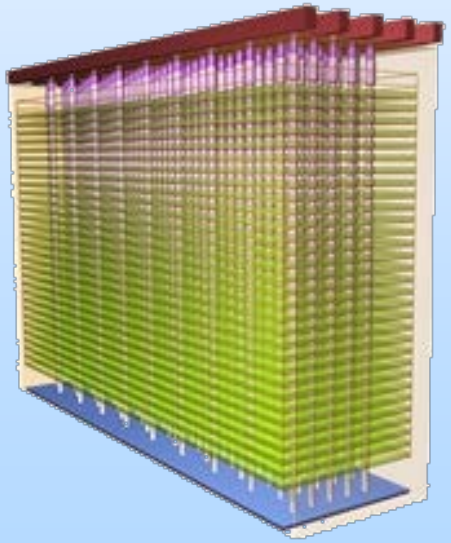


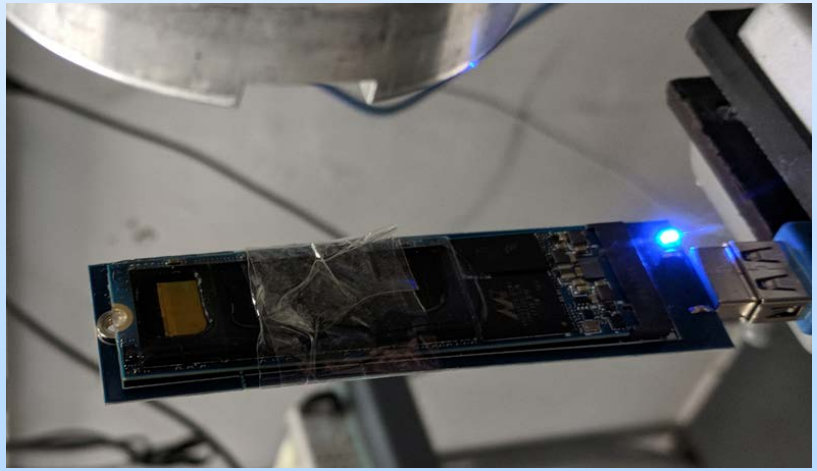
- Memory array cells are SEU hard:
  - None after 1.1x10^{7}/cm^{2} @ 85.4 MeV·cm^{2}/mg
  - None after 1x10^{7}/cm^{2} @ LET$_{eff}$ 120.8 MeV·cm^{2}/mg (45°)
- Low SEFI threshold, but low cross-section (<2x10^{-6}cm^{2})
  - No inadvertent writes noted
- >500 krad TID (including control circuitry)

Recent Results – 3D NAND Flash

- **Planar NAND flash limited by CMOS scaling**
  - **Step back a few nodes but grow vertically (32 to 96 layers!)**
- **Extensive SEE testing of Micron 32-layer 3D NAND**

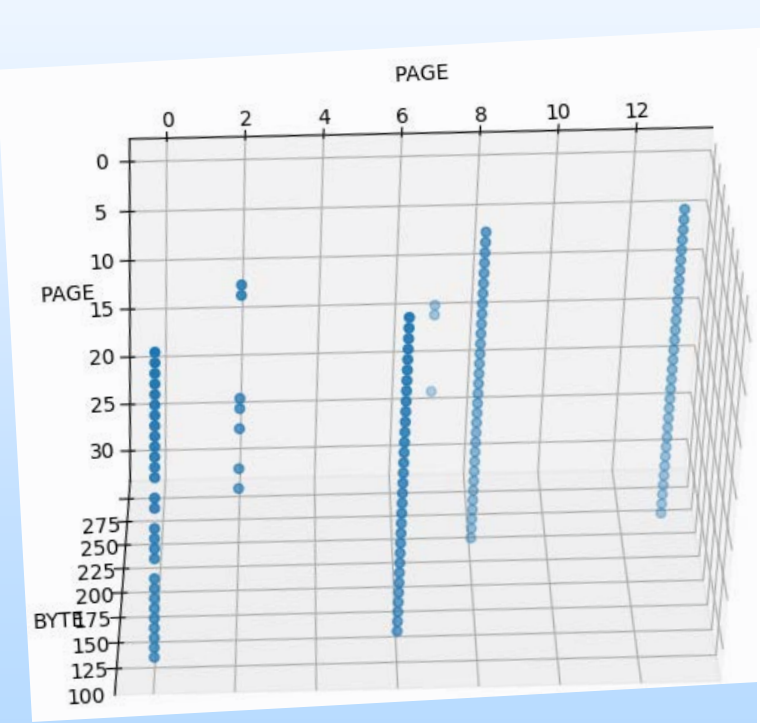
- **Early SSD test data on:**
  - **Intel, Micron 64-Layer**
  - **WD/SD/Toshiba 64-Layer**
  - **Samsung 64-Layer**
  - **more coming soon…**

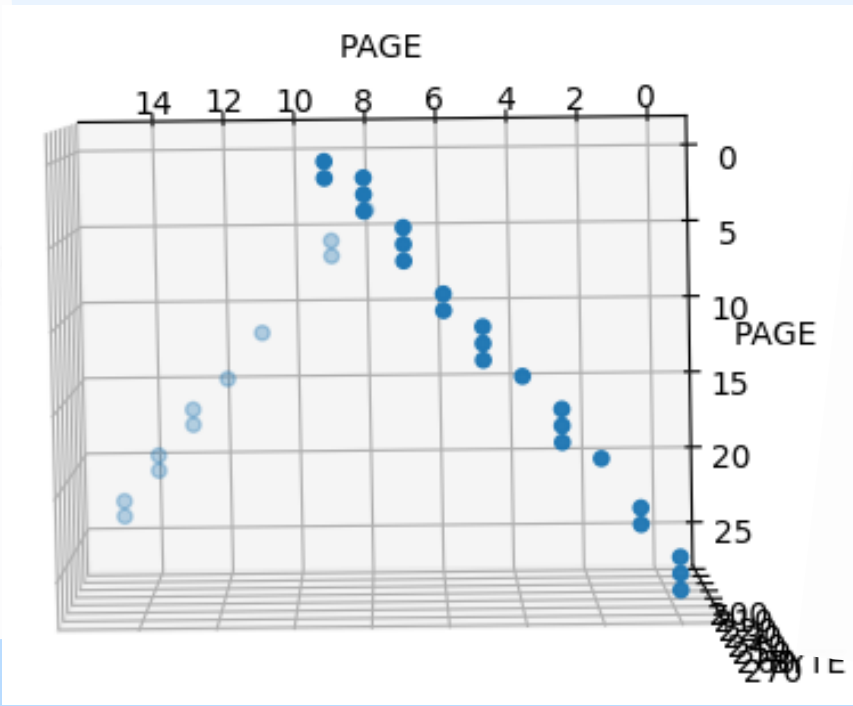


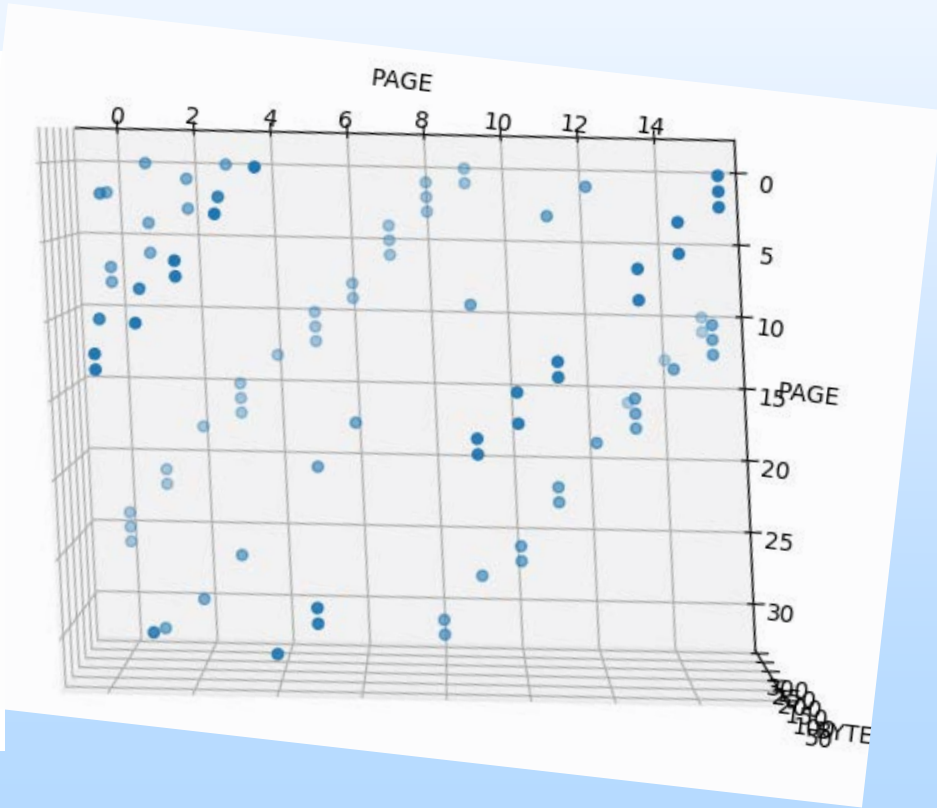


Recent Results -- 3D NAND Flash

- **3D memory structures require careful data analysis….**
- **When an SBU isn't an SBU → single-ion tracks through 3D array:**



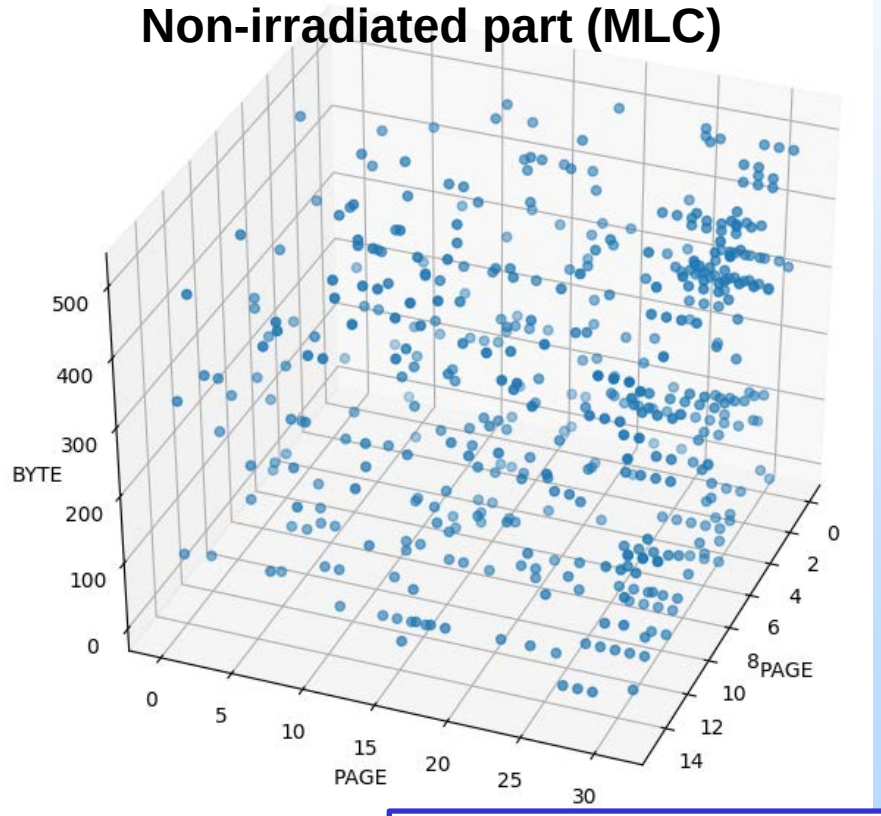




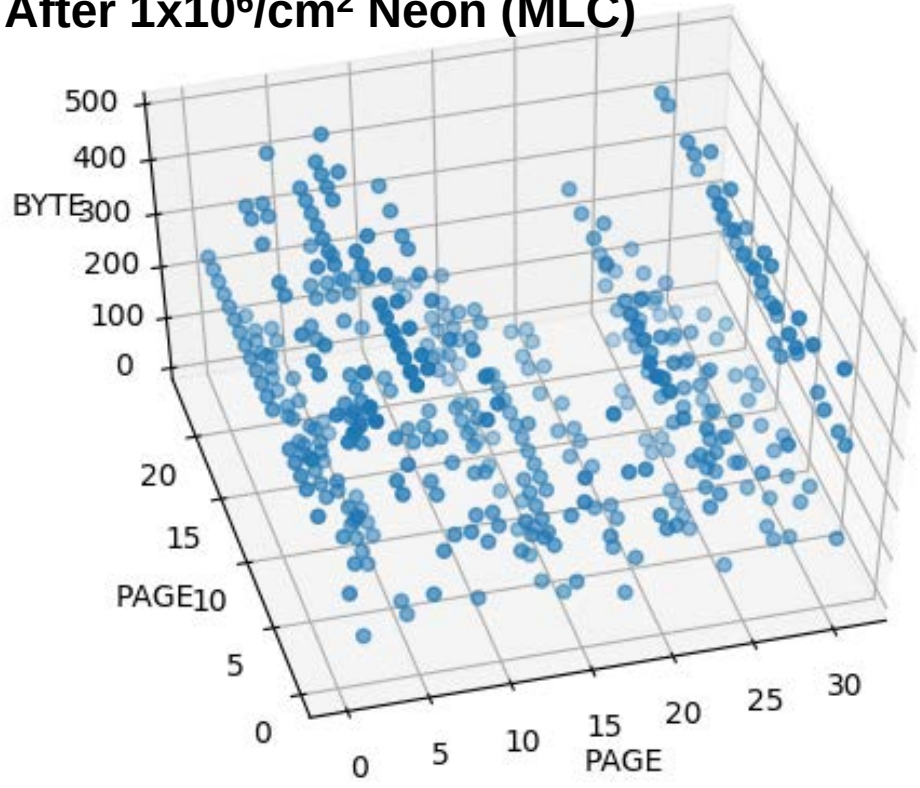
Recent Results – 3D NAND Flash

- **Manufacturers specify ECC based on normal “background” errors intrinsic to NAND flash (left)**

Non-irradiated part (MLC)



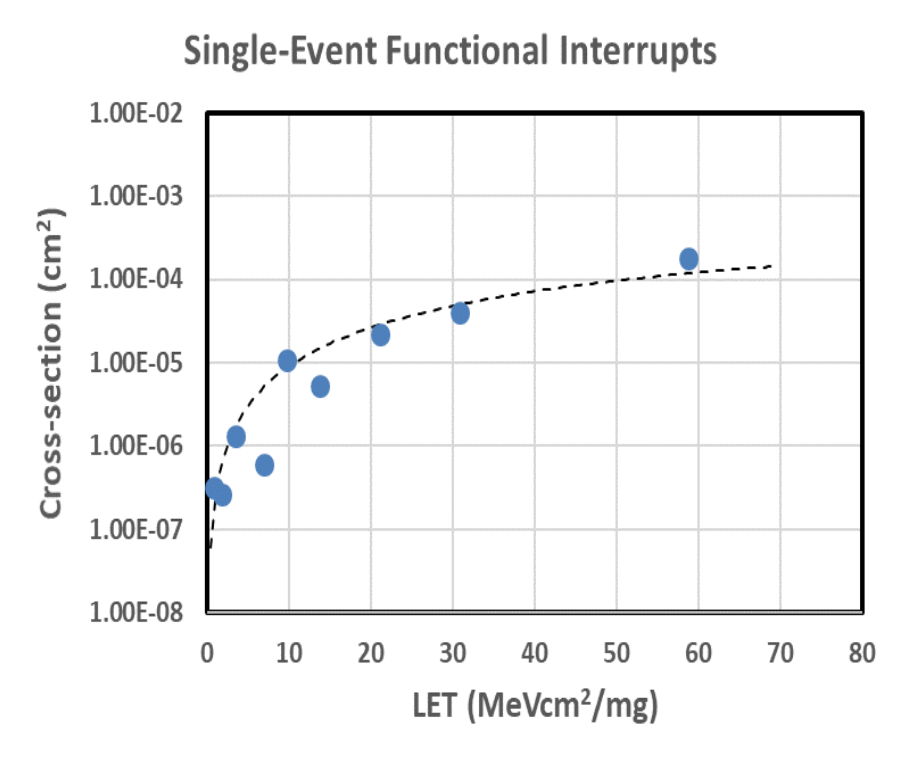
After 1x10^6/cm^2 Neon (MLC)



Will ECC built for (left) fix SEUs (right)?

Recent Results – 3D NAND Flash

- **Of course, individual bit upsets are only part of the puzzle:**
- **CMOS control circuitry remains highly susceptible to large block/page errors that required a device reset (SEFI)**



Ongoing Testing – 3D NAND Flash SSDs

- **Easiest way to access wide variety of state-of-the-art COTS flash**
- **By far the hardest way to test it!**
  - **Abstraction, logical address mapping, EDAC, etc**
  - **Number of upsets expected from SEU *low* compared to memory size and built-in error rate**
- **Can we observe general trends from manufacturer-to-manufacturer in state-of-the-art 3D NAND flash?**

Ongoing Testing – 3D NAND Flash SSDs

- First round of testing: Too few parts spread across too many MFG!
  - Low decapsulation yield on some parts led to unreliable operation
  - Very slow access time; must access entire memory space
- Results hard to generalize in a useful fashion:
  - Device might run to $1x10^{8}cm^{-2}$ without any “bad blocks” noted
  - Others: sudden emergence of large number of errors as ECC overwhelmed
- Second test: Irradiate large batch at different levels, then take time to carefully measure and post-process
  - Allow for thorough exercising of device post-irradiation
  - With enough parts, we can also look for SEFI this time
  - Not necessarily a “3D NAND” effect, but still the dominant error mode
- Hope to correlate block failure rate to “expected” block failure rate based on piece part data and knowledge of ECC implementation

Plans Moving Forward

- **3D NAND Flash**
  - **Piece-part testing when able, particularly as projects begin to use them!**
  - **COTS Solid-State Drive (SSD) testing for broad trends, manufacturer comparisons (more testing next week!)**
- **Non-Flash**
  - **Avalanche 40nm STT-MRAM SEE & TID testing ~Fall**
  - **Everspin MRAM testing collaborations with other NEPP tasks**
  - **3D X-Point (Intel Optane) SEE (HI & Proton) testing**
  - **Identify emerging non-flash technologies & partnership opportunities**